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INTRODUCTION TO CDMA

CDMA OVERVIEW

Code Division Multiple Access (CDMA) is based on technology originally developed by the Allies during World War II to resist enemy radio jamming. It has been significantly refined during the intervening decades, and is used today in digital cellular services and Personal Communication Services (PCS), as well as a variety of military applications.

The earliest radio transmissions were unintentionally spread across a broad frequency spectrum, much like CDMA. However, the proliferation of uses for radio, coupled with the inherent inability to discern the difference between one radio signal and another, led to change. This change was the division of the radio spectrum into specific bands and frequencies, or channels, to prevent one transmission from interfering with another. This change was made possible by improvements in radio filter technology and the advent of the vacuum tube.

With CDMA technology, we again spread the signal over a broad frequency of spectrum. CDMA breaks up a digitized voice transmission into small packets of encoded data which are then transmitted along with other transmissions across a broad band of spectrum. Each transmission is spread in bandwidth by its own encoding sequence so that no transmission has the same code. Although all transmissions are sent out simultaneously, the unique code allows the receiver to separate one transmission from all the others. The CDMA technology developed and patented by QUALCOMM® enables the receiver to identify and discern the desired signal from all other transmissions and sources of interference on the channel.

CDMA can be compared to a cocktail party. Everyone at the party is in the same room (like being on the same frequency channel) and talking at the same time. You can imagine that if all of the conversations in the room were in a language you didn't understand, they would all sound like noise. However, if just one conversation was in your native language, you could discern that conversation above all the rest. This is analogous to the concept of code division: if you know the code, you can discriminate one conversation from another.

DIFFERENCES BETWEEN CDMA AND TDMA

Time Division Multiple Access (TDMA) divides a channel into a number of discrete time slots assigned to each call. The use of a vocoder and digital technology allows the speech to be broken up into packets of data which can be interleaved with other voice packets and distributed over time in a regular sequence. Each voice signal is digitized by the system and then sent out in short bursts. The transmission happens so quickly that several conversations can occur at the same time, but none will be transmitted in exactly the same time slot as any other.

However, since TDMA utilizes narrow frequency bands, it is inherently limited by the number of channels and the number of time slots that can be put into each channel. The planned implementation of TDMA allows only a three-fold expansion of utilization. Even with the new innovations in voice encoding, the architecture of the currently proposed systems in the U.S. is limited to a maximum expansion of six times current analog cellular capacity, much less than the capacity of CDMA.

With CDMA, there are no regular time slots for the bits of data. When a caller stops talking, his or her transmitter instantly reduces power. When the caller resumes talking, the power is immediately increased. Because all other signals on the frequency are seen as noise, just like any other source of interference, the reduction in power reduces the interference to all other calls. In this way, a large number of messages can be spread across a wide channel without significantly interfering with each other. The capacity of the system

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is limited only by the signal-to-noise ratio and the corresponding ability to differentiate the transmission from all other noise on the channel. Because CDMA does not allocate a tangible and limited resource such as time or frequency, the capacity limit is "soft". On any given frequency, the capacity is only reached when the noise level makes it impossible to clearly differentiate a transmission from surrounding noise.

ENHANCED CDMA SECURITY

CDMA provides greater privacy through its unique enhanced security features. CDMA utilizes digital encoding for every telephone call or data transmission. One of 4.4 trillion unique codes are assigned to every communication, which distinguish it from the multitude of calls simultaneously transmitted over the same broadcast spectrum. Only your CDMA phone has the right code to receive your conversation. With CDMA digital encoding, even your phone number remains private — that means no more cloning.

CDMA SOFT HANDOFFS

A handoff occurs when a call has to be transferred from one cell to another as the user moves between cells. In a traditional cellular or TDMA handoff, the connection to the current cell is broken, and then the connection to the new cell is made. This is known as a break-before-make, or hard handoff. Since all cells in CDMA use the same frequency, it is possible to make the connection to the new cell before leaving the current cell. This is known as a make-before-break or soft handoff. Soft handoffs allow for fewer dropped calls and better sound quality. TDMA systems are not capable of performing soft handoffs.

VARIABLE RATE VOCODER

The key to efficiency in digital voice transmission is the conversion of an audio signal into binary numbers. This allows the digital signal to be compressed and grouped into packets of information. The increased spectral efficiency of digital cellular is partly due to the use of a vocoder to convert speech into digital code. The vocoder samples the spoken word, but only encodes a skeleton of the actual word. The model for reconstructing the human speech sounds is contained in the receiver which is able to reconstruct the desired sound when it receives the transmitted code, much as a music synthesizer can emulate a saxophone or piano. The vocoder, in effect, characterizes the instrument, the human voice, as it changes and describes these changes to the speech synthesizer in the receiver, allowing very natural speech to be produced. Therefore, fewer bits of information need to be transmitted per unit time.

CDMA achieves performance near toll-quality through a unique variable-rate vocoder developed by QUALCOMM which effectively achieves the same voice quality of other vocoders, but does so with an average of half the rate of standard vocoders. While a standard vocoder is either on, transmitting background noise as well as blank space at full rate, or off, QUALCOMM's variable rate vocoder outputs data at various rates between 0.8 kbps (⅛ rate) and 8.55 kbps (full rate) for the rate set 1 option, or various rates between 1.0 kbps (⅛ rate) and 13.3 kbps (full rate) for the rate set 2, PureVoice™ option. Background noise is encoded at the lower quality level of ⅛ rate. The vocoder samples speech every 20 milliseconds. As soon as it detects speech coming up, it doubles the encoding rate to ¼ rate, then ½ rate as the intensity increases, then full rate during high energy speech, while achieving full rate voice quality at all times. As speech drops off the process reverses, falling first to ½ rate, then ¼ rate, then ⅛ rate for the background noise. In reality the actual average data rate is significantly less than ½ of full rate.

Variable rate vocoding cannot help TDMA because it is incapable of providing for variable rate packet sizes in a way that would allow additional sharing of the channel.

POWER CONTROL

One of the keys to the success of CDMA is the power control technology developed by QUALCOMM. Through the use of sophisticated open loop and closed loop control circuitry, the system constantly monitors and adjusts mobile unit power output to the minimum level required to maintain optimum clarity and quality

of voice reception. The open loop circuit monitors the transmitted signals from the cell which allows the mobile to predict the transmitter power necessary to reach the cell. The closed loop circuit evaluates the actual quality of the transmission at the cell station and adjusts each mobile unit's power to the minimum level required to maintain high quality voice performance.

This breakthrough in power control technology equalizes the power of each mobile at the cell site, regardless of how close or far away it is from the tower. Equalizing the power level makes each mobile unit look the same to the cell site and minimizes the total interference. Minimizing power output also results in significant advantages in battery power conservation.

CDMA SYSTEM MAINTENANCE

Systems engineering will be easier with CDMA than other technologies because, unlike other systems, CDMA requires very little frequency coordination. This is due to the fact that the same frequency band is reused in every cell. Additionally, as a system grows, it will not be necessary to continually re-engineer the existing system to coordinate frequencies.

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MSM2300

MOBILE STATION MODEM

OVERVIEW

APPLICATION DESCRIPTION

The dual-mode Code-Division Multiple-Access/ Advanced Mobile Phone System (CDMA/AMPS) cellular telephone is a complex consumer communications instrument that relies heavily upon digital signal processing. To simplify the design and reduce the production cost of the subscriber unit, QUALCOMM has developed a Mobile Station Modem (MSM2300), an Analog Baseband Processor (BBA2) and Automatic Gain Control (AGC) Amplifiers, Q5500 and Q5505. These devices perform all of the signal processing in the subscriber unit, from IF to audio.

The QUALCOMM MSM2300 is the fourth generation ASIC in the MSM family. The MSM2300 offers improved functionality, lower cost and significant power savings over previous MSM versions. The MSM2300 integrates functions that support a dual-mode CDMA/FM subscriber unit. Subsystems within the MSM2300 include a CDMA processor, a Digital FM (DFM) processor, a QUALCOMM Codebook Excited Linear Predictive (QCELP®) Vocoder, a 80C186EC microprocessor and assorted peripheral interfaces that are used to support other functions.

The MSM2300 (Figure 1) demodulates Rx digital baseband data from the BBA2. The BBA2 converts the modulated IF signal from the RF section of the subscriber unit into digital baseband data. For transmission, the MSM2300 modulates and sends digital baseband data to the BBA2. The Tx signal path of the BBA2 converts Tx digital baseband data into modulated IF. The MSM2300 communicates with the external RF and analog baseband circuitry of the subscriber unit to control signal gain in the RF Rx and Tx signal paths, reduce baseband offset errors and tune the system frequency reference.

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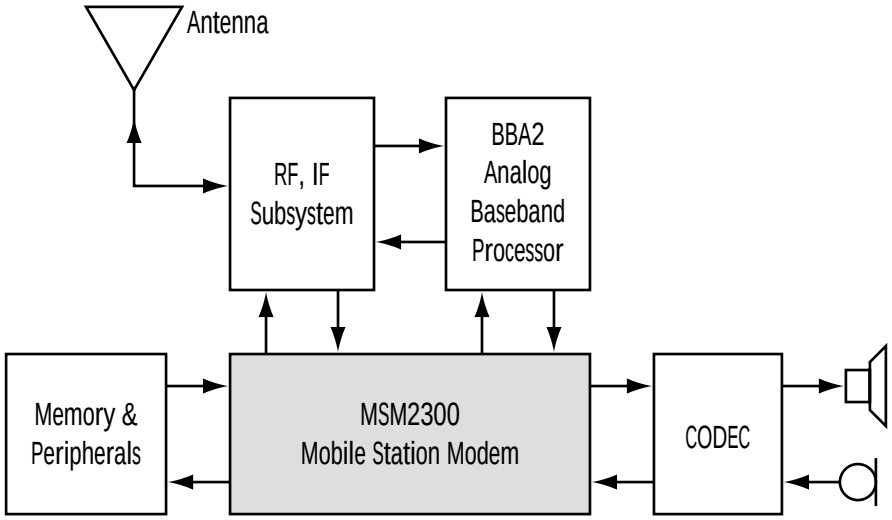
Figure 1. Typical Subscriber Unit Block Digram



The MSM2300 performs baseband digital signal processing and executes the subscriber unit system software. It is the central interface device in the subscriber unit, correlating RF, baseband and audio circuits, as well as memory and user interface features. The user interface of the subscriber unit typically includes the keypad, LCD display, ringer, microphone and earpiece. These are either under the direct or indirect control of the MSM2300. The MSM2300 also contains complete digital modulation and demodulation systems for both CDMA and AMPS cellular standards, as specified in IS-95-A.

The subscriber unit system software controls most of the functionality and activates the features of the subscriber unit. System software is executed by an embedded 80C186EC microprocessor within the MSM2300.

The CODEC interfaces directly with the microphone and earpiece, converting analog audio signals from the microphone into digital signals for the vocoder. The CODEC also converts digital audio data from the vocoder into analog audio for the earpiece. The MSM2300 supports an auxiliary external Pulse Coded Modulation (PCM) interface. The auxiliary CODEC is optional within the subscriber unit.

The MSM2300 is available in three package styles. A 208-pin Plastic Quad Flat Pack (PQFP) is available for low-volume system development applications. The 208-pin version allows connection to an MSM In-Circuit Emulator (MICE) for software development purposes. For high-volume subscriber unit production, a 176-pin Thin Quad Flat Pack (TQFP) and a 196-ball Plastic Ball Grid Array (PBGA) are available. These package styles do not allow access to the MICE Mode. The 196-ball PBGA is only one third the size of the 176-pin TQFP making it perfect for very dense subscriber unit applications.

The MSM2300 is fabricated in an advanced submicron CMOS process. The device operates between 2.7 and 3.6 V for low-power consumption and long talk time. As the subscriber changes modes, the MSM2300 powers down unused circuits to keep power consumption to a minimum.

The MSM2300's electrical specifications, mechanical specifications and pin functions are compatible with the MSM2.2. The MSM2300 has many internal functional enhancements and new debugging features, yet the programming requirements have remained as backwardly compatible as possible allowing a smooth migration from the MSM2.2.

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MSM2300 FEATURES

MSM2300 GENERAL FEATURES

- Supports IS-95A compliant CDMA and AMPS subscriber units
- Low 2.7 to 3.6 V DC power voltage operation
- Internal DFM subsystem for AMPS operation (with BBA2-shrink)
- Software-controlled power management features
- Advanced submicron CMOS design
- Three package versions available: A 176-pin TQFP and a 196-ball PBGA for high-volume production and a 208-pin PQFP development version. (The 208-pin version supports MICE for system development.)
- ANSI/IEEE 1149.1 Testability

MSM2300 AUDIO PROCESSING FEATURES

- 8 kbps vocoder
- 13 kbps vocoder
- Accepts an independent external vocoder clock source
- Support for 9600 bps and 14.4 kbps data rates
- Support for an external, user-supplied vocoder
- Dual-Tone Multiple-Frequency (DTMF) generation
- DTMF detection (CDMA Mode only)
- Earseal Echo Cancellation (ESEC) (CDMA Mode only)
- Programmable digital filters for audio signal path compensation in both CDMA and AMPS Modes
- Supervisory Audio Tone (SAT) transponding in FM Mode
- Voice Operated Switch (VOX)

MSM2300 MICROPROCESSOR SUBSYSTEM FEATURES

- Embedded industry-standard Intel® 80C186EC microprocessor subsystem
- Watchdog and sleep timers
- Interrupt controller with support for both internal and off-chip interrupt driven devices
- DMA controller with support for searcher DMA transfers (on-chip only)
- Chip select circuitry with direct support for RAM, ROM/FLASH, EEPROM, an LCD display and two other devices
- Address latches for demultiplexed address/data busses
- Programmable wait state generator
- Designed to operate with up to 20 MHz microprocessor clock frequency

MSM2300 SUPPORTED INTERFACE FEATURES

- Support for up to two external µ-Law, A-Law or linear CODECS from various manufacturers
- Bi-directional serial data port with 64 byte RX and 64 byte TX FIFO buffers and hardware handshaking
- Direct interface to Analog Baseband Processor (BBA2/Q5312)
- More than 30 general purpose I/O pins (several with interrupt capability)
- Interface for an external keypad
- Can use up to 1 MByte of external RAM & ROM, and supports up to 1 MByte of EEPROM with optional bank switching
- Support for either 8-bit or 16-bit external RAM
- Two spare Pulse Density Modulated (PDM) outputs for user-defined analog control
- General purpose programmable M/N counter output
- Ringer generation circuitry

MSM2300 ENHANCEMENTS OVER MSM2.2

- Through integration, the MSM2300 consumes significantly less power and provides more flexibility than QUALCOMM's MSM2.2.
- The MSM2300 searcher engine can operate at rates up to eight times faster than the searcher provided in the MSM2.2, allowing for faster acquisition and neighbor list search intervals.
- The MSM2300 searcher reports the best four local maxima peaks per search window, reducing microprocessor overhead. Also, the MSM2300 searcher reports the position of the multipath

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peaks with a higher resolution, allowing greater precision than the searcher provided in the MSM2.2.

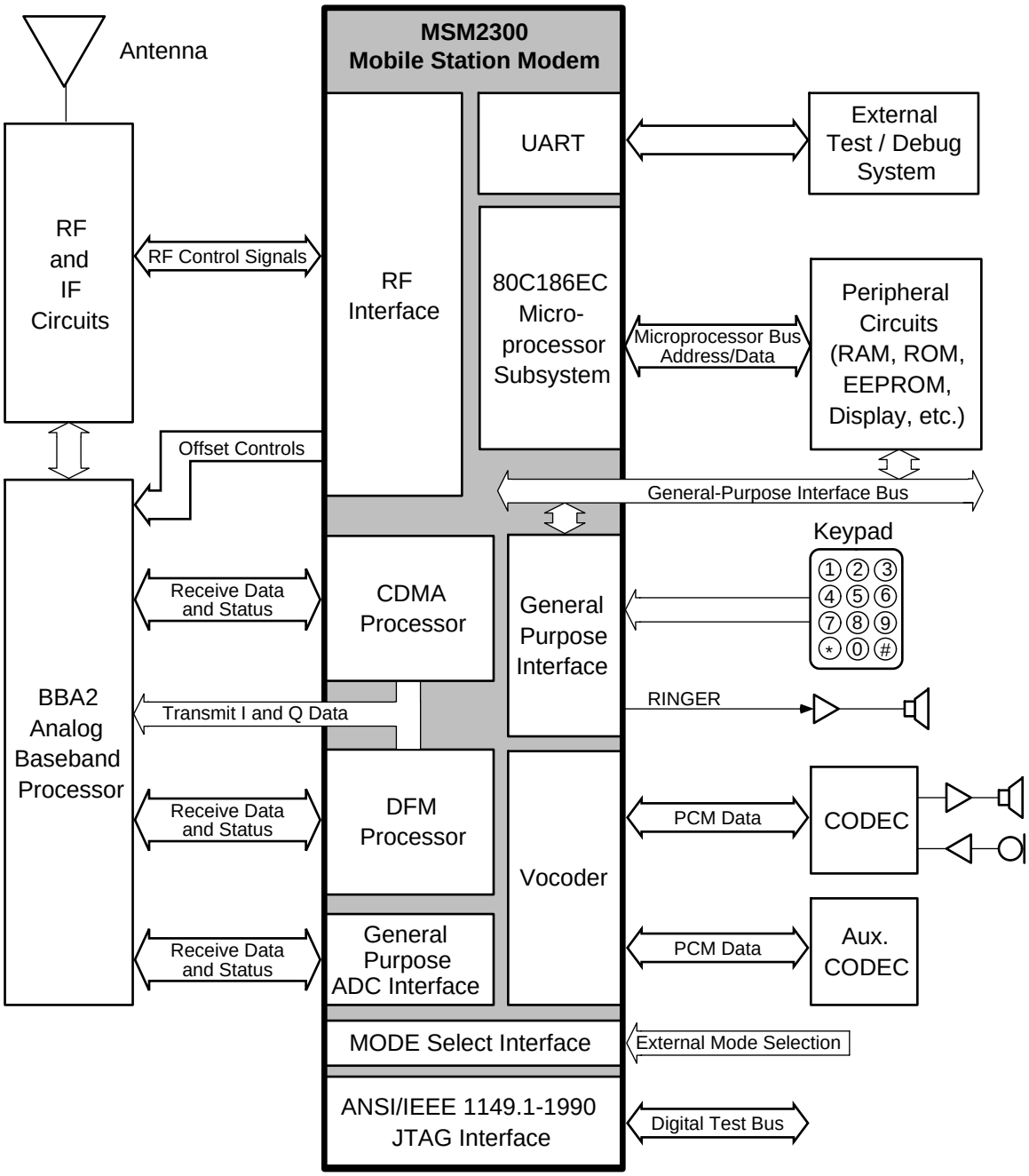
- The MSM2300 uses an enhanced Viterbi decoder resulting in a 0.5 - 0.7 dB improvement in 14.4 kbps rate-set operation, as compared with the MSM2.2.
- The MSM2300's RF subsystem has been enhanced over the MSM2.2 to improve intermodulation spurious response attenuation as outlined in IS-98, Section 9.4.3.
- The MSM2300 vocoder clock source is more flexible than the MSM2.2, and now includes XTAL_IN DIV 3, GPIO28 DIV 2, XTAL_IN DIV 2, CHIPX8 and GPIO28, each as possible clock sources.
- Both the MSM2300's CDMA VOX and DFM VOX have been enhanced over the MSM2.2 for improved performance.
- The UART's Rx and Tx FIFO sizes are double the FIFO sizes of the MSM2.2.
- The MSM2300's internal 80C186EC serial port is available for use as a second UART.
- The MSM2300 M/N counter has a larger range than the M/N counter provided in the MSM2.2.
- The MSM2300 has improved clock management features over the MSM2.2.
- Microprocessor power-down during Slotted Paging Mode is now supported.
- The MSM2300's electrical specifications, mechanical specifications and pin functions are compatible with the MSM2.2. The MSM2300 has many internal functional enhancements and new debugging features, yet the programming requirements have remained as backwardly compatible as possible, allowing a smooth migration from the MSM2.2.

DEVICE OPERATION

This section explains the relationships between each of the MSM2300 subsystems and its internal blocks and circuits. It also describes how the device performs signal processing tasks within the subscriber unit.

This section is divided into subsections representing the major subsystems. Figure 2 shows the subsystems, blocks and circuits within the MSM2300 and their interconnection to areas within the subscriber unit.

Figure 2. MSM2300 Functional Block Diagram



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RF INTERFACE

The RF Interface communicates with the subscriber unit's external RF, IF and analog baseband circuitry. Signals to this circuitry control signal gain in the RF Rx and Tx signal path, reduce baseband offset errors and maintain the system's frequency reference.

The RF Interface performs the following functions:

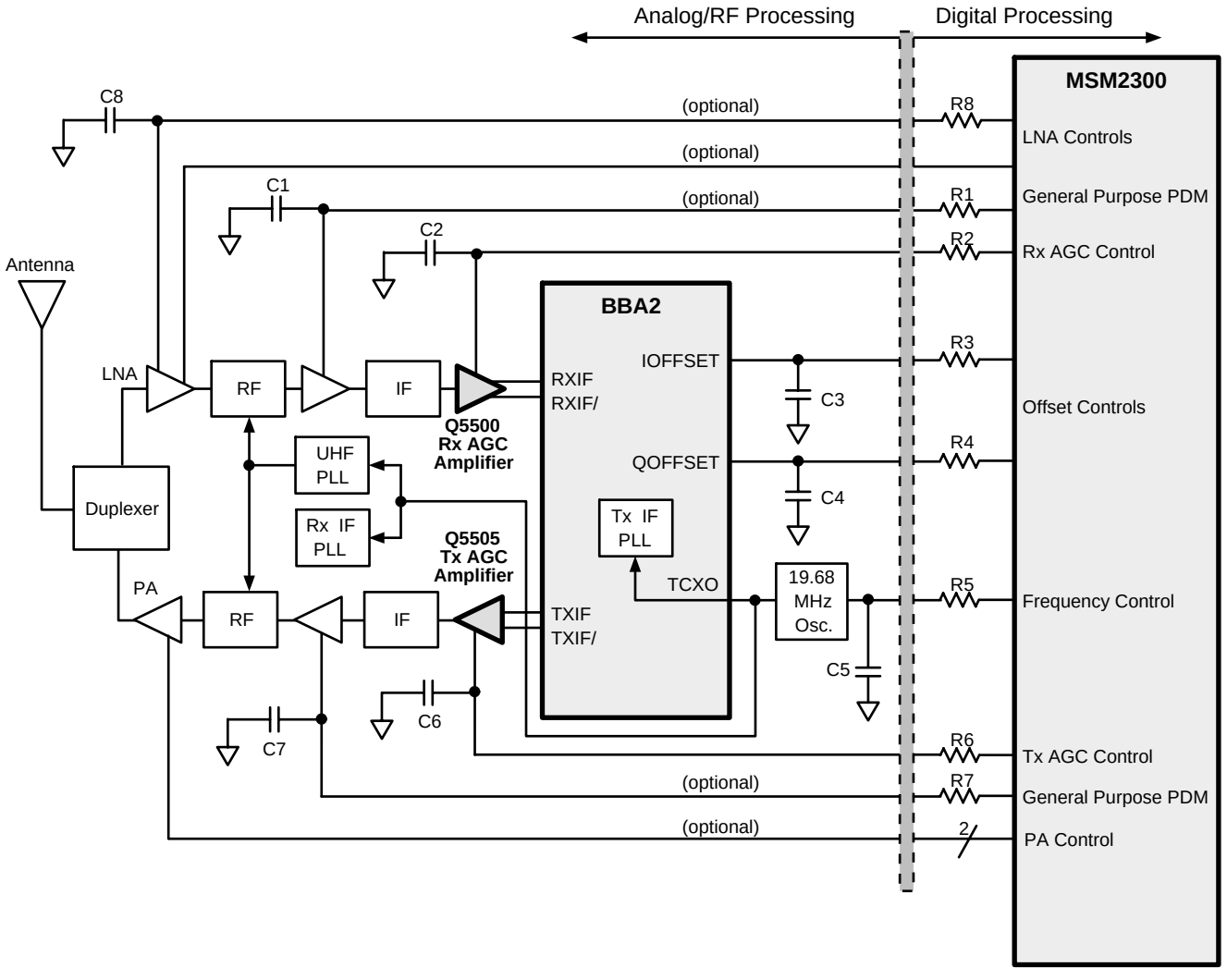
- Adjusts the I and Q channel baseband data offsets
- Tunes the master oscillator frequency (and the UHF and IF frequencies)
- Controls IF signal gain in the Rx and Tx signal paths
- Controls Power Amplifier (PA) and Low-Noise Amplifier (LNA) characteristics using digital control signals

The MSM2300's RF subsystem is an enhancement of the MSM2.2 improving intermodulation spurious response attenuation as outlined in IS-98, Section 9.4.3.

The RF Interface uses digital circuitry to monitor and control analog parameters in the BBA2 and the subscriber unit's RF subsystem. Figure 3 shows the RF Interface control signals to the BBA2 and the subscriber unit's RF subsystem.

PDM signals are filtered using an RC network to produce analog control voltages. These PDM signals include AGC controls, I and Q offset controls and a frequency adjust for the master frequency and timing reference oscillator. Two general-purpose PDM signals are available to supply user-defined control and calibration.

Figure 3. RF Interface Block Diagram to BBA2 and RF Subsystem



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In addition to PDM signals, the RF Interface has several digital control signals. These signals are used to configure and program the LNA and PA, save power in Sleep Mode and monitor the RF subsystem's phase-locked loops.

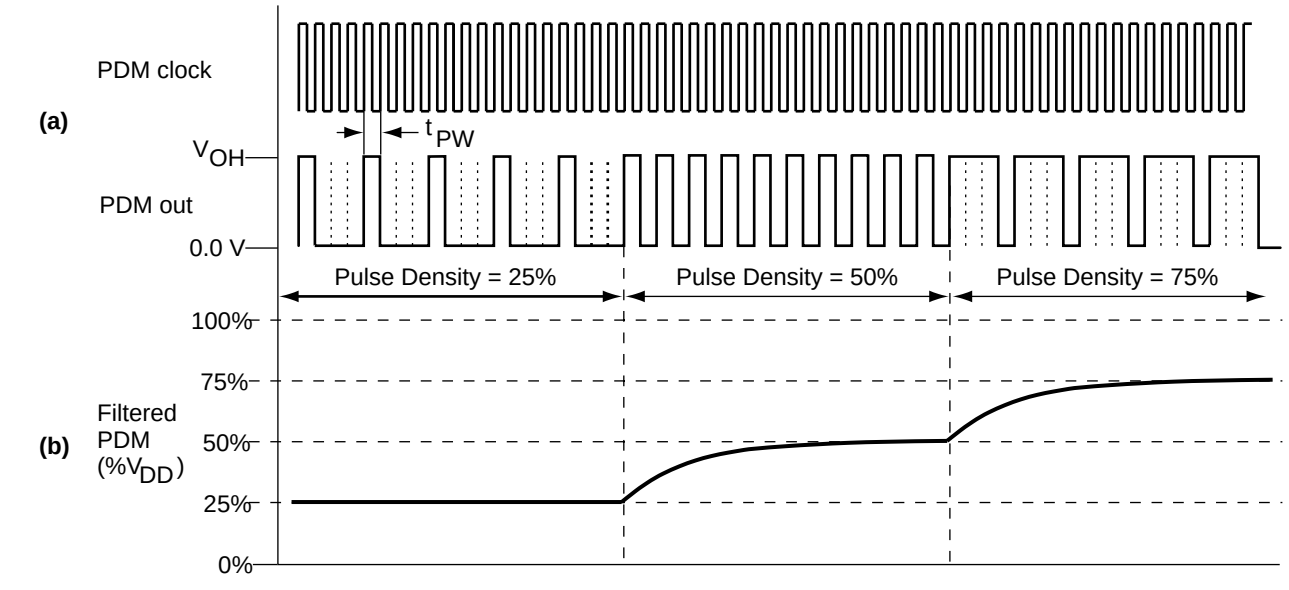
There are separate CDMA and DFM control loops that generate PDM signals. A multiplexer connects the appropriate PDM signal to its corresponding output pin. The multiplexer's select input determines the subscriber unit's operating mode (DFM or CDMA). Digital I and Q components from the Rx signal path of the BBA2 are the fundamental inputs to the RF Interface. The RF Interface uses these I and Q components and digital signal processing functions to calculate control values for the PDM outputs.

PDM OUTPUT SIGNALS

The RF Interface uses PDM output signals to control analog functions in the BBA2 and analog circuits in the subscriber unit's RF subsystem. PDM is a method used to convert digital control values into analog control voltages. PDM signals are streams of constant-width pulses (top of Figure 4) that are RC-filtered to develop DC voltages for controlling amplifier and oscillator components in the subscriber unit's RF subsystem. The RC-filtering of PDM signals is shown in Figure 4. The RC components are located between the MSM2300 and the analog control voltage input of the controlled component. The low-pass RC filter produces a low-ripple DC control voltage for AGC amplifiers and other analog circuit functions.

Pulses from PDM outputs have a rate of occurrence (density) proportional to a corresponding digital PDM value determined by (or stored in) the MSM2300. The density of the PDM pulse stream is the number of pulses that occur within a given time interval. For example, in Figure 4 pulse densities of 25%, 50% and 75% are shown from left to right, respectively. The pulse stream is smoothed using a single-pole RC low-pass filter. The DC component of the filtered pulse stream is directly proportional to the density of the pulse stream multiplied by the logic high voltage, V_{OH}, of the MSM2300. The operating mode (DFM or CDMA) determines the PDM clock frequency and pulse width. In DFM Mode, the PDM clock rate is TCXO/4 (4.92 MHz) and the minimum pulse width is 203 ns. In CDMA Mode, the PDM clock rate is CHIPX8 (9.8304 MHz) and the minimum pulse width is 101.7 ns.

Figure 4. Digital PDM and Filtered Analog Waveforms



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VOCODER SUBSYSTEM

The MSM2300 has an internal vocoder supporting both 8 kbps and 13 kbps vocoding; it also supports an external vocoder. The internal vocoder functions in both CDMA and DFM Modes. In CDMA Mode, the vocoder converts digital PCM samples from the CODEC into compressed packets for transmission. The vocoder encodes and decodes packets using QUALCOMM's QCELP speech algorithm. When receiving, the CDMA vocoder takes packet data from the demodulator and produces digital PCM samples for the CODEC. In DFM Mode, the vocoder acts as a DSP (filtering, gain control, limiting), processing digital audio samples during both receive and transmit operation.

CDMA VOCODER

In CDMA Mode (digital IS-95-A operation), the vocoder performs QCELP encoding of PCM samples into reverse link frames and QCELP decoding of forward link frames into PCM samples. The vocoder compresses (encodes) speech into a low bit-rate signal and reconstructs (decodes) compressed speech from a low bit-rate signal, all without reducing sound quality. Speech is coded using a sophisticated model of human speech reproduction. This model includes components relating to spectral, pitch and noise characteristics of speech. In the MSM2300, the vocoder is capable of both 8k and 13k QCELP for embedded voice processing. The internal vocoder may also be bypassed in CDMA Mode, allowing an external vocoder to be used.

The MSM2300 vocoder clock source is more flexible than the MSM2.2, and now includes XTAL_IN DIV 3, GPIO28 DIV 2, XTAL_IN DIV2, CHIPX8 and GPIO28 each as possible clock sources.

In CDMA Mode, the vocoder QCELP algorithm uses codebooks to vector quantize the residual speech signal. QCELP differs from CELP in that it produces a variable output data rate based on the level of speech activity. The QCELP algorithm adjusts the data rate based on the energy in the speech signal. Higher data rates are used for active, high-energy speech segments and lower data rates are used for silent, low-energy periods. Low energy periods occur during natural pauses in speech that occur when listening, exhaling or pausing between words and syllables. An intermediate rate is used when the input speech signal energy is between thresholds, or when transitions between speech and silence occur. The vocoder encodes active, high-energy speech segments at the full-rate of 13 kbps (for 13k Mode) or 8 kbps (for 8k Mode) producing high-quality speech, while background noises and pauses in speech are coded at 1 kbps (eighth-rate), creating a low average data rate without affecting speech quality.

For the reverse link, analog speech produced by the microphone is converted to digital PCM samples using the subscriber unit's CODEC. The PCM samples are passed to the vocoder for QCELP encoding to compress the speech samples. The encoding rate is determined by the vocoder which formats the encoded speech samples as data packets. A new data packet with data rate information is read by the microprocessor every 20 ms. The microprocessor then sends the data packets to the reverse link subsystem where the information bits are convolutionally encoded, interleaved, modulated and passed to the CDMA DACs on the BBA2, forming the reverse link Tx waveform.

Vocoder decoding is done near the end of the CDMA Rx signal path, just before the subscriber unit CODEC. As the subscriber unit receives the forward traffic channel, Rx data flows from the BBA2's CDMA Analog-to-Digital Converters (ADCs) to the CDMA demodulator for demodulation and symbol combining. After symbol combining, the data is passed to the deinterleaver and the Viterbi decoder, where deinterleaving and error-correction occur. The microprocessor moves the recovered information bits (packets) into the vocoder (as data packets) every 20 ms. The vocoder then uses the QCELP algorithm to reconstruct speech from the data packets.

Along with the data packets, the microprocessor sends data rate information to the vocoder. Data rate information tells the vocoder which data rate was used to encode the current data. After decoding the data packet at the appropriate data rate, the vocoder pulse code modulates the resulting speech samples and passes them to the CODEC where they are converted to an analog speech waveform.

The CDMA vocoder can also perform echo-cancellation, two-stage rate reduction (13k only), DTMF tone generation and detection and VOX for hands-free operation. Both the MSM2300's CDMA VOX and DFM VOX have been enhanced over the MSM2.2 to reduce power consumption. There is also an audio loop-back function for testing the CODEC interface.

DIGITAL FM (DFM) VOCODER

In DFM Mode (analog IS-95A), the vocoder performs digital signal processing of both the transmit and receive audio data streams. During an AMPS phone call, Rx and Tx information is sent directly to the vocoder, reducing the need for microprocessor intervention in the signal stream. The vocoder then filters and formats the voice data for the external CODEC. Handset CODEC voice data is signal processed by the DFM vocoder and transferred to the DFM subsystem. In both CDMA and DFM Mode, the vocoder provides a direct PCM sample interface.

CDMA DIGITAL BASEBAND PROCESSOR

The CDMA digital baseband processor performs forward-link demodulation, time tracking and reverse-link modulation for CDMA digital baseband signals. The MSM2300 CDMA digital baseband processor has been enhanced to provide more integration and functionality than the CDMA processor in the MSM2.2. Figure 5 shows the MSM2300 CDMA Digital Baseband Processor block diagram.

SEARCHER ENGINE

After programming the position and the size of the search window, the searcher engine finds the largest multipath peak within the search parameter set. The MSM2300 searcher engine can operate at rates up to eight times faster than the searcher provided in the MSM2.2, allowing for faster acquisition and neighbor list search intervals. The MSM2300 searcher engine reports the best four local maxima peaks per search window, reducing microprocessor overhead. Also, the MSM2300 searcher reports the position of the multipath peaks with a higher resolution, allowing greater precision than the searcher provided in the MSM2.2.

DEMODULATING FINGERS

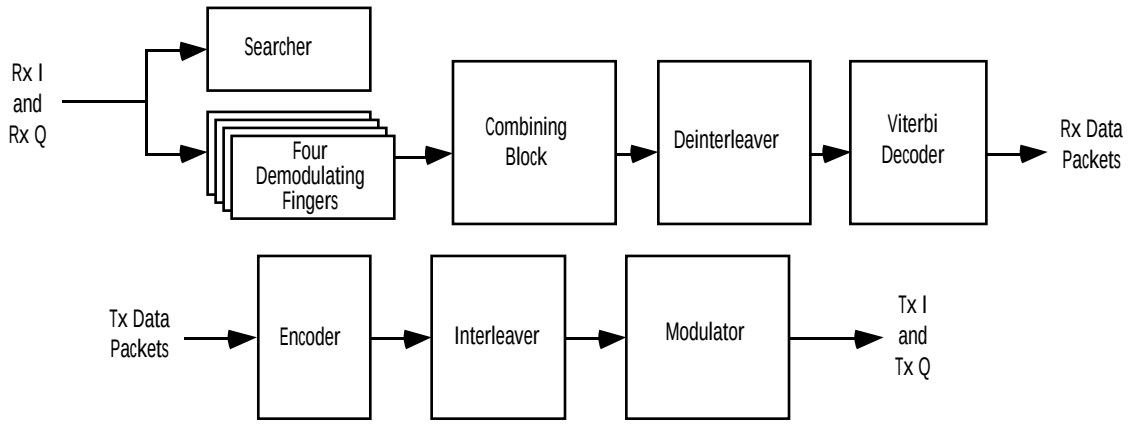
The MSM2300 contains four identical demodulating fingers. Each demodulating finger performs the following on its assigned signal path:

- Quadrature despreading
- Walsh uncovering
- Frequency tracking
- Time tracking

The MSM2300's four demodulating fingers provide better multipath reception than the fingers provided in the MSM2.2.

The MSM2300 pilot, RSSI and time tracking loop filters have enhanced bandwidth programmability over the fingers provided in the MSM2.2. The time tracking capability of each MSM2300 demodulating finger has been enhanced. A Finger Disable Mode has been added

Figure 5. CDMA Digital Baseband Processor Block Diagram



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to each MSM2300 demodulating finger to decrease power when the demodulating finger is not in use.

COMBINING BLOCK

The combining block is made up of three functional blocks:

- Symbol combiner
- Carrier frequency error combiner
- Power combiner

The symbol combiner combines the modulation symbols received by each of the demodulating fingers, performs long code PN despreading, creates mobile station timing references and compensates for oscillator drift. The carrier frequency error combiner combines and processes the frequency error information provided by each of the four demodulation fingers. The power combiner processes the power control bits demodulated by each finger, and sends a power control decision to the closed-loop AGC circuit.

The MSM2300 combining block has been enhanced over the MSM2.2, adding programming flexibility.

DEINTERLEAVER AND VITERBI DECODER

The deinterleaver is used to reverse the interleaving performed by the base station. Interleaving provides protection against burst errors and fades.

The MSM2300 uses an enhanced Viterbi decoder resulting in a 0.5 - 0.7 dB improvement in 14.4 kbps rateset operation, as compared with the MSM2.2. The Viterbi decoder optimally decodes the convolutional coding from the base station. The Viterbi decoder operates by finding the most likely path through the encoder trellis that produced the transmitted symbol stream. In this way, many modulation symbols that have been corrupted by noise can be recovered. Quality bits and Cyclic Redundancy Code (CRC) bits are used to verify the quality of the decoded data.

CONVOLUTIONAL ENCODER AND INTERLEAVER

The encoder convolutionally encodes reverse link data frames. The convolutional encoder block automatically inserts CRC bits for the reverse link frames.

The interleaver “scrambles” the reverse link data to protect the data against transmission fades and burst errors. The reverse link data is unscrambled by the base station’s deinterleaver.

MODULATOR

The modulator performs the orthogonal modulation, long code PN spreading and quadrature spreading. The resulting data stream is then bandlimited with FIR filters and sent to the BBA2. The MSM2300 modulator is enhanced to use less power than the modulator provided in the MSM2.2.

DIGITAL FM PROCESSOR

The MSM2300 also supports Advanced Mobile Phone System (AMPS) cellular operations. The DFM processor performs digital signal processing operations for the subscriber unit using the AMPS cellular standard, IS-95A.

DFM processing is distributed in the MSM2300 and involves not just audio signals, but also Wideband Data (WBD), SAT transpond and DTMF tone pairs. The microprocessor also processes WBD, SAT and DTMF signals. Figure 6 shows the DFM signal processing blocks and the DFM signal flow from CODEC through the MSM2300 and to the BBA2. The DFM subsystem and the vocoder (in DFM Mode) perform separate but distinct processes on Rx and Tx DFM data.

The vocoder performs several functions for DFM. The vocoder interpolates incoming Tx PCM from the CODEC to a higher sample rate for the DFM subsystem. The vocoder’s Tx path also includes a SAT transponder, DTMF generation circuits, the VOX and the pre-emphasis filter.

In the Rx signal path, the vocoder decimates the incoming Rx data from the DFM subsystem to outgoing Rx PCM data for the CODEC. The vocoder’s Rx path also has SAT and DTMF detection circuits, VOX and a de-emphasis filter.

The DFM subsystem performs voice and WBD operations for both Rx and Tx signals. The DFM subsystem’s Tx path accepts voice data from the vocoder and interpolates it to a higher outgoing rate for the BBA2. The DFM subsystem’s Rx path accepts I/Q components from the BBA2 and decimates it to a lower

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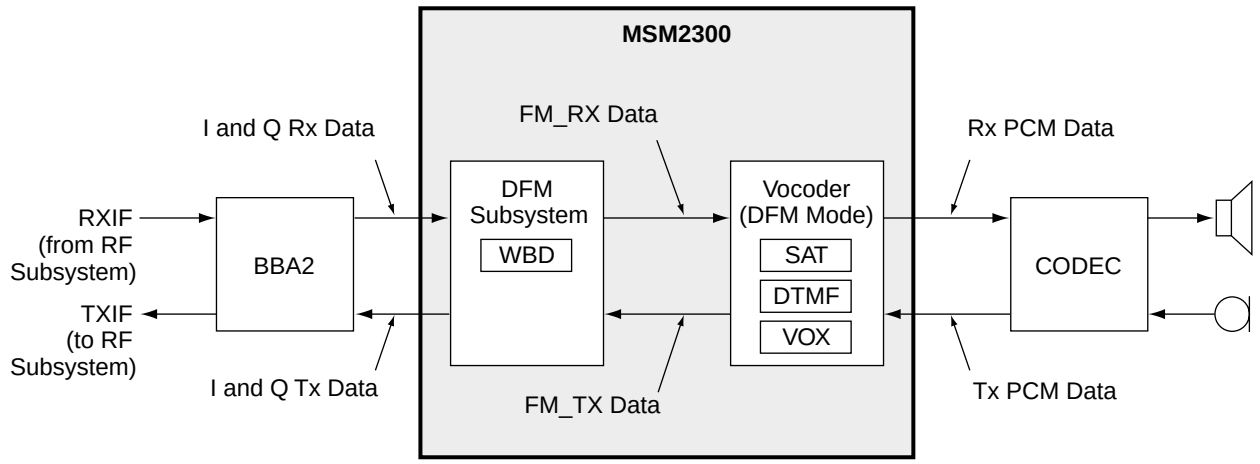
Figure 6. DFM Signal Flow from CODEC to BBA2



outgoing rate for the vocoder. Voice data processing is done independent from the microprocessor.

'186 MICROPROCESSOR AND PERIPHERALS

The MSM2300 contains an embedded Intel® 80C186EC microprocessor and supporting peripherals, including some QUALCOMM-specific circuits such as the QUALCOMM Peripheral Control Unit (QPCU). The QPCU includes:

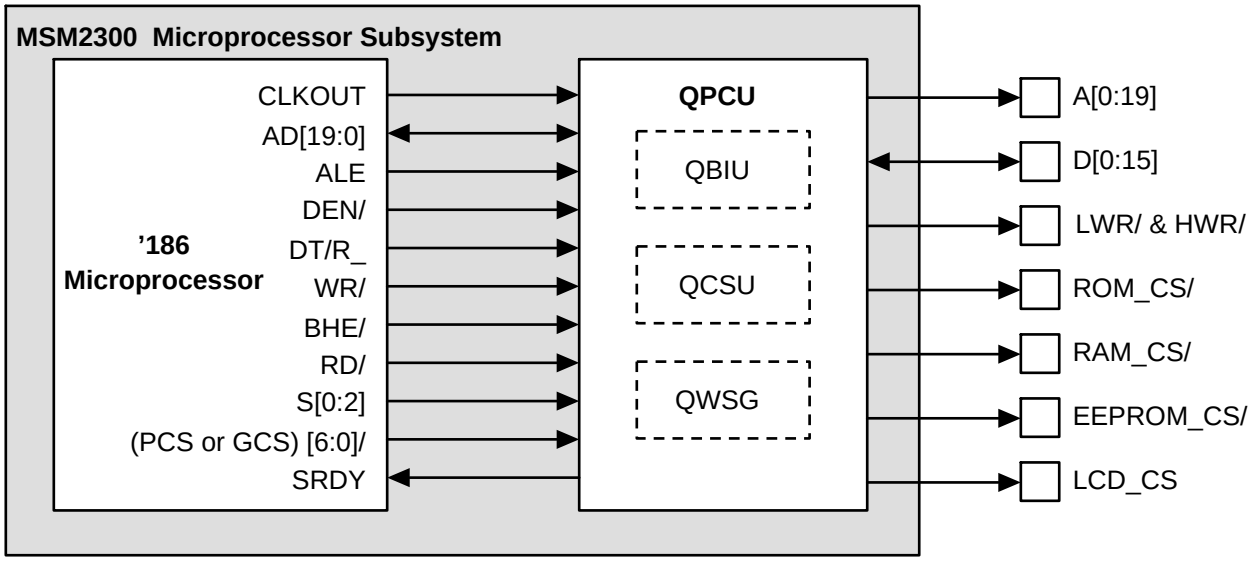
- A QUALCOMM Bus Interface Unit (QBIU)
- A QUALCOMM Chip Select Unit (QCSU)
- A QUALCOMM Wait State Generator (QWSG)

Other related peripherals include the Interrupt Subsystem, Watchdog Timer and Universal Asynchronous Receiver Transmitter (UART). These peripherals (shown in Figure 7) extend the functionality of the MSM2300. The Interrupt Subsystem includes:

- MSM2300 Interrupt Controller
- Microprocessor internal interrupt controller

The MSM2300 Interrupt Controller handles interrupt from various subsystems, then performs a Bitwise OR to pass the interrupts onto the microprocessor's internal interrupt controller. The Interrupt Subsystem frees the microprocessor from such time-consuming operations as polling. Each interrupt has its own status flag and mask for enabling/disabling. Several levels of

Figure 7. MSM2300 Microprocessor Block Diagram



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interrupt masking are available along the path from the originating source through the microprocessor's internal interrupt controller.

The Watchdog Timer ensures that the subscriber unit resets and re-initiates when it encounters either hardware or software anomalies.

The UART is a serial communication link to external systems for test and debug of the subscriber unit. The UART operates at rates up to 115.2 kbps and includes receive and transmit FIFOs, hardware handshaking and programmable data sizes. The UART's Rx and Tx FIFO sizes are double the FIFO sizes of the MSM2.2. The internal 80C186EC serial port is available for use when using the MSM2300.

The 80C186EC microprocessor and peripheral system features 1 Mbyte of address space, 64 kbyte I/O space, interrupt and DMA controllers and a timer/counter.

The MSM2300 microprocessor interface has been enhanced over the MSM2.2 to reduce power consumption.

SUPPORTING INTERFACES

Several interfaces in the MSM2300 support other devices within the subscriber unit and provide connections to external peripheral components. These interfaces support board testing and other subscriber unit operations. A brief description of each of these interfaces is given below:

1. BBA2-shrink Interface
   The interface that the MSM2300 and the BBA2-shrink share includes a CDMA/FM transmit I and Q channel data bus, separate CDMA/FM receive data busses and an interface to the General-Purpose ADC on the BBA2. The MSM2300 also receives the BBA2 CHIPX8 and TCXO/4 clock signals.
2. External CODEC Interface
   The external CODEC interface consists of both primary and auxiliary interfaces. The primary interface is normally used as the main CODEC interface. The auxiliary interface may be used for hands-free mobile operation.
3. GPIO Interface
   The General Purpose Input/Output Interface includes 31 I/O connections and five interrupts. The GPIO interface supports communications between the internal microprocessor and external peripherals.
4. Mode Select Interface
   The Mode Select Interface supplies three inputs (MSM2300-176) or four inputs (MSM2300-208) allowing the user to change the MSM2300 operating state between MICE Mode (208-pin devices only), NATIVE Mode and High Impedance (HI-Z) Mode.
5. Keypad Interface
   The Keypad Interface allows a connection to an external keypad.
6. Ringer Interface
   The Ringer Interface may be programmed to generate a single-tone or DTMF output.
7. M/N Counter Interface
   The M/N Counter Interface produces a programmable frequency, programmable duty-cycle counter that can be used to switch a supplemental switcher power supply or make a tone.
8. UART Interface
   The UART Interface is a serial communication link that can be used to test, debug or upgrade the subscriber unit's functions.
9. JTAG Interface
   The MSM2300 complies with ANSI/IEEE 1149.1-1990, the Joint Test Action Group (JTAG) interface. The JTAG Interface may be used to test digital interconnects within the subscriber unit during manufacture.

INPUT / OUTPUT SIGNALS

Figure 8 shows the functions provided by the MSM2300's pins, and the relative sizes of the 176-pin TQFP and the 196-ball PBGA package options. Table 1 provides descriptions of the pin functions.

Figure 8. MSM2300 176-pin and 196-ball Functional Diagram

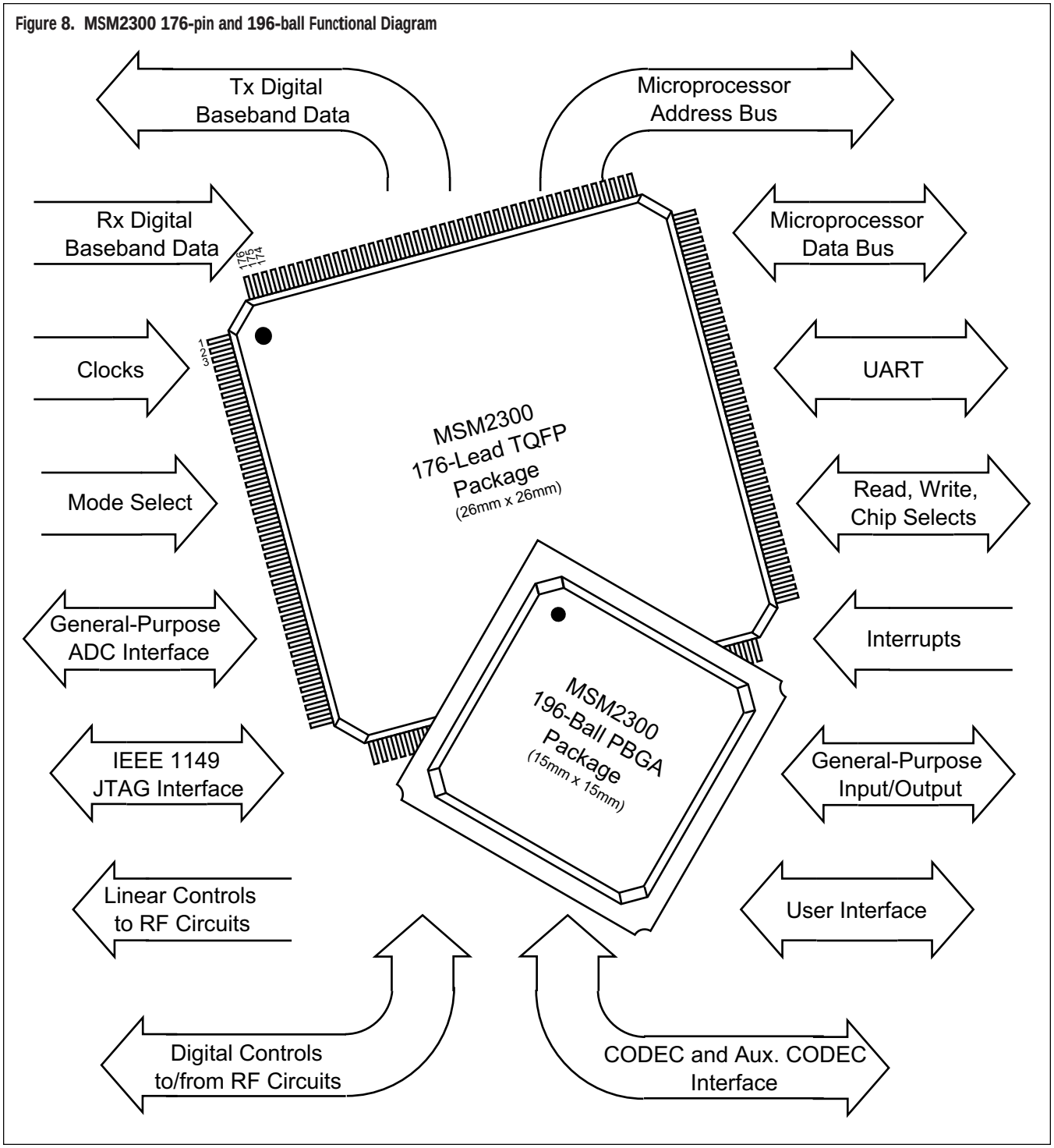

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Table 1. MSM2300 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Microprocessor Address Bus	The internal 80C186EC microprocessor interfaces to standard peripheral devices such as RAM, ROM and EEPROM.
Microprocessor Data Bus	
Read, Write, Chip Selects, Interrupts	
General-Purpose Input/Output	The MSM2300 offers 30 GPIO for user-definable features.
UART	A UART is available for external access to subscriber unit RAM and ROM, manufacturing test convenience.
User Interface	The User Interface of the MSM2300 includes signals to and from the keypad, ringer and LCD display of the subscriber unit.
CODEC and Aux. CODEC Interface	The MSM2300 can directly interface with several industry-standard CODECs. The MSM2300 offers two CODEC interfaces for microphone/earpiece interfacing in the subscriber unit.
Digital Controls to/from RF Circuits	Digital control signals are available from the MSM2300 for controlling the LNA and PA in the RF subsystem.
Linear Controls to/from RF Circuits	The MSM2300 controls the gain of the receive and transmit AGC amplifiers, receive and transmit signal path offsets in the BBA2 chip, the gain of the system LNA and the fine tuning of the system master frequency reference by way of Pulse Density Modulated signals. A single-pole RC low-pass filter is used to convert the pulse streams to DC control voltages.
IEEE 1149 JTAG Interface	A full JTAG interface conforming with the IEEE 1149 standard is available for test and debug of subscriber unit subassemblies.
General Purpose ADC Interface	The MSM2300 interfaces with the general-purpose ADC on the BBA2 chip. This ADC is generally used for monitoring the battery voltage, RF power output level or temperature of the subscriber unit.
Mode Select	The MSM2300 may be operated in several modes including NATIVE (normal operation), MICE (for in-circuit emulation of the 80C186EC microprocessor) or MOUSE (using an external microprocessor).
Clocks	The MSM2300 operates with three fundamental clocks: CHIPX8 runs at 9.8304 MHz and is supplied by the BBA2 chip, TCXO/4 is a 7.92 MHz clock supplied by the BBA2 and the microprocessor clock which is input on the XTAL_IN pin.
Rx Digital Baseband Data	The BBA2 chip converts the Receive IF signal from the RF subsystem of the subscriber unit to digital baseband data for both CDMA and AMPS operating modes of the MSM2300.
Tx Digital Baseband Data	The MSM2300 generates transmit digital baseband data for the BBA2 chip. The BBA2 chip converts that digital data to an analong IF frequency of the subscriber unit.

TECHNICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2 shows the absolute maximum ratings, and Table 3 shows the recommended operating conditions of the MSM2300. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_S	Storage Temperature	-65	+150	°C
T_J	Junction Temperature	–	+150	°C
V_I	Voltage on any INPUT or OUTPUT Pin	-0.5	V_{DD} + 0.5	V
V_{DD}	Supply Voltage	-0.3	+4.6	V
I_{IN}	Latch-up Current	–	±150	mA
V_{ESD}	Electrostatic Discharge Voltage (HBM MIL 883 301S)	–	±2000	V

Table 3. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}	Supply Voltage	2.7	3.6	V
T_A	Operating Temperature (176-pin and 196-ball package)	-40	+85	°C
	Operating Temperature (208-pin package)	0	+70	°C

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DC ELECTRICAL CHARACTERISTICS

Table 4 shows the DC electrical characteristics for the MSM2300.

Table 4. DC Electrical Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
V_{IH}	High-level Input Voltage, CMOS/Schmitt	0.65 V_{DD}	V_{DD} + 0.3	V	–
V_{IL}	Low-level Input Voltage, CMOS/Schmitt	-0.3	0.35 V_{DD}	V	–
I_{IH}	Input High Leakage Current	–	2	µA	1
I_{IL}	Input Low Leakage Current	-2	–	µA	2
I_{IHPD}	Input High Leakage Current with Pull Down	10	60	µA	1, 3
I_{ILPU}	Input Low Leakage Current with Pull Up	-60	-10	µA	2, 3
I_{OZH}	High-level Three-State Leakage Current	–	2	µA	1
I_{OZL}	Low-level Three-State Leakage Current	-2	–	µA	2
I_{OZHPD}	High-level Three-State Leakage Current with Pull Down	10	60	µA	1, 3
I_{OZLPU}	Low-level Three-State Leakage Current with Pull Up	-60	-10	µA	2, 3
I_{OZHKP}	High-level Three-State Leakage Current with Keeper	-25	-3	µA	1, 3
I_{OZLKP}	Low-level Three-State Leakage Current with Keeper	3	25	µA	2, 3
I_{OS}	Output Short-Circuit Current	-300	300	µA	–
V_{OH}	High-level Output Voltage, CMOS/Schmitt	V_{DD} - 0.45	V_{DD}	V	4
V_{OL}	Low-level Output Voltage, CMOS/Schmitt	0.0	0.45	V	4
C_{IN}	Input Capacitance	–	15	pF	–

Notes:

1. Pin voltage = V_{DD} Max. For keeper pins, pin voltage = V_{DD} Max - 0.45 Volts.
2. Pin voltage = V_{SS} and V_{DD} = V_{DD} Max. For keeper pins, pin voltage = 0.45 Volts and V_{DD} = V_{DD} Max.
3. Refer to Tables 3.1 in User Manual for which pins have pull ups, pull downs and keepers.
4. Refer to Tables 3.1 in User Maunual for I_{OH} and I_{OL} current capacity for output pins (at V_{DD} = V_{DD} Min).

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POWER CONSUMPTION

These values are an estimation of maximum operating currents for a nominal V_{DD} = 3.3 V. This information should be used as a general guideline for system design.

CDMA Modes assume that the subscriber unit is operating in compliance with the CDMA specifications of IS-95-A. FM Modes assume that the subscriber unit is operating in compliance with the AMPS specifications of IS-95-A. Estimates for maximum power supply current are under the following conditions: V_{DD} = 3.3 V and T_A = 25°C. Table 5 shows the power supply currents for MSM2300 operating modes. As this is a single-chip design, the power supply current values include microprocessor, DSP and CDMA functional blocks.

Table 5. Power Supply Currents for MSM2300 Operating Modes

SYMBOL	MODE	TYPICAL	UNITS
I_{DD1}	CDMA Rx/Tx (active full-duplex operation)*	65 – 80	mA
I_{DD2}	CDMA Rx (idle: CDMA Rx + processor + some "buffering" active; all else shut down)	40	mA
I_{DD3}	CDMA Sleep (CDMA + processor in Standby Mode; some "buffering" active)	1.25	mA
I_{DD4}	FM Rx/Tx (active full-duplex operation)	35	mA
I_{DD5}	FM Rx (idle: receive channel active, transmit channel "off")	7.5	mA

Notes:

* All of the above currents are highly software dependent. They also depend upon vocoding rate, microprocessor clock frequency and digital I/O load characteristics.

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MSM2300 PACKAGING

The MSM2300 is offered in 176-pin TQFP, 196-ball PBGA and 208-pin PQFP (pre-production use only) packages.

The 176-pin TQFP and 196-ball PBGA packages are designed for production release phones. Figure 9 provides the basic package dimensions for the 176-pin TQFP package. Figure 10 provides the basic package dimensions for the 196-ball PBGA package.

Figure 9. MSM2300 176-pin TQFP Package Dimensions

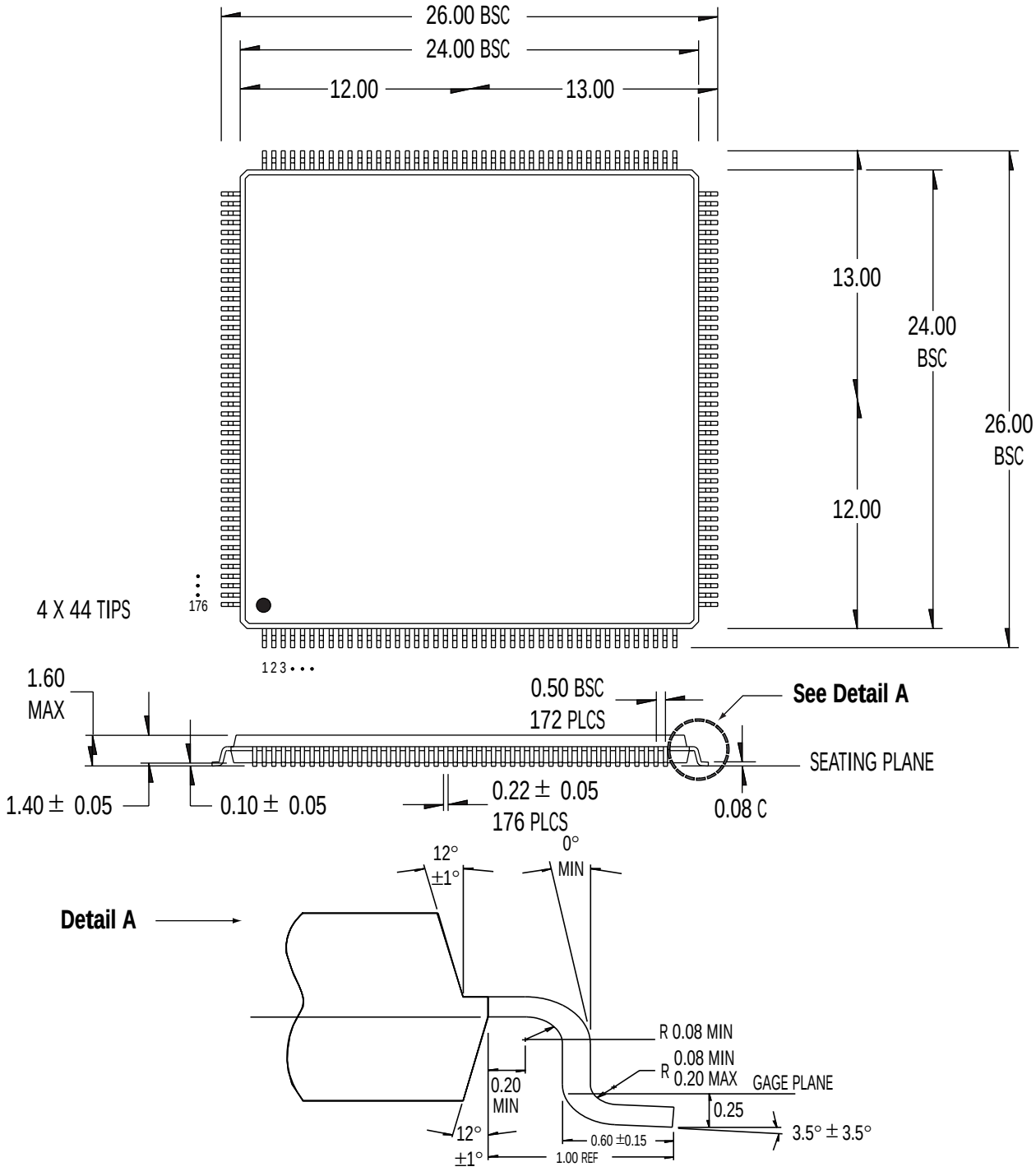

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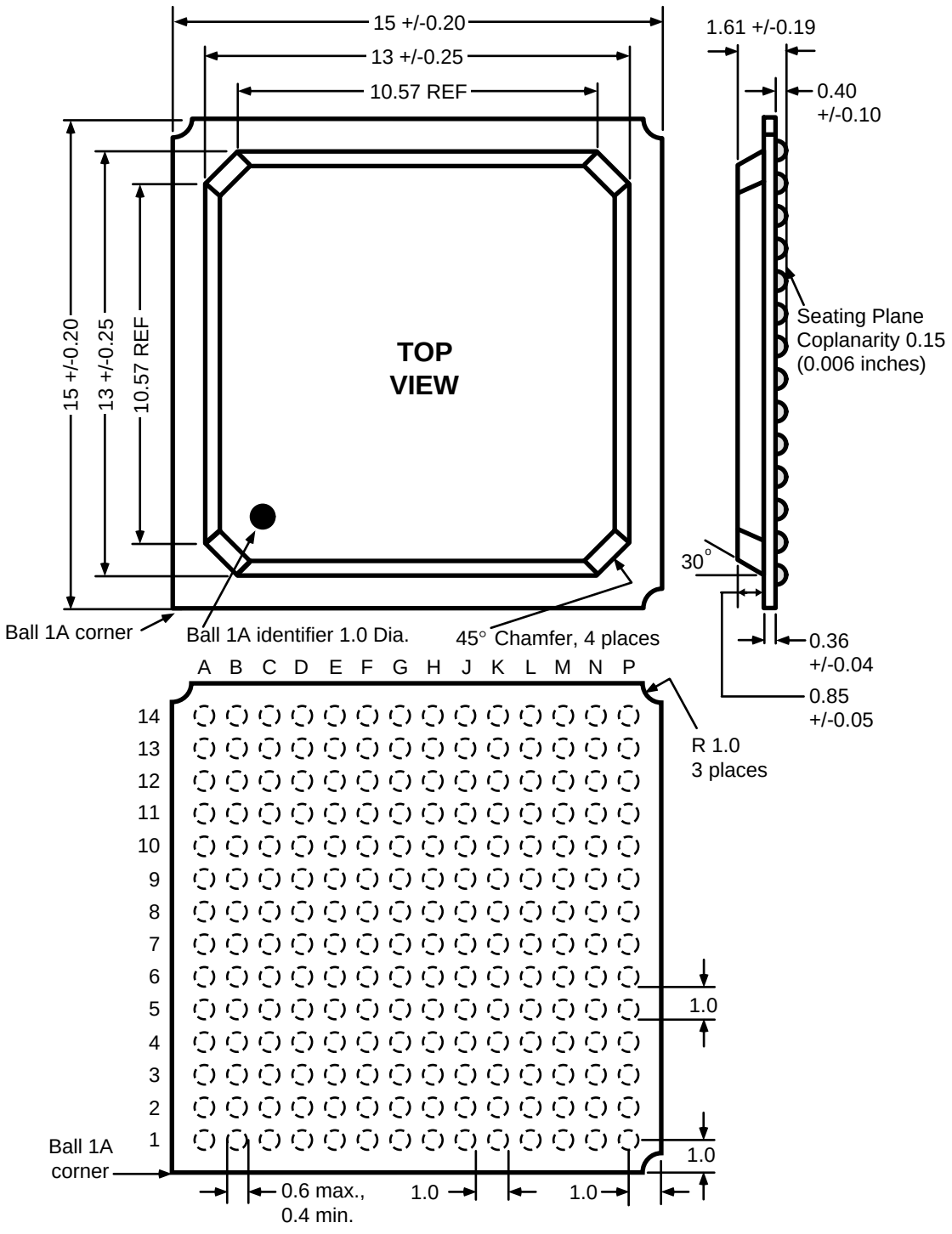
Figure 10. MSM2300 196-ball PBGA Package Dimensions



Solderball Material is 63% Sn / 37% Pb

TOP VIEW
(Ball Pattern and Location)
(All dimensions in mm)

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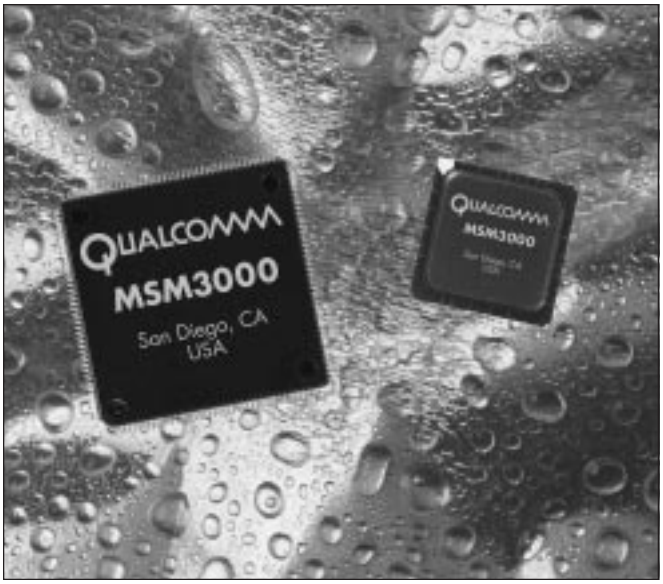
MSM3000

MOBILE STATION MODEM

PRELIMINARY SPECIFICATIONS



OVERVIEW

The dual-mode code-division multiple-access advanced mobile phone system (CDMA/AMPS) cellular telephone is a complex consumer communications instrument that relies heavily upon digital signal processing. To simplify the design and reduce the production cost of the subscriber unit, QUALCOMM has developed a Mobile Station Modem (MSM3000), and Transmit and Receive IF Converters (IFT3000/ IFR3000). These devices perform all of the signal processing in the subscriber unit, from IF to audio.

The QUALCOMM MSM3000 is a 5th-generation device. The MSM3000 integrates functions that support a dual-mode CDMA/FM subscriber unit. Subsystems within the MSM3000 include a CDMA processor, a Digital FM (DFM) processor, a QUALCOMM designed DSP for voice compression, an ARM® ARM7TDMI microprocessor and several peripheral interfaces that are used to support other functions. The MSM3000 consumes less power and provides more flexibility than QUALCOMM's MSM2300. The MSM3000 is compatible with QUALCOMM's Q5312 Analog Baseband Processor (BBA2) along with the Q5500 IF Receive AGC Amplifier and Q5000 IF Transmit AGC Amplifier, or with the IFR3000 and IFT3000 IF to Baseband Converters. Figure 1 shows a diagram of the MSM3000 used in a typical subscriber unit along with QUALCOMM's IFR3000 and IFT3000. Figure 2 shows the size of previous MSM, BBA and AGC combinations compared to using MSM3000 along with IFR3000 and IFT3000.

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Figure 1. The MSM3000 in a Subscriber Unit

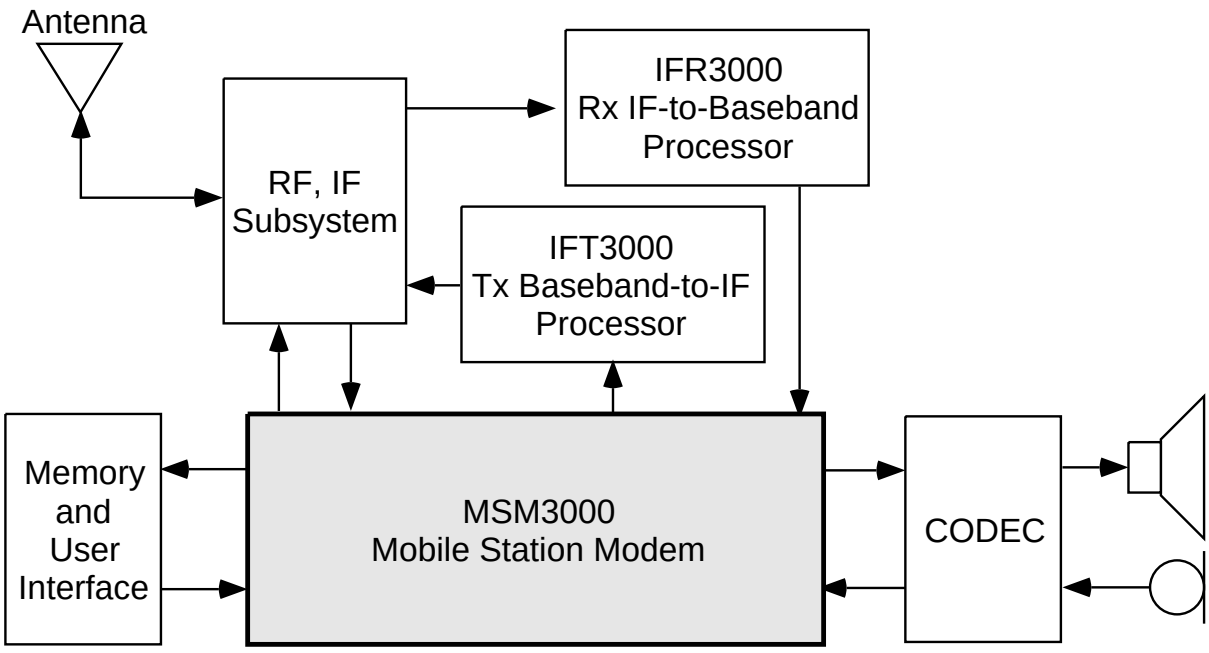
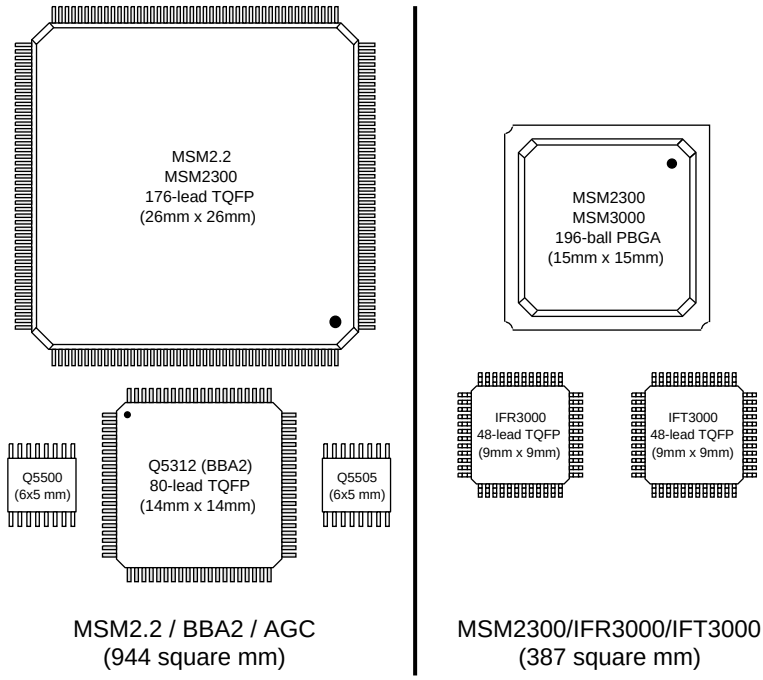


Figure 2. Package Area Comparison



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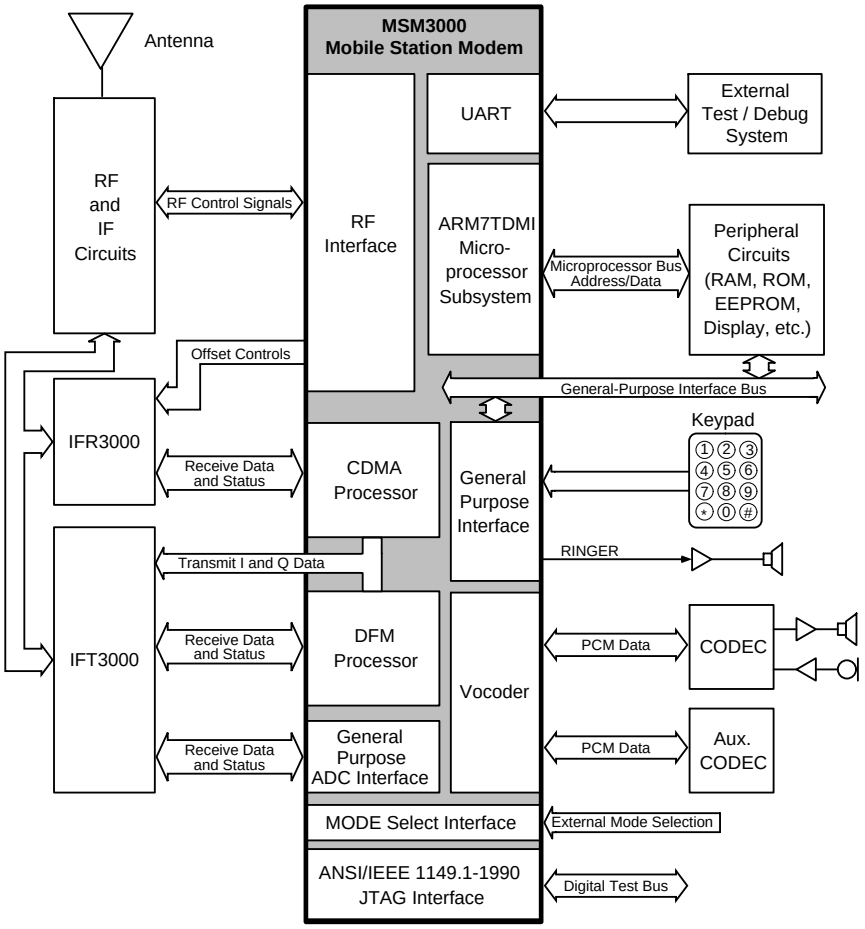
The MSM3000 demodulates Rx digital baseband data from the IFR3000 (or Q5312 BBA2). The IFR3000 converts the modulated IF signal from the RF section of the subscriber unit into digital baseband data. For transmission, the MSM3000 modulates and sends digital baseband data to the IFT3000. The Tx signal path of the IFT3000 converts Tx digital baseband data into modulated IF. The MSM3000 communicates with the external RF and analog baseband circuitry of the subscriber unit to control signal gain in the RF Rx and Tx signal paths, reduce baseband offset errors and tune the system frequency reference.

The MSM3000 performs baseband digital signal processing and executes the subscriber unit system software. It is the central interface device in the subscriber unit, connecting RF, baseband and audio circuits, as well as memory and user interface features. The user interface of the subscriber unit typically includes the keypad, LCD display, ringer, microphone and earpiece. These are either under the direct or indirect control of the MSM3000. The MSM3000 also contains complete digital modulation and demodulation systems for both CDMA and AMPS cellular standards, as specified in IS-95A.

The subscriber unit system software controls most of the functionality and activates the features of the subscriber unit. System software is executed by an embedded ARM microprocessor within the MSM3000.

The CODEC interfaces directly with the microphone and earpiece, converting analog audio signals from the microphone into digital signals for the Vocoder. The CODEC also converts digital audio data from the Vocoder into analog audio for the earpiece. The MSM3000 supports an auxiliary external Pulse Coded Modulation (PCM) interface. The auxiliary CODEC is optional within the subscriber unit. Figure 3 shows an MSM3000 Functional Block Diagram that describes these interfaces.

Figure 3. MSM3000 Functional Block Diagram



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MSM3000 FEATURES

MSM3000 GENERAL FEATURES

- Supports IS-95A compliant CDMA and AMPS functionality
- Low 2.7 to 3.3 V DC power supply voltage operation
- DFM subsystem for AMPS operation (with IFR3000/IFT3000)
- Supports Phase 1 High Data Rate (HDR) of 76.8 kbps for Rate Set 1, and 86.4 kbps for Rate Set 2
- Software-controlled power management features
- Advanced submicron CMOS design
- 176-pin TQFP and 196-ball PBGA packages
- ANSI/IEEE 1149.1A Testability

MSM3000 AUDIO PROCESSING FEATURES

- 8 kbps vocoder
- 13 kbps vocoder
- EVRC
- Optional independent external vocoder clock source
- Interface for an external, user-supplied vocoder
- Dual-Tone Multiple-Frequency (DTMF) generation
- Programmable digital filters for audio signal path compensation in both CDMA and AMPS Modes
- Supervisory Audio Tone (SAT) transponding in FM Mode
- DTMF detection (CDMA Mode only)
- Earseal Echo Cancellation (ESEC) (CDMA mode only)
- Voice Operated Switch (VOX)
- Voice Recognition

MSM3000 MICROPROCESSOR SUBSYSTEM FEATURES

- Embedded industry-standard ARM7TDMI microprocessor
- Watchdog and sleep timers
- Interrupt controller with support for both internal and off-chip interrupt driven devices
- In-phone debug capability through the JTAG interface
- Chip select circuitry with direct support for RAM, ROM/FLASH, EEPROM, an LCD display and two other devices
- Programmable wait state generator
- Designed to operate with up to 20 MHz microprocessor clock frequency

MSM3000 SUPPORTED INTERFACE FEATURES

- Interfaces for up to two external m-Law, A-Law, or linear CODECS from various manufacturers
- Bi-directional serial data port with 64-byte Rx and 64-byte Tx FIFO buffers and hardware handshaking
- Serial Bus Interface for control of IFR3000 and IFT3000 IF/Baseband Converters
- More than 30 general purpose I/O pins (several with interrupt capability)
- External keypad interface
- Support for up to 8 MBytes of external RAM and 8 MBytes of external ROM or 1 MByte of EEPROM
- Support for either 8-bit or 16-bit external RAM
- Three spare Pulse Density Modulated (PDM) outputs for user-defined analog control
- General purpose programmable M/N counter output
- Programmable ringer output

MSM3000 ENHANCEMENTS OVER MSM2300 / MSM2310

The MSM3000 has several design enhancements which reduce the power consumption and provide more features than the MSM2300/MSM2310. The Q186 microprocessor in the MSM2300/MSM2310 is replaced by the ARM7TDMI microprocessor in the MSM3000. The advantages of ARM7TDMI include:

- 4 Gbytes of memory space
- Increased performance with a RISC architecture and 3-stage pipelining.
- High code density with 32-bit ARM and 16-bit THUMB™ instruction set.
- State-of-the-art software tool suite
- Reduced power dissipation
- In-phone debug capabilities
- Improved SLEEP controller for significant standby power reduction

The MSM3000 also includes the following enhancements:

- EVRC
- DFM Slotting improves standby time and reduces overall power consumption during DFM Mode
- Phase 1 High Data Rate (HDR) support
  - 8 co-channel demod Rate Set 1: 76.8 kbps
  - 6 co-channel demod Rate Set 2: 86.4 kbps
- Improved AGC control, allowing the use of High Efficiency Power Amplifiers
- Hardware enhancements improve standby time in CDMA Mode
- Serial Bus Interface Master Controller, a 3-pin serial interface to the IFR3000 and IFT3000, and other RF and IF circuits
- Reduced die size and reduced overall power consumption, compared to the MSM2300
- Voice Recognition
  - Speaker Dependent, Speaker Independent and Voice prompt support
  - Multiple languages supported
- Supports low power, low frequency crystal to enable TCXO shutoff

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INPUT / OUTPUT SIGNALS

Figure 4 shows the functions provided by the MSM3000's pins, and the relative sizes of the 176-pin TQFP and the 196-ball PBGA package options. Table 1 provides descriptions of the pin functions.

Figure 4. MSM3000 176-pin and 196-ball Functional Diagram

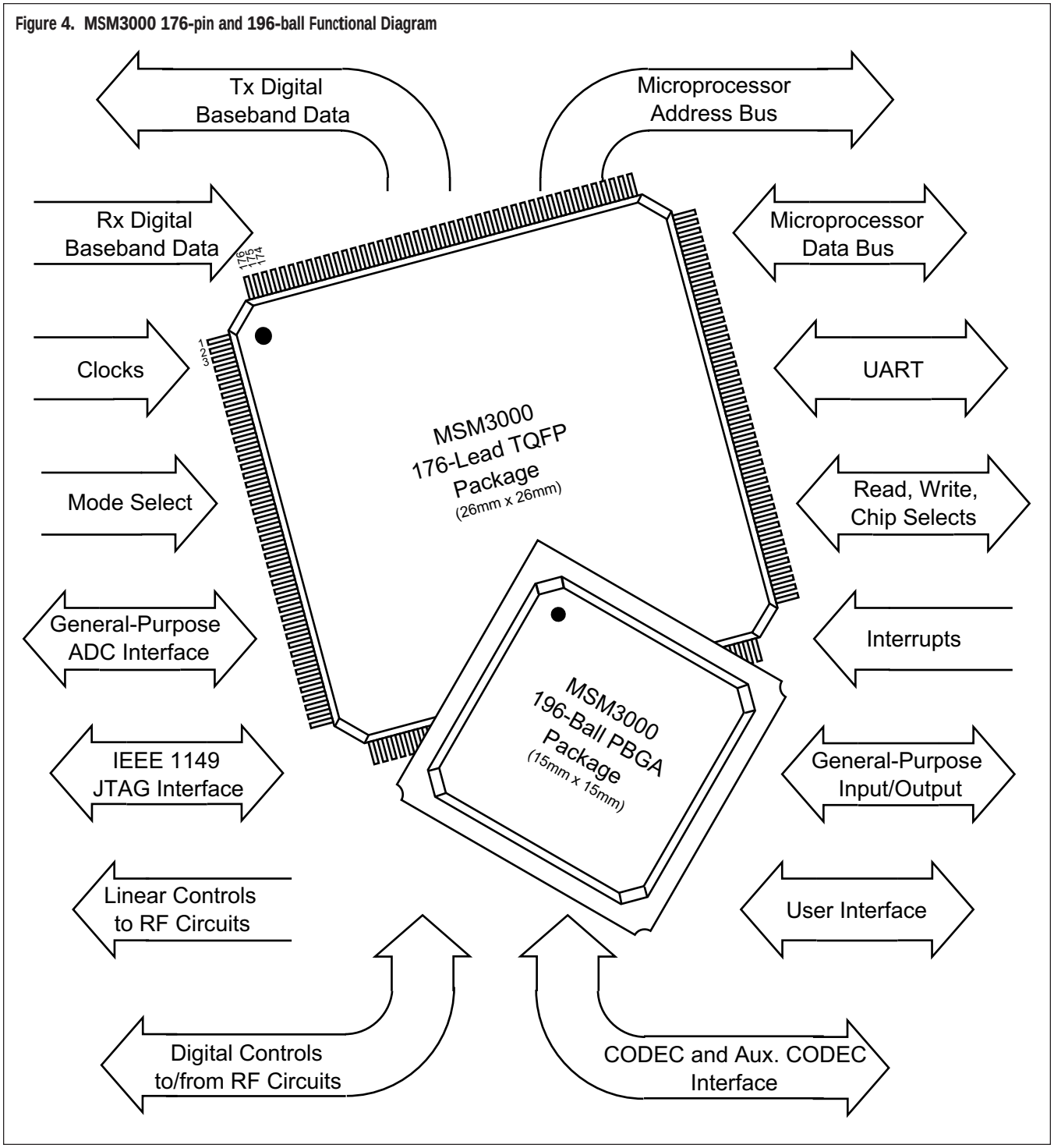

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Table 1. MSM3000 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Microprocessor Address Bus	The internal ARM7TDMI microprocessor interfaces to standard peripheral devices such as RAM, ROM and EEPROM.
Microprocessor Data Bus	
Read, Write, Chip Selects, Interrupts	
General-Purpose Input/Output	The MSM3000 offers 30 General-Purpose Input/Output pins (GPIO) for user-definable features.
UART	A UART is available for external access to subscriber unit RAM and ROM, manufacturing test convenience.
User Interface	The User Interface of the MSM3000 includes signals to and from the keypad, ringer and LCD display of the subscriber unit.
CODEC and Aux. CODEC Interface	The MSM3000 can directly interface with several industry-standard CODECs. The MSM3000 offers two CODEC interfaces for microphone/earpiece interfacing in the subscriber unit.
Digital Controls to/from RF Circuits	Digital control signals are available from the MSM3000 for controlling the LNA and power amplifier in the RF subsystem.
Linear Controls to/from RF Circuits	The MSM3000 controls the gain of the receive and transmit AGC amplifiers, receive and transmit signal path offsets in the Baseband Processors, the gain of the system LNA and the fine tuning of the system master frequency reference by way of Pulse Density Modulated signals. A single-pole RC low-pass filter is used to convert the pulse streams to DC control voltages.
IEEE 1149 JTAG Interface	A full JTAG interface conforming with the IEEE 1149 standard is available for test and debug of subscriber unit subassemblies.
General Purpose ADC Interface	The MSM3000 interfaces with the general-purpose ADC on the Baseband Processor. This ADC is generally used for monitoring the battery voltage, RF power output level or temperature of the subscriber unit.
Mode Select	The MSM3000 may be operated in several modes including NATIVE (normal operation), MICE (for in-circuit emulation of the ARM microprocessor) or MOUSE (using an external microprocessor).
Clocks	The MSM3000 operates with three fundamental clocks: CHIPX8 runs at 9.8304 MHz and is supplied by the BBA2 chip, TCXO/4 is a 7.92 MHz clock supplied by the Baseband Processor and the microprocessor clock which is input on the XTAL_IN pin.
Rx Digital Baseband Data	The Baseband Processor converts the Receive IF signal from the RF subsystem of the Subscriber Unit to digital baseband data for both CDMA and AMPS operating modes of the MSM3000.
Tx Digital Baseband Data	The MSM3000 generates transmit digital baseband data for the Baseband Processor. The Baseband Processor converts that digital data to an analong IF frequency of the subscriber unit.

MSM3000 PACKAGING

The MSM3000 is available in a 196-ball Plastic Ball Grid Array (PBGA) package, with a 15 mm X 15 mm footprint for very dense subscriber unit applications. It is also available in a 176-pin Thin Quad Flat Pack (TQFP) package.

The MSM3000 is fabricated in an advanced submicron CMOS process. The device operates between 2.7 and 3.3 V for low power consumption and long talk time. As the subscriber changes modes, the MSM3000 powers down unused circuits to keep power consumption to a minimum.

Figure 6 provides the basic package dimensions for the 176-pin TQFP package. Figure 7 provides the basic package dimensions for the 196-ball PBGA package.

Figure 5. MSM3000 176-pin TQFP Package Dimensions

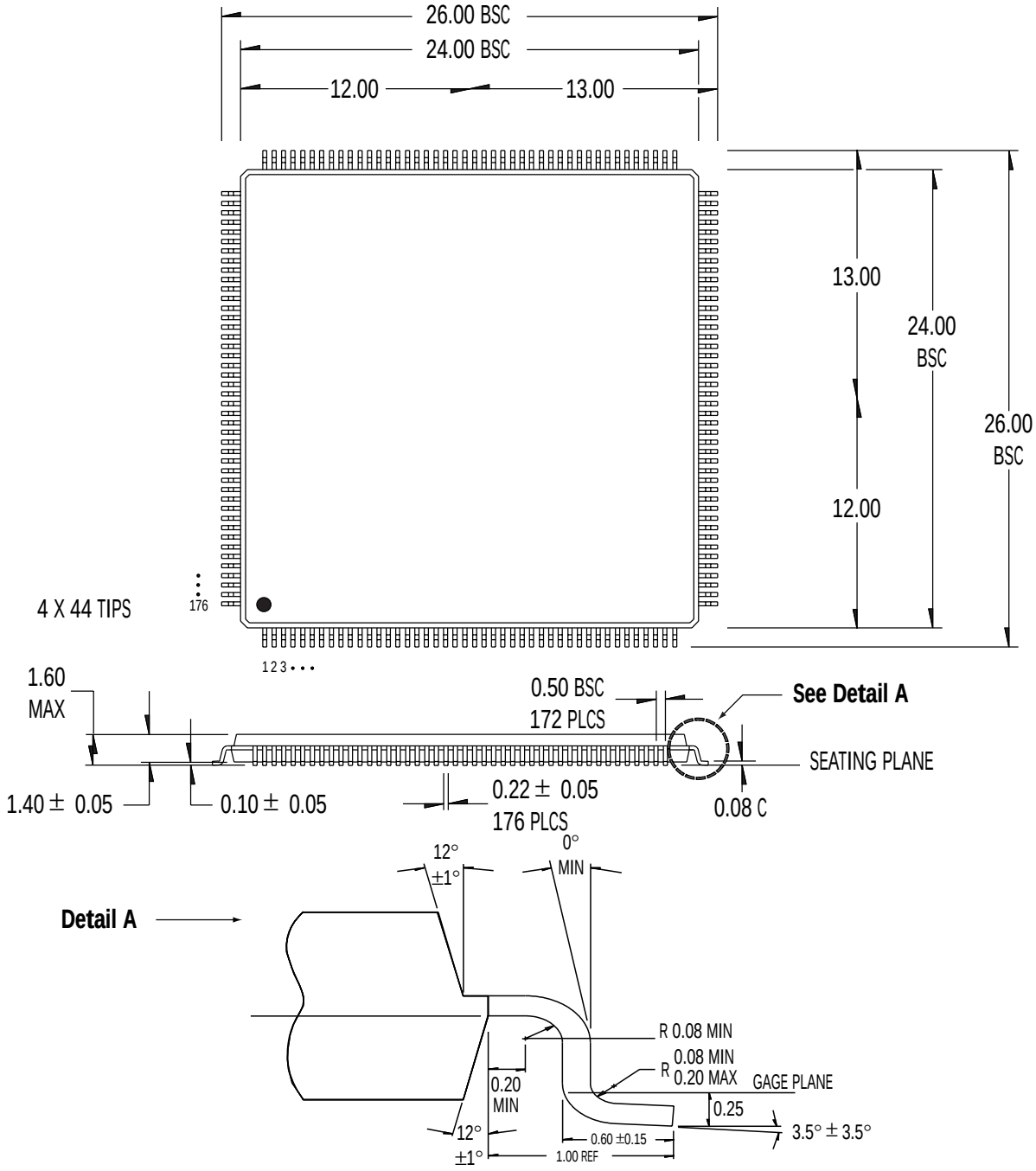

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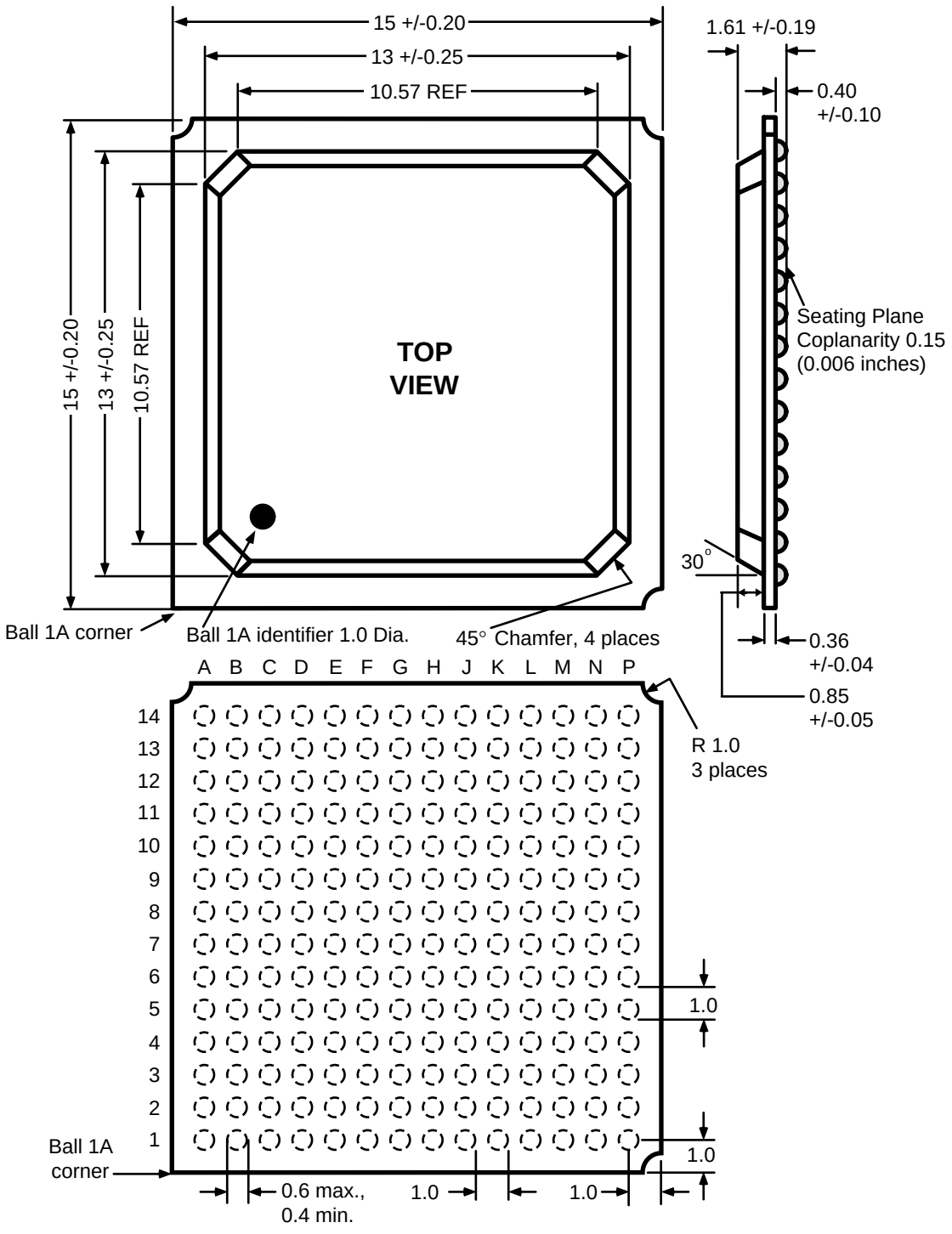
Figure 6. MSM3000 196-ball PBGA Package Dimensions



Solderball Material is 63% Sn / 37% Pb

TOP VIEW
(Ball Pattern and Location)
(All dimensions in mm)

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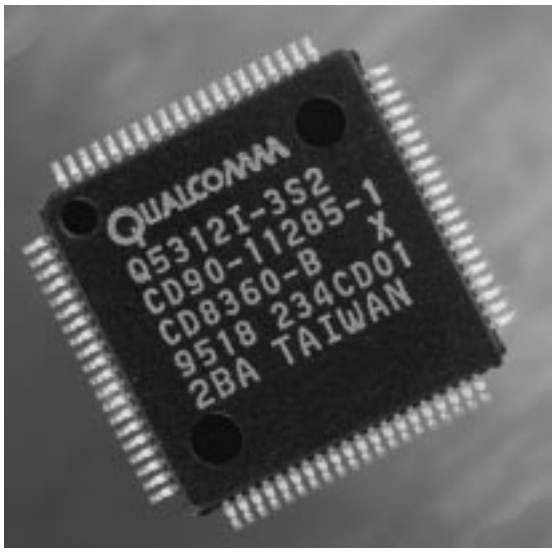
Q5312I-3S2

BBA2-SHRINK

Q5312I-4S2

BBA2-SHRINK (CDMA ONLY) ANALOG BASEBAND PROCESSORS



OVERVIEW

APPLICATION DESCRIPTION

The QUALCOMM Analog Baseband Processor (BBA2-shrink), also known as Q5312, is designed for use in dual-mode Code Division Multiple Access (CDMA) and FM portable cellular telephones. The BBA2-shrink interfaces between the RF and the digital processing circuitry of the telephone. The BBA2-shrink receive path circuitry converts analog Intermediate Frequency (IF) signals to the baseband frequency range, then converts the analog baseband signals into digital signals. The transmit path circuitry converts digital data into analog baseband signals which are then up-converted to the IF frequency range.

The BBA2-shrink includes receive and transmit Voltage Controlled Oscillators (VCOs) and other clock synthesis and processing circuits. There is also a general purpose Analog-to-Digital Converter (ADC) included for battery and signal strength monitoring. The BBA2 is designed to interface directly with QUALCOMM's Mobile Station Modem (MSM) family of devices. The MSM is a CMOS VLSI Application Specific Integrated Circuit (ASIC) that performs all of the digital processing in the telephone. The MSM along with the BBA2-shrink form the core of the portable CDMA/FM cellular telephone.

The BBA2-shrink is fabricated on an advanced Bi-CMOS process which accommodates both precision analog circuitry and low-power CMOS functions. The device has been designed to operate from nominal power supply voltage of 3.3 V, with power control logic keeping power consumption to a minimum. Electrical performance parameters are guaranteed over a –30°C to 85°C range.

The BBA2-shrink is packaged in an 80-lead Thin Plastic Quad Flat Pack (TQFP) package. With a lead pitch of 0.51 mm and a total above board thickness of 1.7 mm, the BBA2-shrink is designed for very dense mechanical assemblies.

There is a special purpose version of the BBA2-shrink which is intended for use in PCS, Wireless Local Loop and other applications where AMPS functionality is not required. This version of the BBA2-shrink is known as the "CDMA only" version (Q5312I-4S2). Specifications for the CDMA only BBA2-shrink are the same as for the dual-mode BBA2-shrink (Q5312I-3S2) except that specifications that apply to AMPS operation are not applied to the CDMA only version of the BBA2-shrink.

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FEATURES

- Dual–mode for CDMA and FM operation
- Receive signal path includes:
  - IF-to-baseband down-conversion
  - Separate CDMA and FM filters and ADCs
  - Conversion of analog baseband to digital format
  - CDMA sampling clock synthesizer
  - Rx IF VCO for I-Q mixer
  - Offset control loop
- Transmit signal path includes:
  - Conversion of digital I-Q data to analog baseband signals
  - Separate CDMA and FM filters and DACs
  - Baseband-to-IF up-conversion
  - Tx IF VCO and PLL for I-Q mixer
- Mode Control Logic for RXTX, SLEEP and IDLE Modes
- General purpose ADC for system monitoring
- Low power consumption in all modes

DEVICE APPLICATION

The BBA2-shrink bridges the gap between the analog RF processing and digital processing sections of the cellular telephone. Figure 1 shows the general circuit blocks in the portable cellular telephone employing BBA2-shrink and MSM.

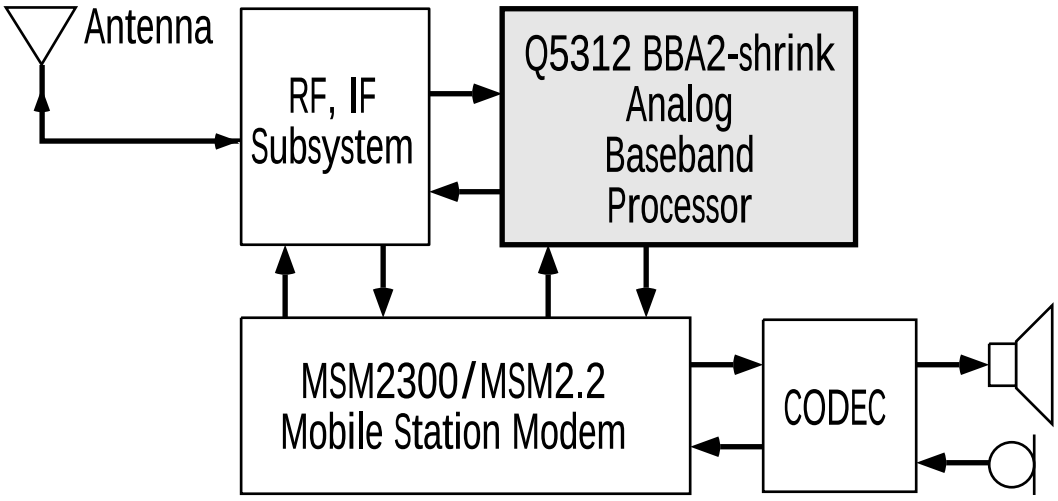
The analog inputs and outputs of BBA2-shrink interface directly with the IF transmit/receive circuitry of the telephone. The digital inputs and outputs of BBA2-shrink interface directly with the MSM.

The RF receive circuitry acquires the low-level forward-link signal from the base station (cell site) and down-converts the signal to the IF frequency band. The RF transmit circuitry takes CDMA or FM modulated analog IF from BBA2-shrink, up-converts the IF signal to the channel frequency and outputs controlled reverse-link power levels to the antenna.

The MSM performs all digital signal processing in the CDMA/FM cellular telephone. It includes digital processors for CDMA modulation/demodulation, digital FM modulation/demodulation, voice processing and a keypad interface. The CODEC (coder-decoder) block interfaces the telephone microphone and earpiece to the MSM. The MSM also has direct connections to the RF/IF section of the telephone for Automatic Gain Control (AGC) and calibration of the RF signal paths for receive and transmit.

The BBA2-shrink receive signal path down-converts the acquired IF signal to baseband where it is then converted to digital data. The digital baseband signals are sent to the MSM for demodulation. When transmitting, the MSM sends modulated digital baseband signals to the BBA2-shrink for up-conversion to the analog IF frequency.

Figure 1. Dual-Mode CDMA/FM Cellular Telephone Block Diagram



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GENERAL DESCRIPTION

The BBA2-shrink consists of a receive signal path, a transmit signal path, clock synthesis and buffering circuits, mode control logic and a general purpose ADC. Figure 2 shows the transmit and receive signal paths.

CDMA RECEIVE SIGNAL PATH

The receive signal path shown in Figure 3 is designed to accept a differential IF signal with CDMA spread spectrum modulation extending ±630 kHz from the IF center frequency of 85.38 MHz. This IF center frequency is not fixed by the BBA2-shrink, but is set by external components chosen by the designer. The incoming IF is demodulated to I and Q baseband components by mixing with 85.38 MHz Local Oscillator (LO) signals in quadrature followed by low-pass filtering.

The 85.38 MHz I and Q LO signals are generated on the BBA2-shrink device. The receive VCO is set to 170.76 MHz by an external varactor-tuned resonant tank circuit (inductor L and capacitor C connected in parallel). An external phase-lock loop and loop filter network provide feedback to varactors that tune the VCO to 170.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

Figure 2. BBA2-shrink Block Diagram

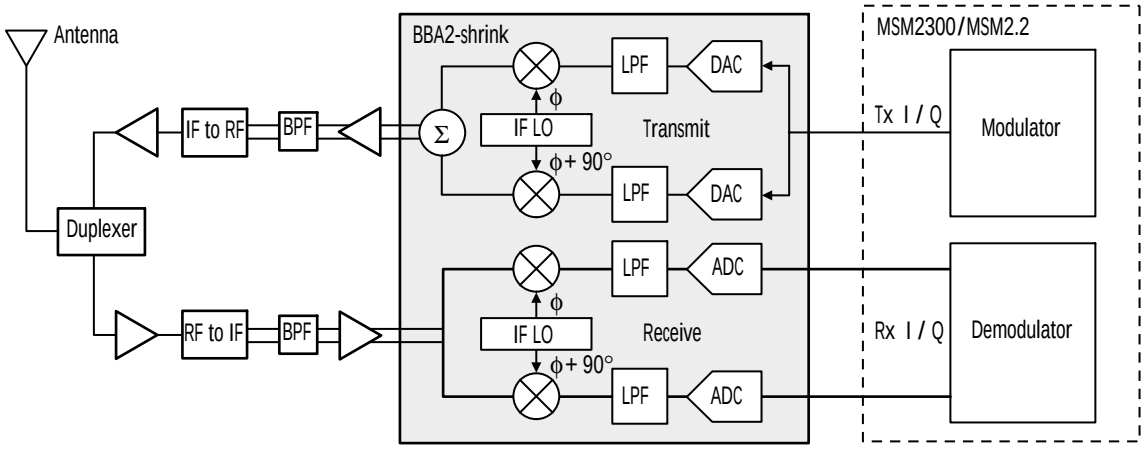
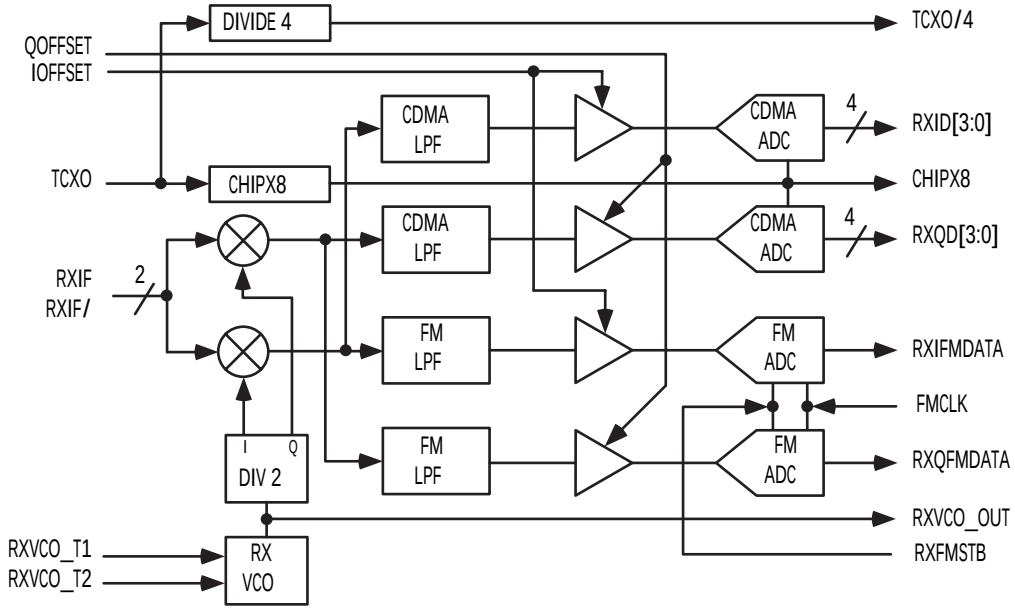


Figure 3. BBA2-shrink Receive Section Block Diagram



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CDMA LOW-PASS FILTERING

After mixing, the receive signal path splits into CDMA and FM sections. For CDMA, the baseband signal extends from 1 kHz to 630 kHz. Frequency components above 750 kHz are out-of-band for CDMA operation. The mixers and the subsequent CDMA low-pass filters combine to form the down-converter which outputs the CDMA baseband signals. The passband, transition band and rejection band characteristics of these low-pass filters, along with external IF bandpass filtering, enable the receiver to select the desired baseband signals from the jamming effects of unwanted signals.

Controlling the offset at the inputs of the ADCs is critical to the receive signal path and MSM digital signal processing. The offset control inputs are provided for this purpose. These inputs are normally driven (through long time-constant RC filters) by the MSM which senses the offset of the digital baseband data and creates a Pulse Density Modulated (PDM) signal for compensation.

CDMA ANALOG-TO-DIGITAL CONVERSION

Analog I and Q baseband components are converted to digital signals by the two identical 4-bit flash (parallel) ADCs. The CDMA ADCs output a new digital value on each rising edge of the ADC clock signal, CHIPX8.

The CHIPX8 ADC clock frequency of 9.8304 MHz is synthesized from the system crystal oscillator frequency of 19.68 MHz. The system crystal oscillator frequency is applied to the TCXO input of BBA2.

FM RECEIVE SIGNAL PATH

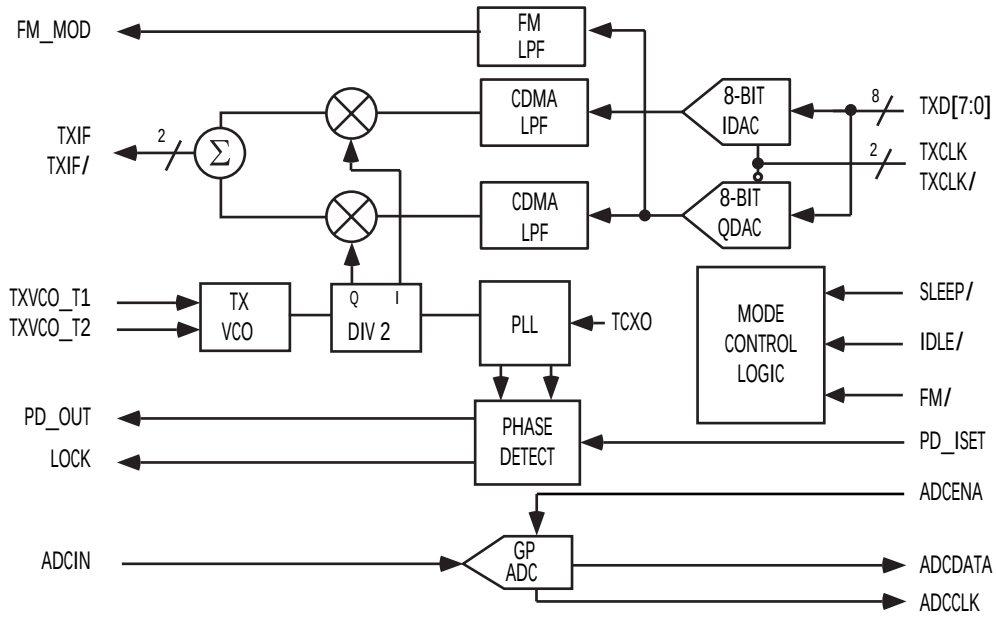
The receive signal path for FM operation is similar to that for CDMA operation. There are differences in the characteristics of the I and Q low-pass filters and the ADCs. The IF frequency is the same as in CDMA (85.38 MHz), but the modulation can only extend ±15 kHz from the IF center frequency to form a 30 kHz wide channel. The low-pass filters for FM operation have a much lower bandwidth than those used in CDMA. The offset of the FM low-pass filters is controlled just like the CDMA low-pass filters by the offset control input pins.

The lower bandwidth of the FM baseband signal allows very low power 8-bit ADCs to be used. The FM I and Q analog baseband signals are sampled and held during the analog-to-digital (A/D) conversion process. The A/D conversion is initiated with a strobe from the MSM. A serial data stream is output beginning with the Most Significant Bit (MSB) of the result.

CDMA TRANSMIT SIGNAL PATH

The BBA2-shrink transmit signal path (shown in Figure 4) accepts digital I and Q baseband data from the

Figure 4. BBA2-shrink Transmit Section Block Diagram



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MSM, and outputs modulated IF centered at 130.38 MHz to the RF transmitter.

CDMA DIGITAL-TO-ANALOG CONVERSION AND FILTERS

Eight bits of I and Q transmit data are multiplexed over an 8-bit input port into the BBA2-shrink CDMA DACs. The transmit data rate is twice as fast as the differential transmit clock, TXCLK and TXCLK/. Incoming data that is valid during the rising edge of the transmit clock is registered into the I DAC. Incoming data that is valid during the falling edge of the transmit clock is registered into the Q DAC. I and Q transmit data values have been compensated in the MSM to account for their ½ clock cycle time difference.

The frequency spectrum at the output of the CDMA DACs contains unwanted frequency components due to DAC output transition edges and transients. The transmit clock frequency and harmonics are found in the spectrum and are also undesirable. Each CDMA DAC is followed by an anti-aliasing low-pass filter with a bandwidth of 630 kHz that reduces unwanted frequency components. Unlike the low-pass filters in the receive signal path, these low-pass filters do not require offset controls.

UP-CONVERTING TO IF

The BBA2-shrink transmit path outputs a differential IF signal with CDMA spread spectrum modulation extending ±630 kHz from the transmit IF center frequency of 130.38 MHz. The analog I and Q baseband components from the CDMA low-pass filters are mixed in quadrature with unmodulated I and Q signals at 130.38 MHz. After mixing, the I and Q IF components are summed and output differentially.

The 130.38 MHz I and Q LO signals are generated on the BBA2-shrink. The transmit VCO is set to 260.76 MHz by an external varactor-tuned resonant tank circuit. An internal phase-lock loop and external loop filter network provides the feedback to the varactors that tune the VCO precisely to 260.76 MHz. A master-slave divide-by-two circuit generates I and Q signals in precise quadrature for the mixers.

FM TRANSMIT SIGNAL PATH

An analog FM modulation signal is constructed from 8-bit digital data supplied by the MSM. Only the Q-channel DAC is used in the BBA2-shrink in FM Mode. All other CDMA circuits are disabled. The DAC output is filtered by a low-pass anti-aliasing filter. The filtered DAC output is the analog FM modulation signal. This signal modulates the frequency of the BBA2-shrink transmit VCO using external components when in FM RXTX Mode. The modulated VCO frequency is halved by divide-by-two circuitry and output on the transmit IF outputs.

OPERATING MODES

The telephone has several modes of operation that determine the circuit block activity level in the BBA2-shrink. The CDMA RXTX or FM RXTX Modes are in effect when the telephone is making a call. IDLE Mode is in effect when no call is in progress, but the telephone receiver is active (ready to answer a call). SLEEP Mode is a low-power mode in which the telephone cannot receive a call but where the digital processor and keypad are still enabled.

The telephone has an additional mode, called Slotted Paging Mode. When in this mode, the MSM toggles itself and the BBA2-shrink between SLEEP and IDLE Modes using a programmable timing interval. This mode allows the telephone to be contacted by the base station without requiring the telephone to be continuously in IDLE Mode. Slotted Paging Mode consumes much less power than IDLE Mode.

The BBA2-shrink operating modes are defined by the states of three digital inputs that come directly from the MSM. These logic signals minimize the power consumed by the BBA2-shrink by disabling unused circuits. The selected circuits in BBA2-shrink become active after the states of the operating mode controls are changed.

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GENERAL PURPOSE ADC

The General Purpose (GP) ADC provides DC measurement capability to the telephone during all modes of operation. It is a low speed, 8-bit resolution ADC. It is designed to digitize DC voltages applied to the ADC input pin from battery level, temperature and other low frequency control or monitoring sensors.

The ADC is in a power-down state during normal BBA2-shrink operation. It is activated by a positive-going pulse on the ADC enable pin. When this input is driven high, the GP ADC powers up and begins a conversion. The DC voltage to be measured must be applied to the ADC input for the duration of the conversion. The ADC output is available from a serial digital interface. Each of the eight data bits is valid (MSB first) during the rising edge of the ADC clock output. When the Least Significant Bit (LSB) of the conversion has been clocked out, the conversion is complete and the ADC returns to a power down condition. The ADC clock and data outputs will be low before and after a conversion. Conversions can only be started when the ADC is inactive after a conversion has been completed. A rising edge of the ADC enable pin during a conversion will be ignored. ADC enable must be low and a conversion completed before a new conversion can be started.

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INPUT / OUTPUT SIGNALS

Figure 5 shows the functions provided by the BBA2-shrink's pins and the size of its 80-pin TQFP package. Table 1 provides descriptions of the pin functions.

Figure 5. Q5312 BBA2-shrink Analog Baseband Processor Functional Diagram

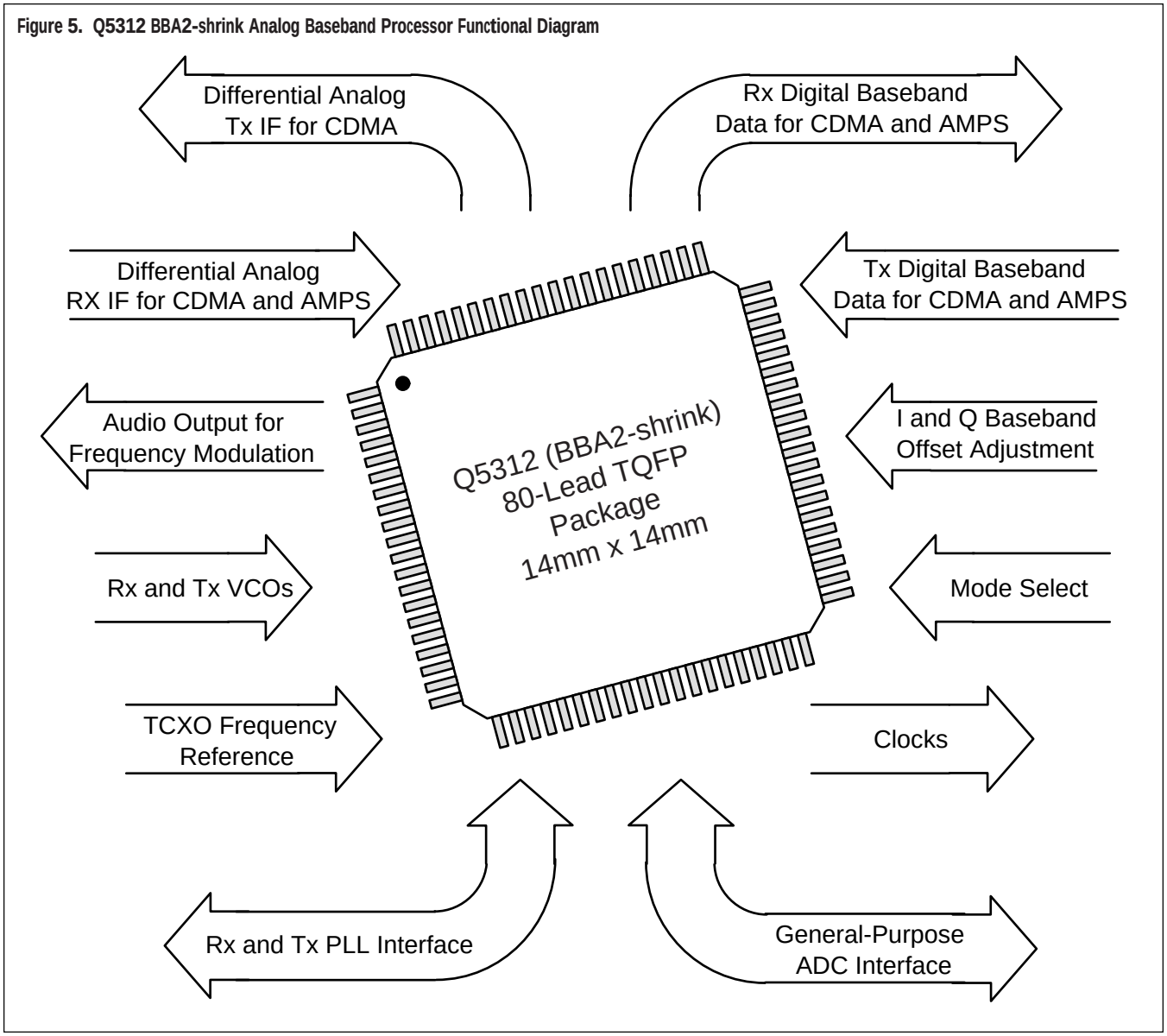

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Table 1. BBA2-shrink Pin Functions

PIN FUNCTIONS	DESCRIPTION
Rx Digital Baseband Data for CDMA and AMPS	The BBA2-shrink chip converts the receive IF signal from the RF subsystem of the subscriber unit to digital baseband data for both CDMA and AMPS.
Tx Digital Baseband Data for CDMA and AMPS	The MSM2300/MSM2.2 generates transmit digital baseband for the BBA2-shrink chip. The BBA2-shrink chip converts that data to an analog IF frequency of the subscriber unit.
I and Q Baseband Offset Adjustment	DC offsets in the receive signal path are removed by way of analog control signals from the MSM2300/MSM2.2. The MSM2300/MSM2.2 control signals use PDM which form DC control signals after being filtered with single-pole RC low-pass filters.
Mode Select	Digital controls from the MSM2300/MSM2.2 put the BBA2-shrink into CDMA or FM Mode, IDLE (receive-only) Mode or SLEEP (minimum power consumption) Mode.
Clocks	The system frequency reference of 19.68 MHz is used to generate clocks for the MSM2300/MSM2.2. CHIPX8 (9.9304 MHz) and TCXO/4 a (4.92 MHz) are generated on the BBA2-shrink chip.
General Purpose ADC Interface	The General-Purpose ADC is generally used for monitoring the subscriber unit battery voltage, RF power output level or temperature. The ADC interface is controlled by the MSM2300/MSM2.2.
Tx PLL Interface	The BBA2-shrink includes a complete Transit PLL for generating the TX IF frequency. The PLL includes a phase detector and requires a simple external loop filter.
Rx and Tx VCOs	The BBA2-shrink chip includes all VCO circuits except the resonant tank. The VCOs operate differentially, reducing common mode noise and improving performance.
Audio Output for Frequency Modulation	In AMPS Mode, frequency-modulation is accomplished by a connection from the BBA2-shrink to the varactor diodes of the transmit VCO.
Differential Analog Rx IF Inputs and TXIF Outputs	The receive IF inputs of the BBA2-shrink are differential, improving performance and reducing cross-coupled noise.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2 shows the absolute maximim ratings of the Q5213 (BBA2-shrink). Operating the BBA2-shrink under conditions that exceed those in the Absolute Maximum Ratings table may result in damage to the device. Absolute Maximum Ratings are limiting values, to be considered individually, while all the other parameters are within their specified operating ranges. Functional operation of the BBA2-shrink under any of the conditions in the Absolute Maximum Rating table is not implied.

Table 2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}, V_{DDD}	Power Supply Voltage	-0.5	+5.0	V
V_I	Voltage on any INPUT Pin	-0.5	V_{DD} + 0.5	V
V_{SC}	Short Circuit Duration, to GND or V_{DD}	–	1	sec
T_S	Storage Temperature	-55	+150	°C
I_{IN}	Current Into or Out of any Pin	–	±200	mA
T_L	Lead Soldering Temperature (10 sec Max.)	–	280	°C
V_{ESD}	ESD Voltage (each pin)	–	1500	V

RECOMMENDED OPERATING CONDITIONS

Table 3 shows the recommended operating conditions. Operating conditions include power supply voltage and ambient temperature parameters that are under the control of the user. The BBA2-shrink meets all electrical, switching and system performance limits when operated in compliance with the recommended operating conditions.

Table 3. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}, V_{DDD}	Power Supply Voltage	3.13	3.47	V
T_A	Ambient Operating Temperature	-30	+85	°C

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ELECTRICAL CHARACTERISTICS

Table 4 shows the electrical characteristics. Electrical characteristics include both physical characteristics such as capacitance, resistance and impedance, and DC characteristics such as digital I/O levels, reference voltages and power supply current. In Table 4, values in the Typical column are based on a 25° C, 3.3 V power supply.

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
I_{DD1}	Power Supply Current. CDMA RXTX Mode.	–	42.9	65	mA
I_{DD2}	Power Supply Current. CDMA IDLE Mode.	–	22.3	29.4	mA
I_{DD3}	Power Supply Current. CDMA SLEEP Mode.	–	1.53	2.65	mA
I_{DD4}	Power Supply Current. FM RXTX Mode.	–	29.5	41.5	mA
I_{DD5}	Power Supply Current. FM IDLE Mode.	–	13.2	20.2	mA
V_{IH}	Logic High Input Voltage.	0.7 x V_{DD}	–	–	V
V_{IL}	Logic Low Input Voltage.	–	–	0.3 x V_{DD}	V
V_{OH}	Logic High Output Voltage. V_{DD} = 3.13 V. I_{OH} current = 300 µA. Larger current provided for digital output transactions.	2.7	–	–	V
V_{OL}	Logic Low Output Voltage. V_{DD} = 3.47 V. I_{OH} current = 100 µA. Larger current provided for digital output transactions.	–	–	0.4	V
I_{IL}	Logic Input Leakage Current. V_{DD} = MAX., V_{IN} = GND to V_{DD}.	–	–	±100	µA
C_{IND}	Input Capacitance, Digital Input.	–	–	15	pF
C_{LD}	Digital Output Load Capacitance.	–	–	20	pF
R_{INRX}	Input Resistance. RXIF to RXIF/ Differential.	400	550	740	Ω
C_{INRX}	Input Capacitance. RXIF and RXIF/ to Ground.	–	0.40	–	pF
Z_{OFF}	Offset Adjust Input Impedance. IOFFSET, QOFFSET.	100	–	–	kΩ
R_L	Load Resistance. TXIF to TXIF/ Differential.	495	500	505	Ω
C_L	Load Capacitance. TXIF, TXIF/ to Ground.	–	–	5	pF
Z_{TX}	Output Impedance. TXIF, TXIF/, Differential.	–	–	60	Ω
Z_{VCO}	VCO Tuning Circuit Input Impedance. RXVOC_T[1:2], TXVCO_T[1:2].	–	2	–	kΩ
Z_{PD}	PD_OUT Output Impedance. Within Compliance Range.	1	–	–	MΩ
LK_{VOL}	LOCK Output Logic Low Voltage. RLD ≥ 10 kΩ to V_{DD}.	–	–	0.4	V
LK_{IOH}	LOCK Output Leakage Current. V_{OUT} = V_{DD}.	–	–	10	µA
Z_{TC}	TCXO Input Impedance.	5	–	–	kΩ
Z_{INAD}	General-Purpose ADC Input Impedance. ADCIN.	20	–	–	kΩ
V_{INAD}	General-Purpose ADC Input Signal Range. V_{DD} = 3.3 V.	0.5	–	2.5	V
V_{OXO4}	TCXO/4 Output Signal Level. Into 10 kΩ load in parallel with 10 pF.	1.5	–	–	V_{PP}
R_{SAD}	General-Purpose ADC Source Resistance. Connected to ADCIN pin.	–	–	39	Ω

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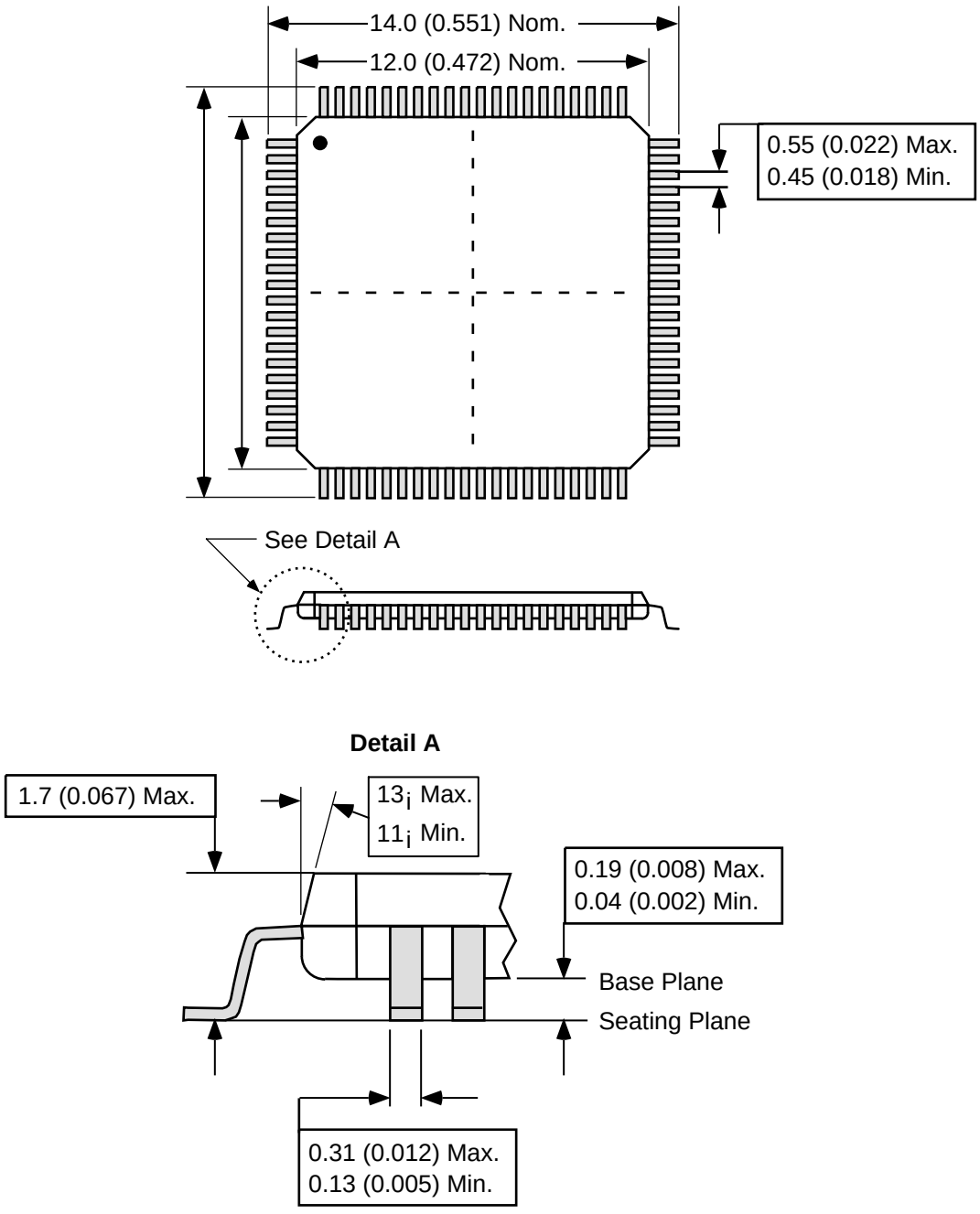
MECHANICAL SPECIFICATIONS

The Q5213 (BBA2-shrink) is packaged in an 80-pin Thin Quad Flat Pack (TQFP) package. The TQFP has 20-mil lead pitch and is no greater than 1.7 mm above the seating plane (JEDEC Publication 95 MS-026 Variation BDD). Figure 6 shows the package outline drawing.

Figure 6. 80-pin TQFP Package Outline Drawing



Dimensions: millimeters (inches)

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IFR3000 / IFT3000
RX AND TX IF / BASEBAND PROCESSORS

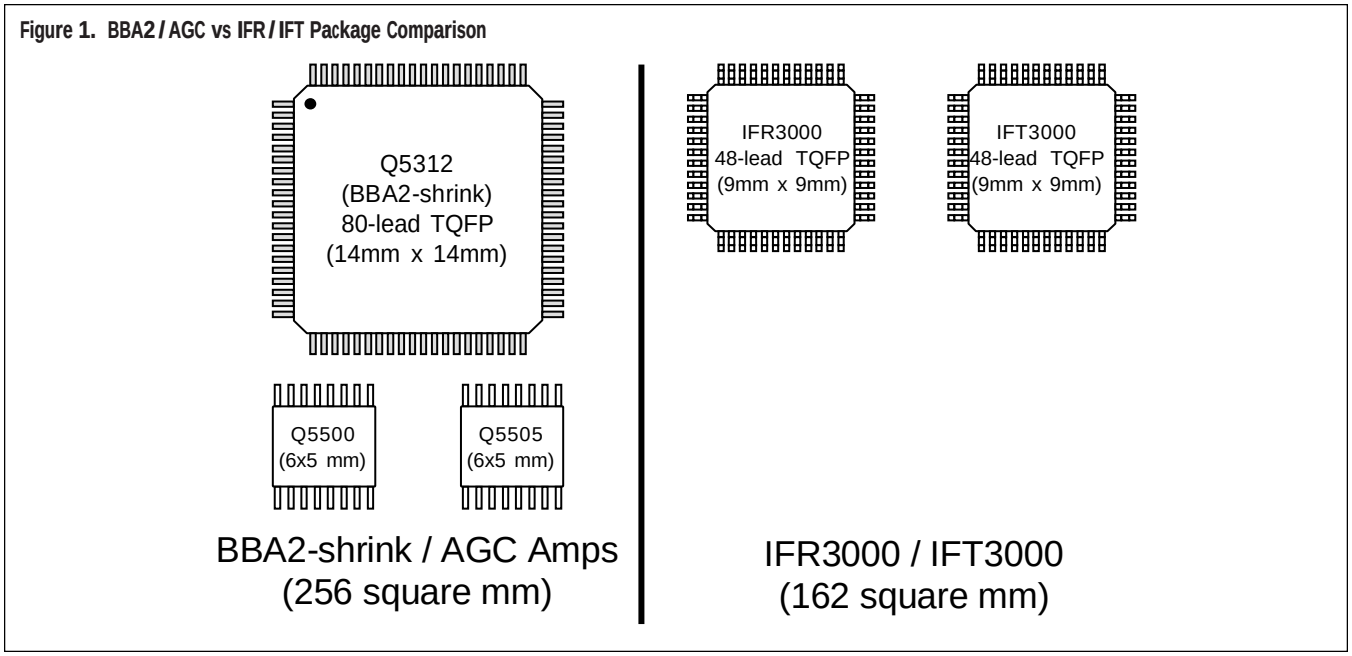
PRELIMINARY SPECIFICATION

OVERVIEW

The QUALCOMM IFR3000 and IFT3000 Rx and Tx IF/Baseband processors offer significant reduction in cost, size and pin count over previous generation products. By integrating the functionality of three Application Specific Integrated Circuits (ASICs) into two ASICs, designers now possess IF-to-Baseband and Baseband-to-IF processing power and Rx and Tx Automatic Gain Control (AGC) circuitry on two 48-pin plastic thin quad flat pack (TQFP) packages.

The IFR3000 and IFT3000 incorporate all the Rx and Tx processing capability of the QUALCOMM Q5312 Analog Baseband Processor (BBA2-shrink) together with the automatic gain control functionality of the QUALCOMM Q5500 Rx and Q5505 Tx AGC Amplifiers. The result is a more economic, two-chip analog baseband solution which offers telephone designers a 40% reduction in size. See Figure 1 for a size comparison between using Q5312 (BBA2), Q5500 and Q5505 (AGCs) versus using IFR3000 and IFT3000.

Figure 1. BBA2 / AGC vs IFR / IFT Package Comparison



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The IFR3000 and IFT3000 Rx and Tx IF/Baseband processors are designed for use in dual-mode CDMA and FM portable cellular telephones. The IFR3000 and IFT3000 interface between the radio-frequency (RF) section and the digital processing circuitry of the telephone.

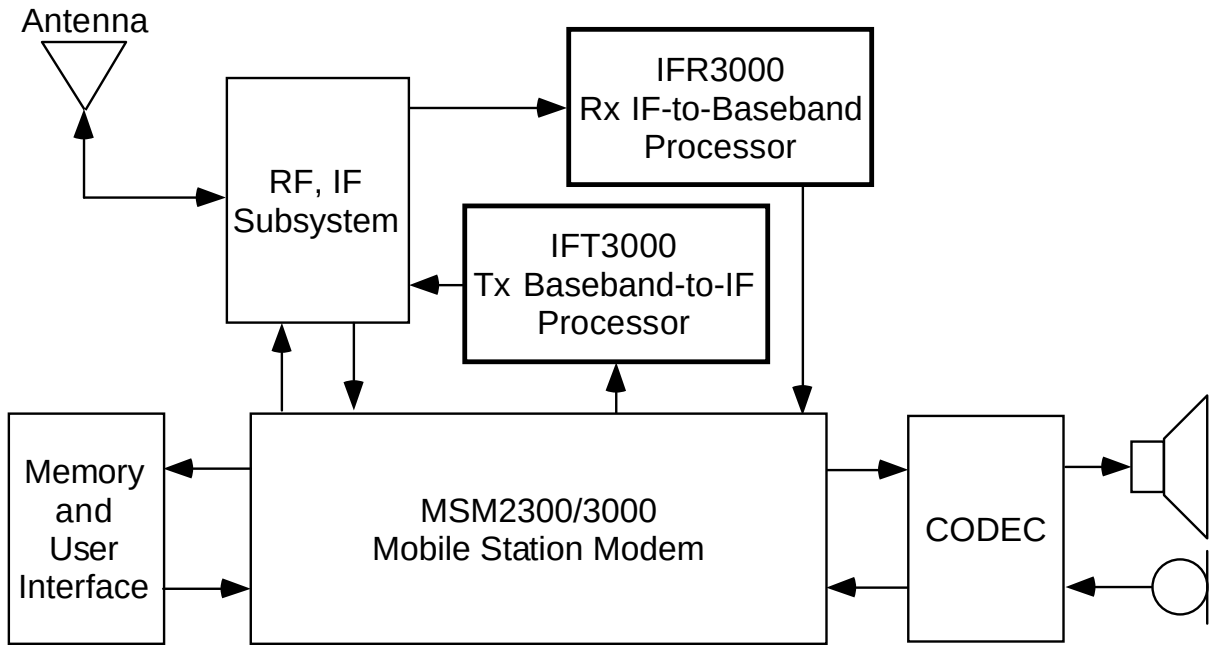
The circuit blocks within the IFR3000 include the Rx AGC amplifier with 90 dB dynamic range, IF mixer and CDMA/FM low-pass filters for down-converting IF to analog baseband, and analog-to-digital converters (ADC) for converting to digital baseband. The IFR3000 includes clock generators that drive the telephone's digital processor and a voltage-controlled oscillator (VCO) which generates the Rx mixer local oscillator (LO) signal.

The circuit blocks within the IFT3000 include digital-to-analog converters (DAC) for converting digital baseband to analog baseband, low-pass filters, a mixer for up-converting to IF and an 85 dB dynamic range Tx AGC amplifier. The IFT3000 includes a fully programmable phase-locked loop (PLL) for generating Tx LO and IF frequencies. The IFT3000 also has an 8-bit general purpose ADC with three selectable inputs for monitoring battery level, RF signal strength and phone temperature.

Both the IFR3000 and IFT3000 interface directly with QUALCOMM's Mobile Station Modem (MSM) ASICs. The MSM ASICs are CMOS VLSI integrated circuits that perform all digital processing in the CDMA/FM subscriber unit. The combination of IFR3000, IFT3000 and MSM family ASICs form the core of the portable CDMA/FM subscriber unit. Refer to Figure 2 which shows a diagram of the IFR3000 and IFT3000 used along with MSM2300 or MSM3000 in a subscriber unit.

The IFR3000 and IFT3000 are fabricated on an advanced BiCMOS process which accommodates both precision high-frequency analog circuitry and low-power CMOS functions. Designed to operate from a power supply voltage range of 2.7 to 3.6 Volts, the IFR3000 and IFT3000 minimize power consumption, chip count and circuit complexity. Electrical performance parameters are guaranteed over the –30°C to 85°C range.

Figure 2. IFR3000 / IFT3000 in a Subscriber Unit



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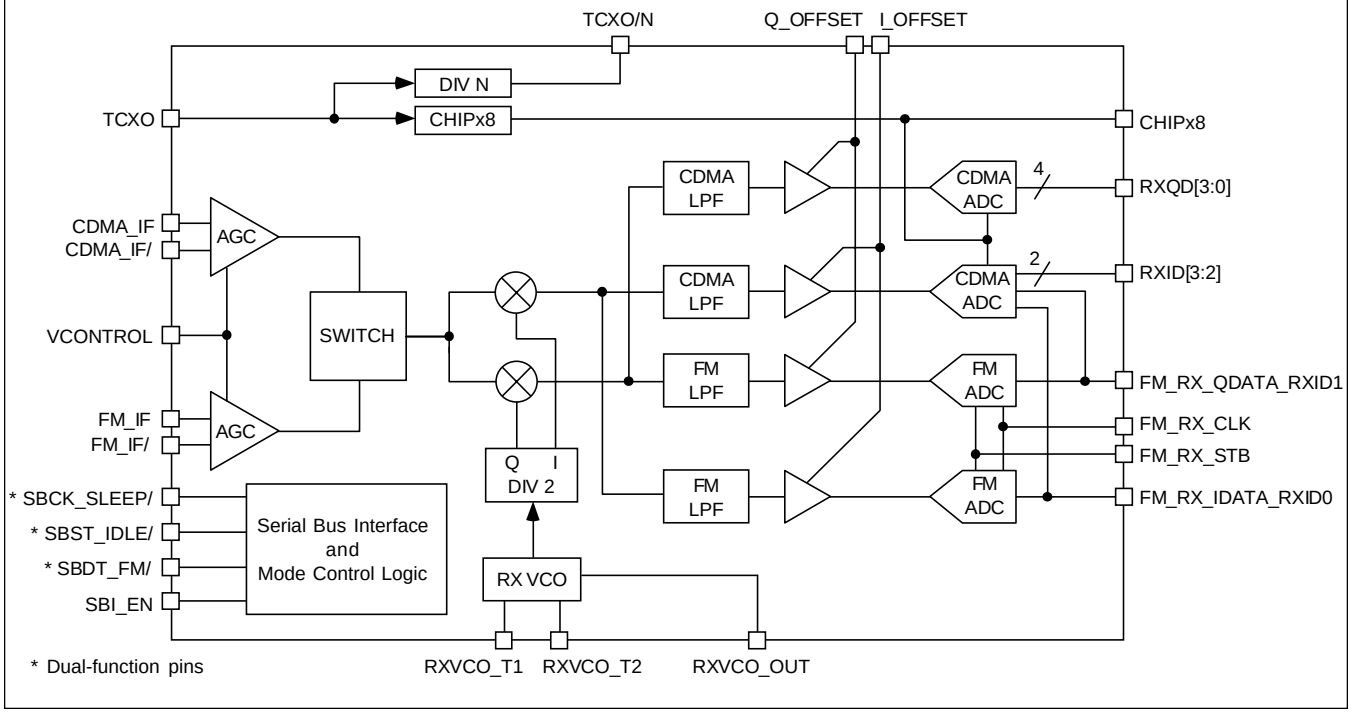
IFR3000 SPECIFICATIONS

Figure 3 shows a functional block diagram of the IFR3000 Rx IF/Baseband Processor.

IFR3000 FEATURES

- Supports IS-98 (CDMA) and IS-19 (AMPS) standards for dual–mode operation
- Operates on 2.7 V to 3.6 V supply voltage
- Low current: 27 / 21 mA in CDMA Rx / FM Rx Modes
- Rx power control through 90 dB dynamic range AGC amplifier
- IF mixer for down-converting IF to analog baseband
- Low-pass filtering for CDMA and FM I- and Q-component baseband signal demodulation
- 4-bit ADCs convert CDMA I and Q analog baseband components to digital baseband
- 8-bit ADCs convert FM I and Q analog baseband components to digital baseband
- Clock generators for CDMA / AMPS operation
- VCO for generation of Rx LO mixing signal
- I- and Q-channel DC offset control inputs drive baseband DC voltage offset to zero in CDMA and FM signal paths
- Operational Mode compatibility with the MSM2300 and MSM3000
- Enhanced features with MSM3000 through three-line serial bus interface (SBI):
  - Slotted FM Mode
  - Selective power-down
  - Mode selection
- 48-lead TQFP packaging for dense circuit assemblies

Figure 3. IFR3000 Functional Block Diagram



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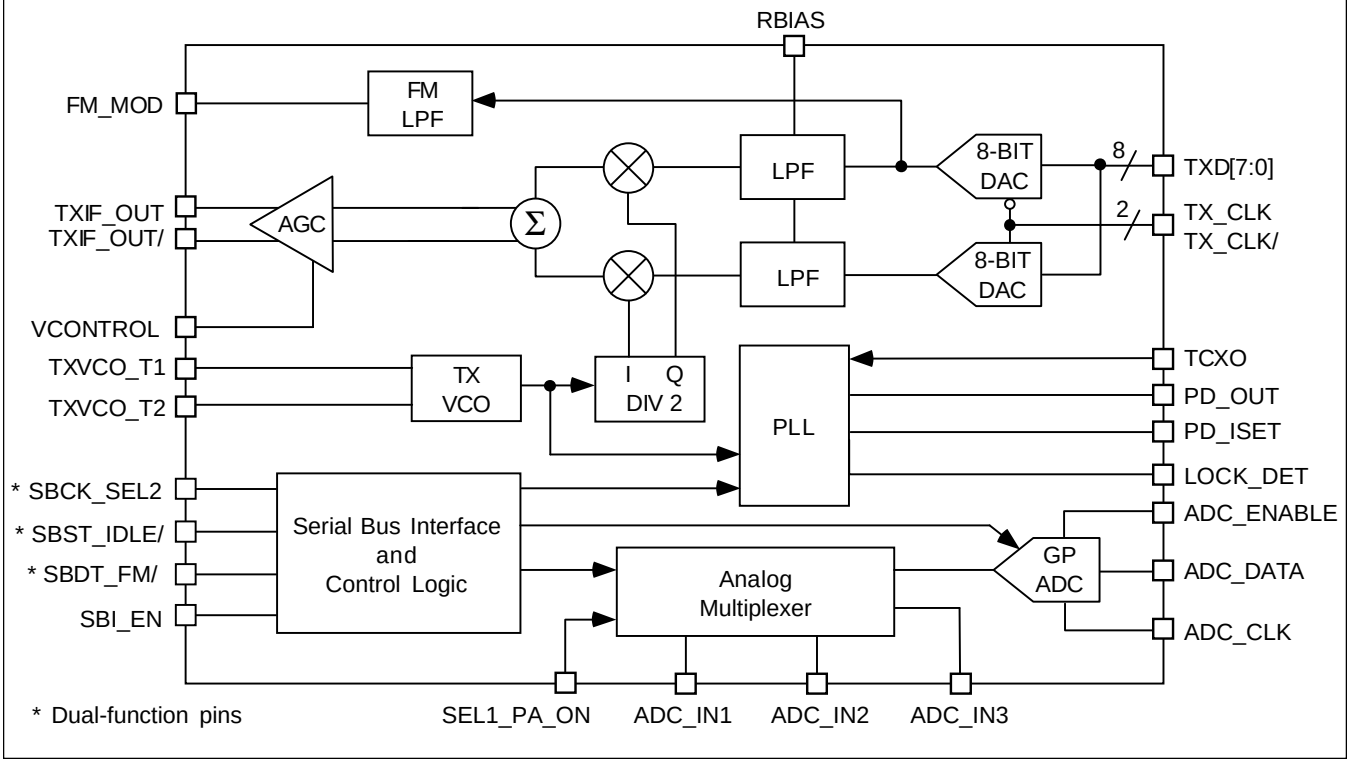
IFT3000 SPECIFICATIONS

Figure 4 shows a functional block diagram of the IFT3000 Tx IF/Baseband Processor.

IFT3000 FEATURES:

- Supports IS-98 (CDMA) and IS-19 (AMPS) standards for dual–mode operation
- Operates on 2.7 V to 3.6 V supply voltage
- 8-bit DACs convert digital baseband signals to analog baseband
- CDMA and FM signal paths include low-pass filters for I and Q output waveform smoothing
- IF mixer up-converts analog baseband to IF
- Tx power control through 85 dB dynamic range AGC amplifier
- Programmable Tx PLL for generating Tx IF frequency
- VCO for generation of Tx LO mixing signal
- 8-bit general-purpose ADC with 3-input analog multiplexer and selectable input ranges
- Operational Mode compatibility with the MSM2300 and MSM3000
- Enhanced features with MSM3000 through three-line serial bus interface (SBI):
  - Tx PLL phase-detector polarity
  - Tx PLL programmability
  - Punctured CDMA transmission
  - Selective power-down
  - Mode selection
- 48-lead TQFP packaging for dense circuit assemblies

Figure 4. IFT3000 Functional Block Diagram



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INPUT / OUTPUT SIGNALS

Figure 5 shows the functions provided by the IFR3000's and IFR3000's pins and the size of their 48-pin TQFP package. Table 1 provides descriptions of the pin functions.

Figure 5. IFR3000 / IFT3000 Rx and Tx IF / Baseband Processors Functional Diagram

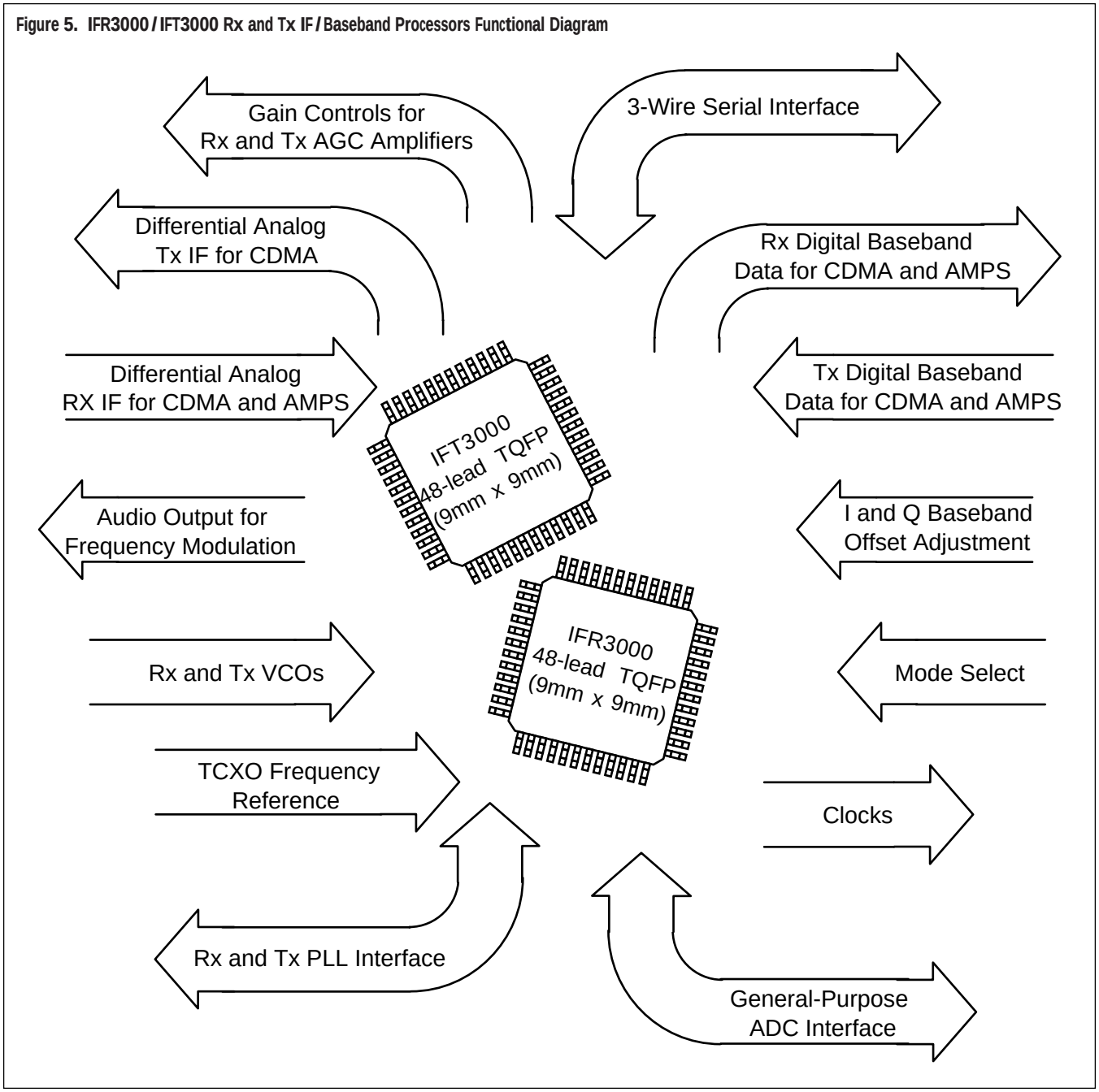

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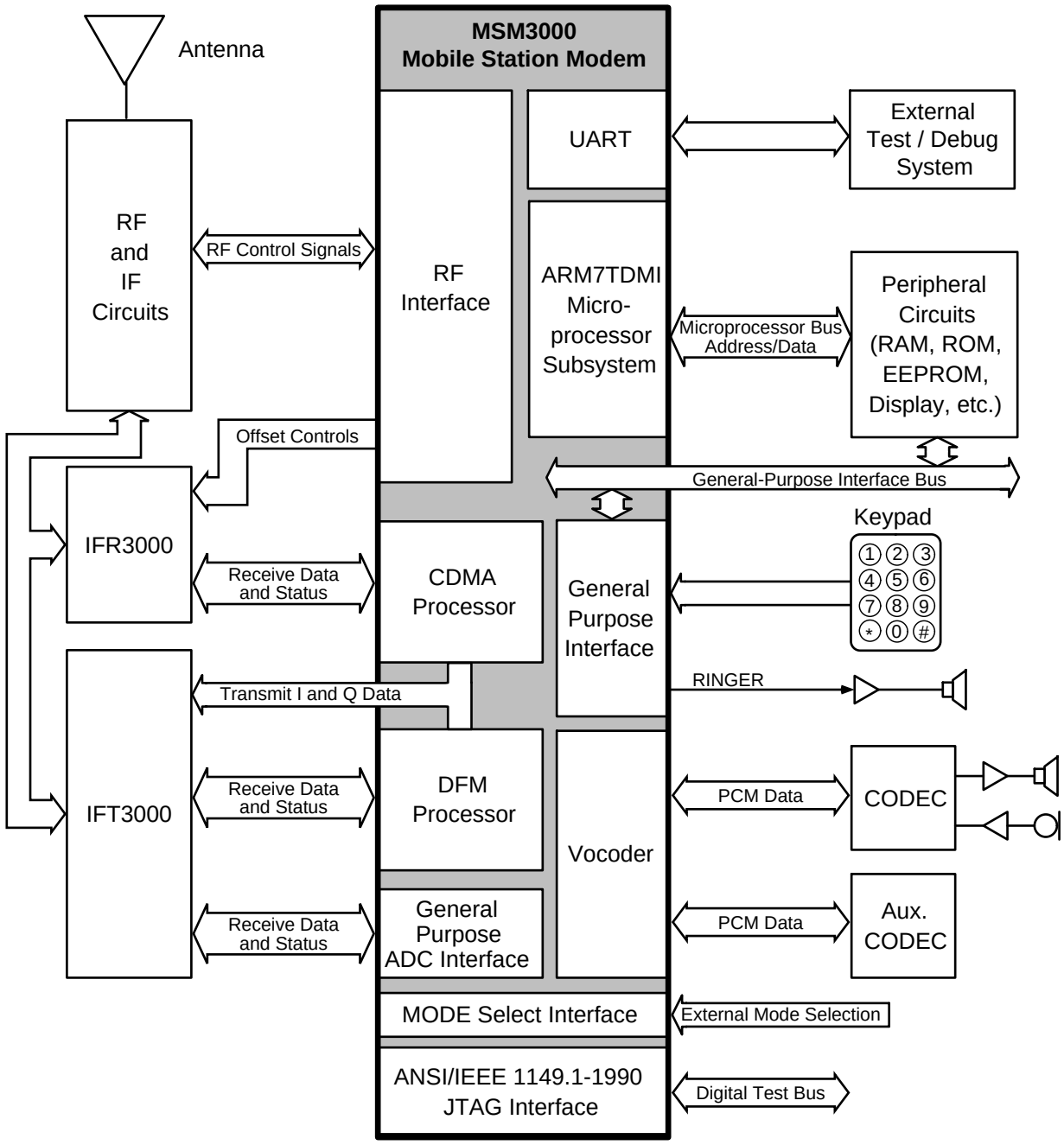
Table 1. IFR3000/IFT3000 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Rx Digital Baseband Data for CDMA and AMPS	The IFR3000/IFT3000 chips convert the receive IF signal from the RF subsystem of the subscriber unit to digital baseband data for both CDMA and AMPS.
Tx Digital Baseband Data for CDMA and AMPS	The MSM3000 generates transmit digital baseband for the IFR3000/IFT3000 chips. The IFR3000/IFT3000 chips convert that data to an analog IF frequency of the subscriber unit.
I and Q Baseband Offset Adjustment	DC offsets in the receive signal path are removed by way of analog control signals from the MSM3000. The MSM3000 control signals use PDM which form DC control signals after being filtered with single-pole RC low-pass filters.
Mode Select	Digital controls from the MSM3000 put the IFR3000/IFT3000 chips into CDMA or FM Mode, IDLE (receive-only) Mode or SLEEP (minimum power consumption) Mode.
Clocks	The system frequency reference of 19.68 MHz is used to generate clocks for the MSM3000. CHIPX8 (9.9304 MHz) and TCXO/4 (4.92 MHz) are generated on the IFR3000/IFT3000 chips.
General Purpose ADC Interface	The General-Purpose ADC is generally used for monitoring the subscriber unit battery voltage, RF power output level or temperature. The ADC interface is controlled by the MSM3000.
Tx PLL Interface	The IFT3000 chip includes a complete Transit PLL for generating the TX IF frequency. The PLL includes a phase detector and requires a simple external loop filter.
Rx and Tx VCOs	The IFR3000/IFT3000 chips includes all VCO circuits except the resonant tank. The VCOs operate differentially, reducing common mode noise and improving performance.
Audio Output for Frequency Modulation	In AMPS Mode, frequency-modulation is accomplished by a connection from the IFR3000/IFT3000 chips to the varactor diodes of the transmit VCO.
Differential Analog Rx IF Inputs and Tx IF Outputs	The receive IF inputs of the IFR3000 chip are differential, improving performance and reducing cross-couple noise.
Gain Controls for Rx and Tx AGC Amplifiers	The IFR3000/IFT3000 chips include AGC amplifiers for the IF Rx and Tx signal paths. Gain control inputs for these amplifiers are driven by the MSM3000.
3-Wire Serial Interface	A 3-wire serial bus (slave) is included on the IFR3000/IFT3000 chips. The serial interface is driven by the MSM3000 (master) and is used for setup and control of the IFR3000/IFT3000 chips.

IFR3000 / IFT3000 / MSM3000 INTERFACE

Figure 6 shows the interface between the IFR3000, IFT3000 and MSM3000 in a subscriber unit.

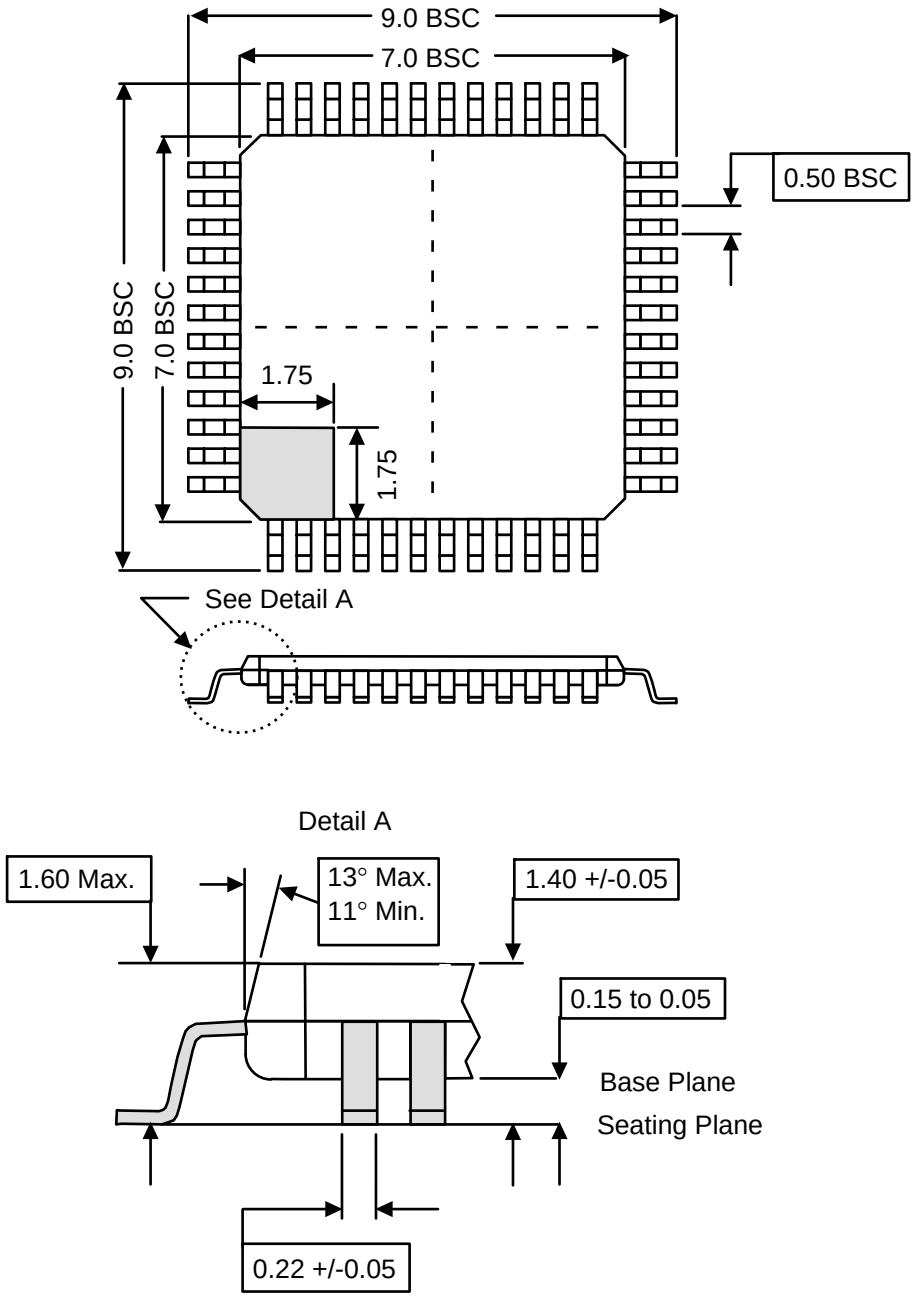
Figure 6. IFR3000 / IFT3000 / MSM3000 Interface



MECHANICAL SPECIFICATIONS

The IFR3000 and IFT3000 are both packaged in a 48-pin Thin Quad Flat Pack (TQFP) package. Figure 7 shows the package outline drawing.

Figure 7. 48-pin TQFP Package Outline Drawing



Dimensions: millimeters

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Q5165

CELL SITE MODEM

CSM1.5

OVERVIEW

The Cell Site Modem (CSM), developed by QUALCOMM Incorporated, is a CDMA digital baseband modem incorporating three individual integrated circuits into a single device (previously a six-device set). The CSM integrates the CDMA Modulator, CDMA Demodulator and Serial Viterbi Decoder modules to provide reduced costs and improved functionality for the base station. The device also improves performance with the CDMA subscriber unit.

The CSM provides QUALCOMM's CDMA licensees with an IS-95 compliant system and a PCS compliant system at 14.4 kbps on a single device. The CSM includes a high-precision Fast Hadamard Transform Engine (FHTE) offering significant performance advantages, as well as a high-performance search engine. For higher quality communications, the searcher, connected to a series of antennas, identifies optimum multipath peaks. The CSM also supports three-way softer hand-off.

PERFORMANCE

Integrating the modulator, demodulator, Viterbi decoder and their associated components into the CSM reduces the microprocessor overhead requirements, eliminates the need for external transmit summer circuitry and allows for greater board density. Improvements in the demodulator, including an optimal soft decision combining technique, provide performance improvements of 17% to 90% (0.7 to 2.8 dB), with a minimum 50% (1.7 dB) average, over QUALCOMM's Base Station Chipset. These improvements lower the output power requirements of the mobile station, resulting in a notable increase in total channel capacity.

Figure 1. Block Diagram of the CSM in the Cell Site

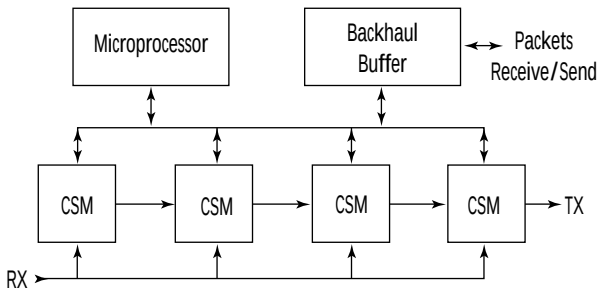

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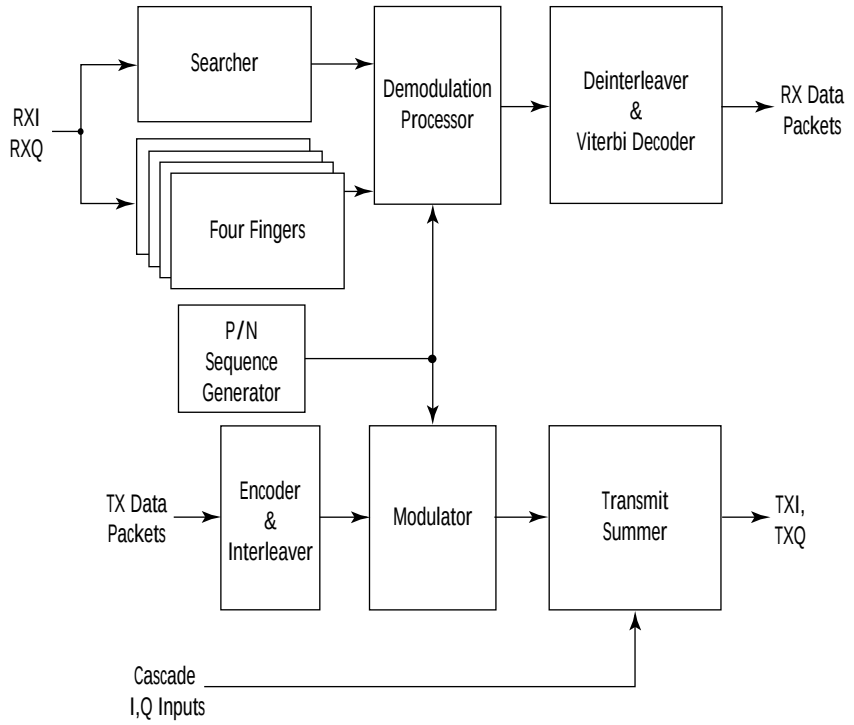
Figure 2. CSM Block diagram



CSM FUNCTIONAL OVERVIEW

SEARCHER

After selecting an antenna set for a search and programming the position and size of the search window, the searcher initiates the search and finds the largest multipath peaks within the search parameter set. Normally, the searcher operates continuously; while the results from a search are read, the next search is already underway. For acquisition searches, the searcher results can be used to detect the presence of a mobile attempting to access the CDMA network. For demodulator multipath searches, fingers may be assigned to the reported paths to improve the demodulator performance of the rake receiver.

FOUR FINGERS

The four fingers make up a front end interface to the demodulator. The fingers provide timing, Walsh chip accumulation, and Walsh chip storage for the demodulation process. The fingers may be programmed to accept data from the same or differing antenna sources.

DEMODULATION PROCESSOR

The demodulation processor performs Fast Hadamard Transforms for the searcher and the four fingers. It also performs optimal soft combining of data from the fingers and performs power calculations, including lock detection and power control decisions.

DEINTERLEAVER & VITERBI DECODER

The deinterleaver is used to reverse the interleaving performed by the mobile unit. Interleaving provides protection against burst errors and fades.

The Viterbi decoder, using the Viterbi algorithm, optimally decodes the convolutional coding from the mobile unit. Quality bits and CRC bits are used to verify the quality of the decoded data.

PN SEQUENCE GENERATORS

There are several PN generators within the CSM. The PN sequences generated are the I channel, Q channel, and long code sequences for both forward and reverse link processing.

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ENCODER & INTERLEAVER

The encoder takes forward link data frames, convolutionally encodes them and performs symbol repetition for bit rates less than full rate. The encoder also automatically generates CRCs for the frames that require them.

The interleaver is used to provide time diversity in transmitted symbols, thereby providing protection from relatively long transmission fades and burst errors. The effects of the interleaver are reversed in the mobile unit deinterleaver.

MODULATOR

The modulator contains three individually programmable sections that generate forward link information streams from the interleaver output. The symbols from the interleaver are scrambled with the long code PN sequence and punctured with power control bits, if appropriate. The punctured symbols are covered with the proper Walsh code and spread with the I and Q PN sequences. The resulting chips are then bandlimited with FIR filters and multiplied by a programmable gain factor. Each of the three transmit sectors supported by the CSM can be driven by a particular section of the modulator, the sum of all three sections or zero.

TRANSMIT SUMMER

The transmit summer provides a flexible method for cascading several CSMs. The outputs from the first CSM in a daisy-chain are connected to the cascade inputs of the second. The outputs from the second are connected to the cascade inputs of the third, and so on. Each CSM in the chain can be programmed to do either of these 3 things:

1. Pass the samples on its cascade inputs straight through to its outputs.
2. Ignore the samples on its cascade inputs and only output the samples it generated.
3. Sum the samples it generates with the samples on its cascade inputs.

The transmit summer adds a parity bit to the output samples and can also do parity checks on the cascade input samples. If the samples fail the parity check, the transmit summer can automatically ignore those samples.

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INPUT / OUTPUT SIGNALS

Figure 3 shows the functions provided by the CSM1.5's pins, and the size of its 100-pin TQFP package. Table 1 provides descriptions of the pin functions.

Figure 3. Q5165 Cell Site Modem 100-pin Functional Diagram

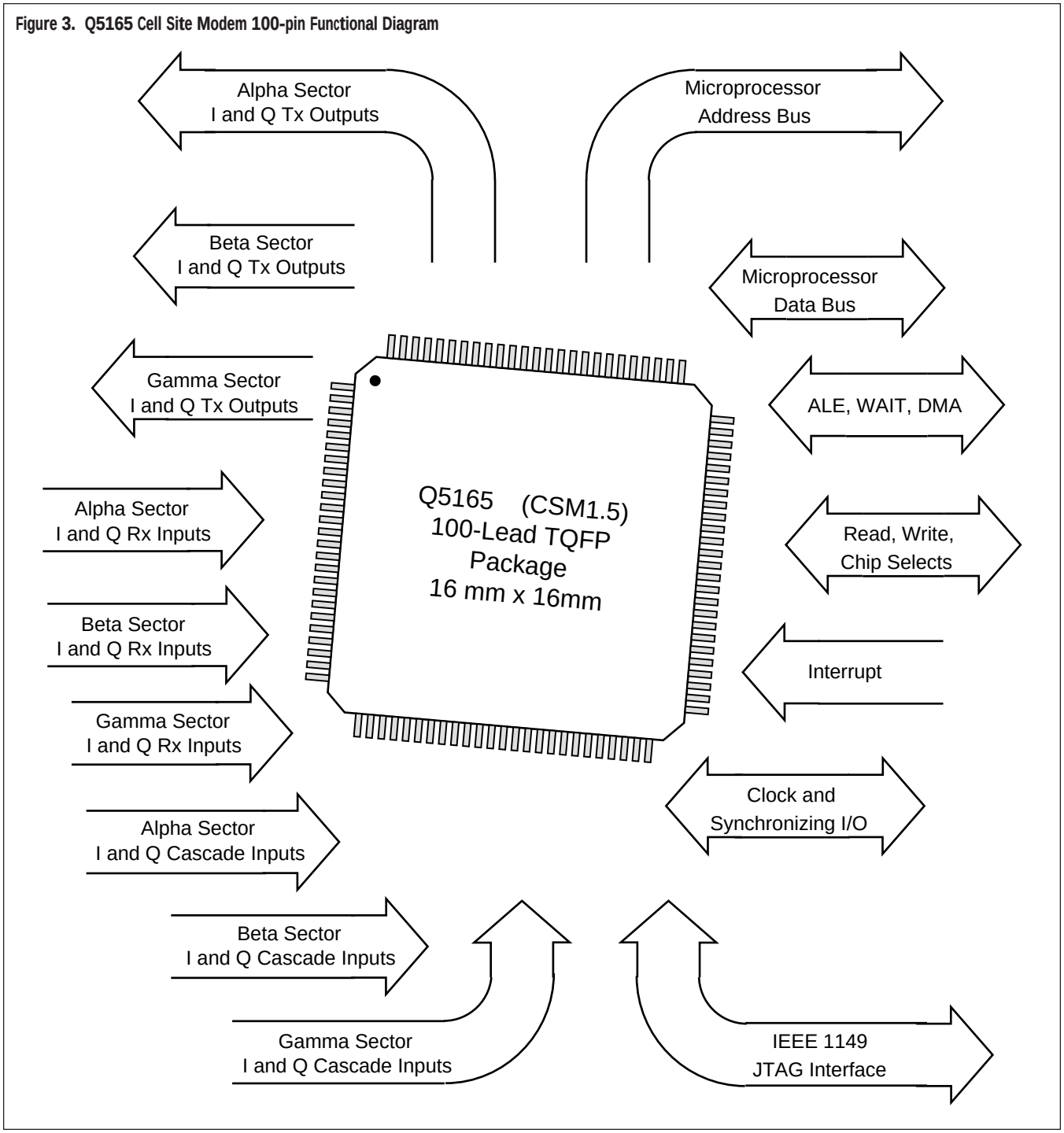

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Table 1. CSM1.5 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Microprocessor Address Bus	The CSM1.5 relies upon external microprocessors for initializations and control of operation.
Microprocessor Data Bus	
ALE, WAIT, DMA, Interrupt	
Read, Write, Chip Select	
Clock and Synchronizing I/O	Controls for operating and synchronizing the CSM1.5 chip with system timing and other CSM1.5 chips in the base station.
IEEE 1149 JTAG Interface	A full JTAG interface conforming with IEEE 1149 standard is available for test and debug of subscriber unit subassemblies.
Alpha, Beta and Gamma Sector I and Q Rx Inputs	Receive I and Q digital baseband data inputs from three sectors.
Alpha, Beta and Gamma Sector I and Q Tx Outputs	Transmit I and Q digital baseband data outputs for three sectors.
Alpha, Beta and Gamma Sector I and Q Cascade Inputs	Additional I and Q digital baseband data from other CSM1.5 chips is summed into the transmit signal path via these inputs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2 provides the absolute maximum ratings for the Q5165 CSM1.5. Table 3 shows the recommended operating range conditions of the CSM1.5. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_S	Storage Temperature	-65	150	°C
T_J	Junction Temperature	–	150	°C
V_I	Voltage on any INPUT or OUTPUT Pin	-0.3	V_{DD} + 0.3	°C
V_{DD}	Supply Voltage	-0.5	4.6	V

Table 3. Operating Range

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}	Supply Voltage	2.7	3.6	°V
T_A	Operating Temperature	-40	85	°C

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ELECTRICAL CHARACTERISTICS

Table 4 provides the electrical characteristics of the CSM1.5.

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	High-Level INPUT Voltage	$V_{DD} \times 0.65$	–	$V_{DD} + 0.3$	V	1
V_{IL}	Low-Level INPUT Voltage	-0.3	–	$V_{DD} \times 0.35$	V	1
V_{OH}	High-Level OUTPUT Voltage	V_{DD} - 0.45	–	V_{DD}	V	2
V_{OL}	Low-Level OUTPUT Voltage	–	–	0.45	V	2
I_{IH}	INPUT High Leakage Current	-1	–	1	µA	3
I_{IL}	INPUT Low Leakage Current	-1	–	1	µA	3
I_{IHPD}	INPUT High Leakage Current, Pull-Down	10	–	60	µA	4
I_{ILPU}	INPUT Low Leakage Current, Pull-Up	-60	–	-10	µA	5
C_{IN}	INPUT Capacitance	–	6.2	–	pF	–

Notes:

1. The device is sensitive to overshoot and undershoot. The INPUT signal must be within the specified limits to guarantee reliable operation.
2. These parameters are specified under the maximum allowable OUTPUT current ratings.
3. This parameter is measured with $0<V_{IN}<V_{DD}$.
4. This parameter is measured with input = V_{DD} and $V_{DD} = V_{DD}$ max.
5. This parameter is measured with input = V_{SS} and $V_{DD} = V_{DD}$ max.

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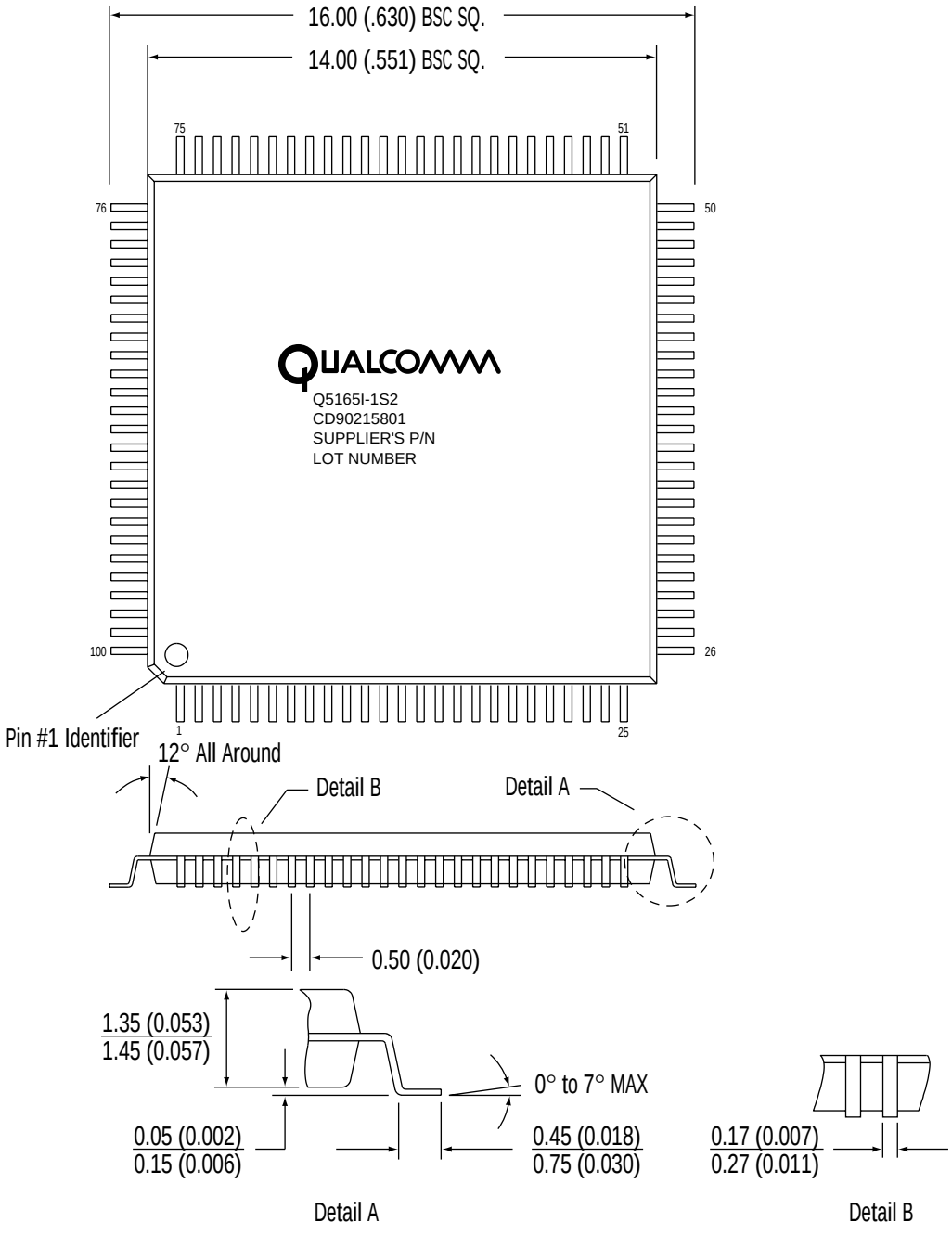
PACKAGING AND MARKING

The Q5165 CSM 1.5 is available in a 100-pin TQFP package shown in Figure 4.

Figure 4. Q5165 CSM 100-pin TQFP Package Outline



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CSM2000

CELL SITE MODEM

Preliminary Data

OVERVIEW

The CSM2000, developed by QUALCOMM Incorporated, is a CDMA digital baseband modem capable of supporting up to eight Forward Link channels and eight Reverse Link channels. QUALCOMM's previous generation of Cell Site Modems (CSM), the CSM1.0 and CSM1.5, could support only one Forward Link channel and one Reverse Link channel per device.

The CSM2000 provides QUALCOMM's CDMA licensees with an IS-95A compliant system capable of supporting both 9.6 kbps and 14.4 kbps channels. The CSM2000 is made up of eight integrated Channel Elements. Each Channel Element is accessed as if it were a single CSM1.0 or CSM1.5. This allows the CSM2000 to be controlled by software written for the CSM1.0 or CSM1.5 with only minor changes.

Figure 1. Block Diagram of the CSM2000

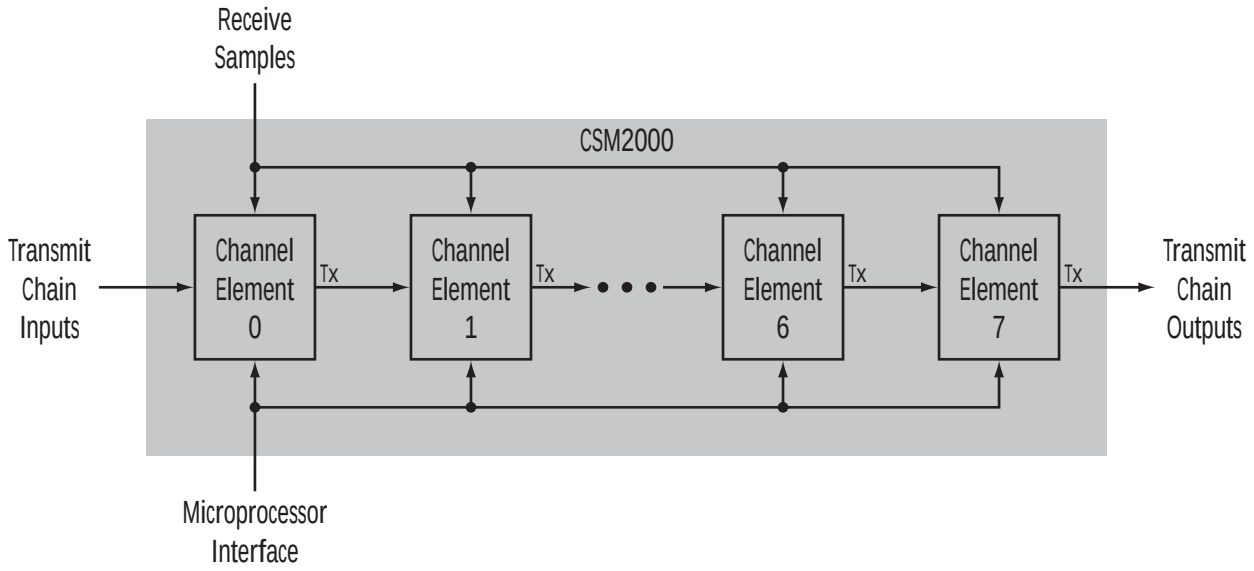

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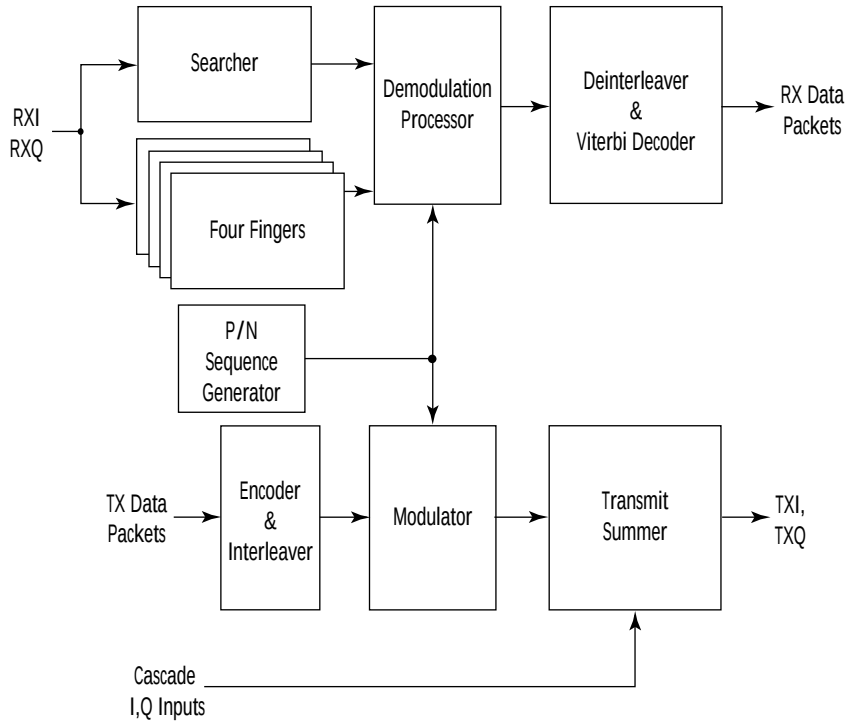
Figure 2. CSM2000 Channel Element Block Diagram



PERFORMANCE

The high integration of the CSM2000 allows a substantial savings in power consumption. The CSM2000 provides more than 75% power savings when replacing eight CSM1.0s and more than 25% power savings when replacing eight CSM1.5s. Improvements in the Demodulator of the CSM2000 provide up to 1.2 dB of improvement over the CSM1.0 and CSM1.5. This reduces the output power required from the mobile unit, resulting in improved Reverse Link system capacity and increased battery life in the mobile unit.

CHANNEL ELEMENT FUNCTIONAL OVERVIEW

SEARCHER

After selecting an antenna set for a search and programming the position and size of the search window, the searcher initiates the search and finds the largest multipath peaks within the search parameter set. Normally, the searcher operates continuously; while the results from a search are read, the next search is already underway. For acquisition searches, the searcher results can be used to detect the presence of a mobile attempting to access the CDMA network. For demodulator multipath searches, fingers may be assigned to the reported paths to improve the demodulator performance of the rake receiver.

FOUR FINGERS

The four fingers make up a front end interface to the demodulator. The fingers provide timing, Walsh chip accumulation and Walsh chip storage for the demodulation process. The fingers may be programmed to accept data from the same or differing antenna sources.

DEMODULATION PROCESSOR

The demodulation processor performs Fast Hadamard Transforms for the searcher and the four fingers. It also performs optimal soft combining of data from the fingers and performs power calculations, including lock detection and power control decisions.

DEINTERLEAVER & VITERBI DECODER

The deinterleaver is used to reverse the interleaving performed by the mobile unit. Interleaving provides protection against burst errors and fades.

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The Viterbi decoder, using the Viterbi algorithm, optimally decodes the convolutional coding from the mobile unit. Quality bits and Cyclic Redundancy Check (CRC) bits are used to verify the quality of the decoded data.

PN SEQUENCE GENERATORS

There are several Psuedorandom Noise (PN) generators within the CSM. The PN sequences generated are the I channel, Q channel and long code sequences for both forward and reverse link processing.

ENCODER & INTERLEAVER

The encoder takes forward link data frames, convolutionally encodes them and performs symbol repetition for bit rates less than full rate. The encoder also automatically generates CRCs for the frames that require them.

The interleaver is used to provide time diversity in transmitted symbols, thereby providing protection from relatively long transmission fades and burst errors. The effects of the interleaver are reversed in the mobile unit deinterleaver.

MODULATOR

The modulator contains three individually programmable sections that generate forward link information streams from the interleaver output. The symbols from the interleaver are scrambled with the long code PN sequence and punctured with power control bits, if appropriate. The punctured symbols are covered with the proper Walsh code and spread with the I and Q PN sequences. The resulting chips are then bandlimited with FIR filters and multiplied by a programmable gain factor. Each of the three transmit sectors can be driven by a particular section of the modulator, the sum of all three sections or zero.

TRANSMIT SUMMER

The transmit summer of each Channel Element combines its outputs with the outputs of the previous Channel Element and passes the result to the next Channel Element. Channel Element 0 recieves its inputs from the CSM2000 pins, and Channel Element 7 sends its result to the CSM2000 pins. This allows the transmit chains of several CSM2000s to be tied together. Each Channel Element in the chain can be programmed to do any one of these three things:

1. Pass the samples on its cascade inputs straight through to its outputs
2. Ignore the samples on its cascade inputs and only output the samples it generated
3. Sum the samples it generates with the samples on its cascade inputs

The transmit summer adds a parity bit to the output samples and can also do parity checks on the cascade input samples. If the samples fail the parity check, the transmit summer can automatically ignore those samples.

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INPUT / OUTPUT SIGNALS

Figure 3 shows the functions provided by the CSM2000's pins, and the size of its 128-pin MQFP package. Table 1 provides descriptions of the pin functions.

Figure 3. CSM2000 128-pin Functional Diagram

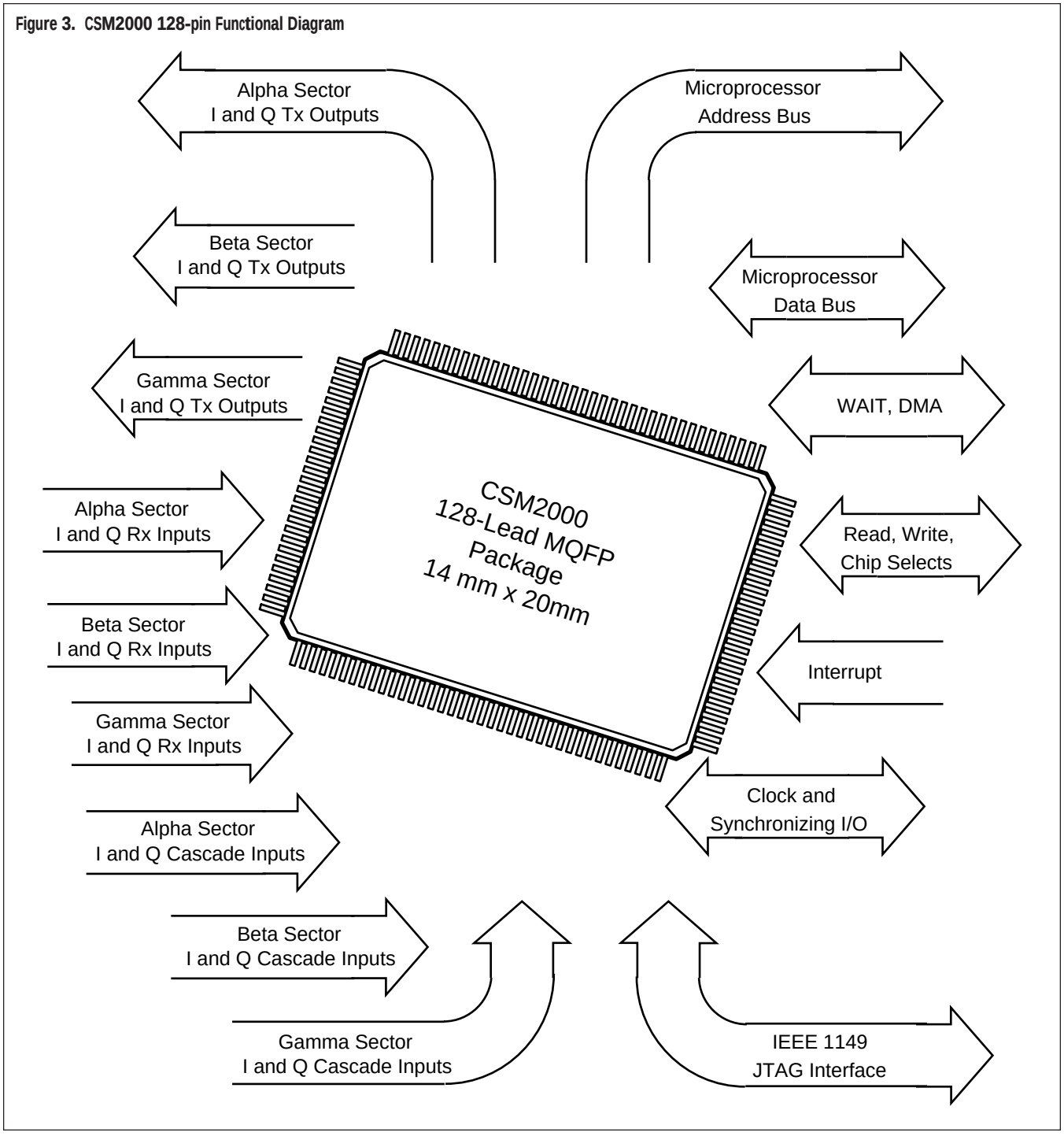

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Table 1. CSM2000 Pin Functions

PIN FUNCTIONS	DESCRIPTION
Microprocessor Address Bus	The CSM2000 relies upon an external microprocessor for initialization and control of operation.
Microprocessor Data Bus	
WAIT, DMA, Interrupt	
Read, Write, Chip Select	
Clock and Synchronizing I/O	Controls for operating and synchronizing the CSM2000 chip with system timing and other CSM2000 chips in the base station.
IEEE 1149 JTAG Interface	A full JTAG interface conforming with IEEE 1149 standard is available for test and debug of subscriber unit subassemblies.
Alpha, Beta and Gamma Sector I and Q Rx Inputs	Receive I and Q digital baseband data inputs from three sectors.
Alpha, Beta and Gamma Sector I and Q Tx Outputs	Transmit I and Q digital baseband data outputs for three sectors.
Alpha, Beta and Gamma Sector I and Q Cascade Inputs	Additional I and Q digital baseband data from other CSM2000 chips is summed into the transmit signal path via these inputs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 2 provides the absolute maximum ratings for the CSM2000. Table 3 shows the recommended operating range conditions of the CSM2000. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS
T_S	Storage Temperature	-65	150	°C
T_J	Junction Temperature	–	150	°C
V_I	Voltage on any INPUT or OUTPUT Pin	-0.3	V_{DD} + 0.3	°C
V_{DD}	Supply Voltage	-0.5	4.6	V

Table 3. Operating Range

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DD}	Supply Voltage	2.7	3.6	°V
T_A	Operating Temperature	-40	85	°C

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ELECTRICAL CHARACTERISTICS

Table 4 provides the electrical characteristics of the CSM2000.

Table 4. Electrical Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{IH}	High-Level INPUT Voltage	$V_{DD} \times 0.65$	–	$V_{DD} + 0.3$	V	1
V_{IL}	Low-Level INPUT Voltage	-0.3	–	$V_{DD} \times 0.35$	V	1
V_{OH}	High-Level OUTPUT Voltage	V_{DD} - 0.45	–	V_{DD}	V	2
V_{OL}	Low-Level OUTPUT Voltage	–	–	0.45	V	2
I_{IH}	INPUT High Leakage Current	-1	–	1	µA	3
I_{IL}	INPUT Low Leakage Current	-1	–	1	µA	3
I_{IHPD}	INPUT High Leakage Current, Pull-Down	10	–	60	µA	4
I_{ILPU}	INPUT Low Leakage Current, Pull-Up	-60	–	-10	µA	5
C_{IN}	INPUT Capacitance	–	6.2	–	pF	–

Notes:

1. The device is sensitive to overshoot and undershoot. The INPUT signal must be within the specified limits to guarantee reliable operation.
2. These parameters are specified under the maximum allowable OUTPUT current ratings.
3. This parameter is measured with $0<V_{IN}<V_{DD}$.
4. This parameter is measured with input = V_{DD} and $V_{DD} = V_{DD}$ max.
5. This parameter is measured with input = V_{SS} and $V_{DD} = V_{DD}$ max.

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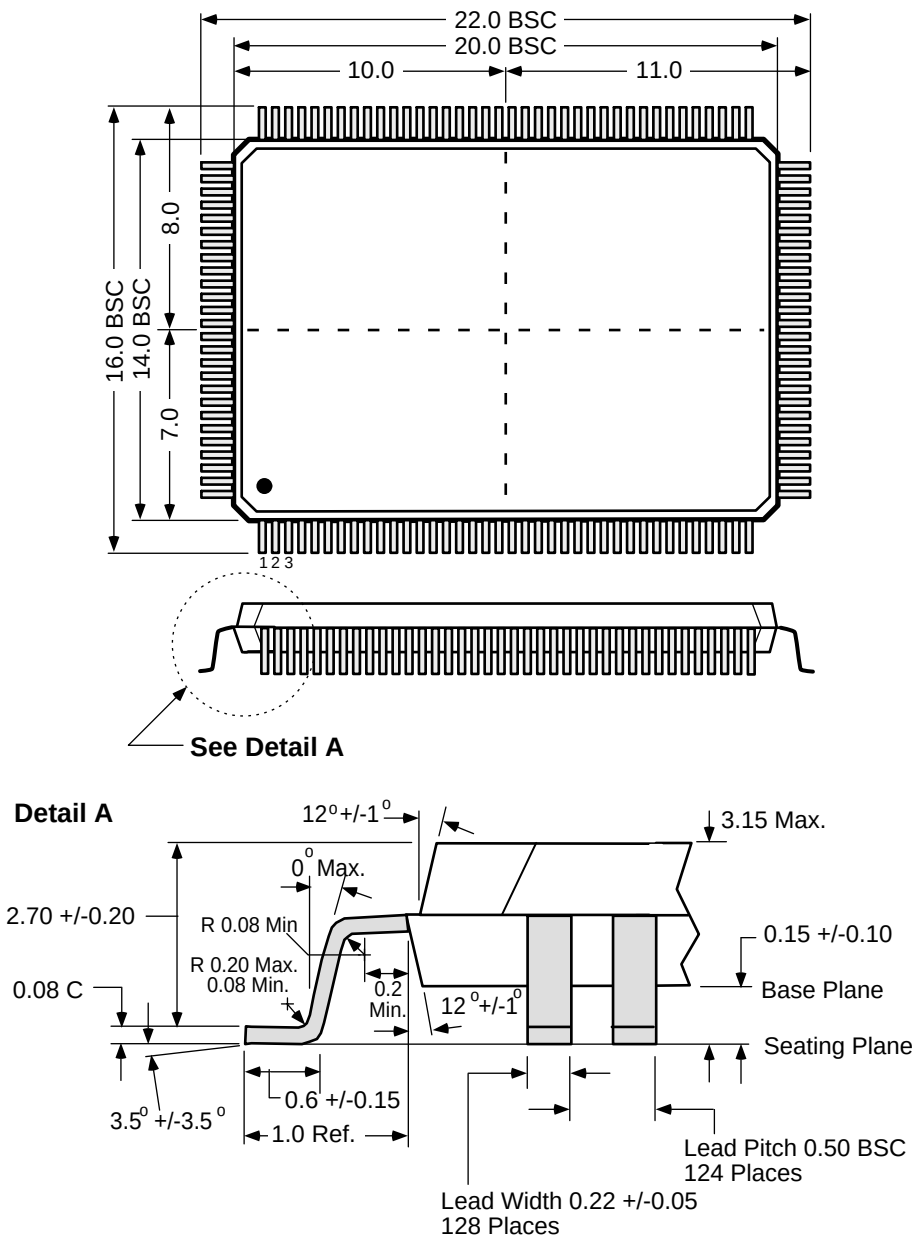
PACKAGING AND MARKING

The CSM2000 is available in a 128-pin MQFP package shown in Figure 4.

Figure 4. CSM2000 128-pin MQFP Package Outline



(All dimensions in millimeters)

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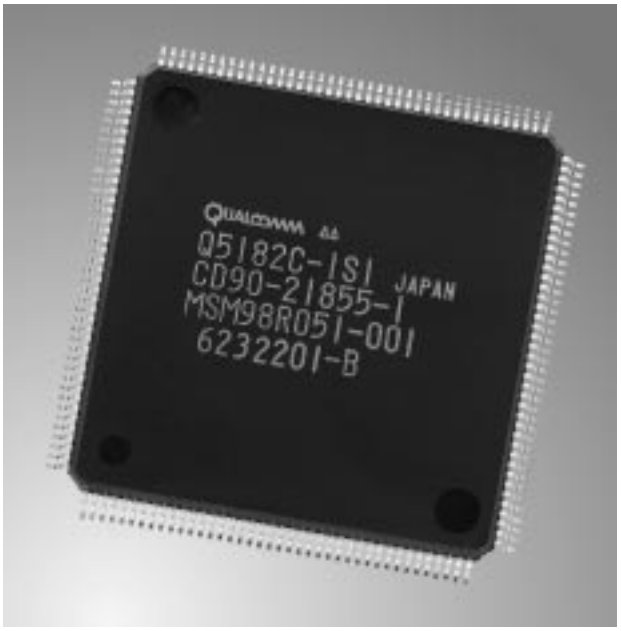
Q5182

FRAME INTERFACE AND ROUTER MODULE FIRM ASIC



OVERVIEW

Various components of the QUALCOMM base station communicate via the Base Station Communication Network (the BCN). The link layer protocol of the BCN uses frames that are similar to HDLC frames (defined by CCITT Q.921) but are constrained in length to a range of 8 to 47 bytes. The Frame Interface and Router Module (FIRM) ASIC provides a highly integrated solution to the task of routing these frames and providing a rate adaptation and buffering capability for them.

FUNCTIONAL DESCRIPTION

Figure 1 illustrates the BCN frame format. The full Address field is used to specify the frame destination, while the Control field contains only a single 2-bit subfield of interest to the FIRM. This subfield specifies a Frame Loss Priority (FLP) value of 0, 1, 2 or 3 for the frame. When heavy traffic threatens to overflow its frame buffers, the FIRM can selectively discard incoming frames with higher FLP values. The Payload field may vary in length from two through 41 bytes to accommodate traffic demand, while the two-byte

Figure 1. BCN Frame Format

ADDRESS FIELD	CONTROL FIELD	PAYLOAD FIELD	FCS FIELD
3 Bytes	1 Byte	2 to 41 Bytes	2 Bytes

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Frame Check Sum (FCS) field protects the entire frame.

The FIRM has two 1-bit serial input ports and two 1-bit serial output ports. Each of these include data and clock pins, utilizing the data format defined by CCITT Q.921. The FIRM also has two 8-bit parallel input ports and two 8-bit parallel output ports with a similar data format except that the data is not bit-stuffed, and frame boundaries are demarked by additional signals rather than by sync flags in the data stream.

Most frequently, a serial input and a serial output port are paired to create a full duplex serial port. Meanwhile, a parallel input port and a parallel output port are paired to create a full duplex parallel port. The two full duplex ports thus formed are then connected through buffers to provide a full duplex path between the serial and parallel ports. The FIRM supports two such full duplex paths.

With this configuration, BCN frames arriving at a parallel input port are subject to address filtering (plus various error checks), and those that pass are put into a buffer; other frames are discarded. Each whole frame is then driven onto the serial output port at a rate determined by its clock line.

In the opposite direction, BCN frames arriving at a serial input port are also subject to address filtering (plus various error checks) and those that pass are put into another buffer. When at least one whole frame has been accumulated, a request is made for the bus connected to the parallel output port. When a grant is received, one frame is driven onto the parallel output port at a high rate of speed, relative to the speed of the serial ports.

The FIRM data paths can be configured in other ways as well. For example a parallel input port can be connected through a buffer to a parallel output port.

The FIRM has a microprocessor interface with an 8-bit wide data port and a separate address port. The microprocessor interface is used to configure the FIRM. For example:

- Set up specific BCN paths through the FIRM
- Set the address filter parameters for each BCN path through the FIRM
- Specify the clock source to be used for each serial port
- Specify which events will activate the interrupt line
- Read registers reporting errors and performance data

In addition, BCN data can be inserted through the microprocessor interface to any of the path buffers. This data is then driven onto the output port connected to the buffer. Similarly, the contents of any of the path buffers can be extracted through the microprocessor port, thus obtaining the data stream from the input port connected to that buffer.

FEATURES

- Maximum frequency of main array clock: 20 MHz
- Maximum speed of each parallel port: One byte per cycle of main array clock
- Maximum speed of each serial port: 17 Mbps
- Maximum speed of microprocessor port: One byte per 4 cycles of main array clock
- IEEE 1149.1 Test Access Port for boundary scan
- Four general purpose I/O pins
- Package: 160 pin PQFP
- Core power requirement: 3.0 V to 3.6 V
- I/O power requirement: 3.0 V to 5.25 V
- Power dissipation: 1.2 W at maximum frequency

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TECHNICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 1 shows the absolute maximum ratings and Table 2 shows the operating ranges of the Q5182 FIRM ASIC. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_{STG}	Storage Temperature	-65	+150	°C	–
V_I	Voltage on any INPUT Pin	-0.3	V_{DDO} + 0.3	V	–
V_O	Voltage on any OUTPUT Pin	-0.3	V_{DDO} + 0.3	V	–
V_{DDC}	Power Supply Voltage for Core Logic	-0.3	+4.6	V	–
V_{DDO}	Power Supply Voltage for I/O Buffers	-0.5	+6.5	V	–
I_I	INPUT Current	-10	+10	mA	–
I_O	OUTPUT Current per I/O	-25	+25	mA	1
V_{ESD}	I/O Electrostatic Discharge Protection	-2000	+2000	V	2
I_{TRIG}	I/O Latch-Up Trigger Current Protection	-200	+200	mA	3

Notes:

1. These values apply to both 4 mA and 8 mA output drivers. Also they apply to to both when V_{DDO} = 3.3 V or when V_{DDO} = 5 V.
2. Method meets the intent of MIL-STD-883, method 3015.
3. Method meets the intent of JEDEC STD 17 publication. This is the maximum allowable current flow through the input and output protection devices.

Table 2. Operating Range

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{DDC}	Supply Voltage for Core Logic	3.0	3.6	V
V_{DDO}	Supply Voltage for I/O Buffers	3.0	5.25	V
V_{DDPRE}	Supply Voltage to I/O Translators	3.0	5.25	V
T_A	Ambient Operating Temperature	0	+70	°C
θ_{JA}	Package Thermal Impedance in Still Air	–	60	°C/W

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DC ELECTRICAL CHARACTERISTICS

Table 3 shows the DC electrical characteristics for the Q5182 FIRM ASIC.

Table 3. DC Electrical Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{IH}	High-Level Input Voltage. TTL Input. V_{DD} = 3.0 ~ 3.6 V.	2.0	V_{DD} + 0.3	V
	High-Level Input Voltage. TTL Input. V_{DD} = 4.5 ~ 5.5 V.	2.2	V_{DD} + 0.5	V
V_{IL}	Low-Level Input Voltage. TTL Input. V_{DD} = 3.0 ~ 3.6 V.	-0.3	0.8	V
	Low-Level Input Voltage. TTL Input. V_{DD} = 4.5 ~ 5.5 V.	-0.5	0.8	V
V_{t+}	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 3.0 ~ 3.6 V.	–	2.0	V
	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 4.5 ~ 5.5 V.	–	2.2	V
V_{t-}	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 3.0 ~ 3.6 V.	0.8	–	V
	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 4.5 ~ 5.5 V.	0.8	–	V
ΔV_t (V_{t+} + V_{t-})	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 3.0 ~ 3.6 V.	0.1	–	V
	TTL-Level Schmitt Trigger Input Threshold Voltage. V_{DD} = 4.5 ~ 5.5 V.	0.2	–	V
V_{OH}	High-Level Output Voltage. I_{OH} = -4 or -8 mA. V_{DD} = 3.0 ~ 3.6 V.	2.4	–	V
	High-Level Output Voltage. I_{OH} = -4 or -8 mA. V_{DD} = 4.5 ~ 5.5 V.	3.7	–	V
V_{OL}	Low-level Output Voltage. I_{OL} = 4 or 8 mA. V_{DD} = 3.0 ~ 3.6 V.	–	0.4	V
	Low-Level Output Voltage. I_{OL} = 4 or 8 mA. V_{DD} = 4.5 ~ 5.5 V.	–	0.4	V
I_{IH}	High-Level Input Current. V_{IH} = V_{DD} = 3.0 ~ 3.6 V.	–	1	µA
	High-Level Input Current. V_{IH} = V_{DD} = 4.5 ~ 5.5 V.	–	10	µA
I_{IL}	Low-Level Input Current. V_{IL} = V_{SS}. V_{DD} = 3.0 ~ 3.6 V.	-1	–	µA
	Low-Level Input Current. V_{IL} = V_{SS}. V_{DD} = 4.5 ~ 5.5 V.	-10	–	µA
	Low-Level Input Current. V_{IL} = V_{SS} (50 kΩ Pull-Up). V_{DD} = 3.0 ~ 3.6 V.	-240	-15	µA
	Low-Level Input Current. V_{IL} = V_{SS} (50 kΩ Pull-Up). V_{DD} = 4.5 ~ 5.5 V.	-250	-20	µA
	Low-Level Input Current. V_{IL} = V_{SS} (3 kΩ Pull-Up). V_{DD} = 3.0 ~ 3.6 V.	-4	-0.25	mA
	Low-Level Input Current. V_{IL} = V_{SS} (3 kΩ Pull-Up). V_{DD} = 4.5 ~ 5.5 V.	-5	-0.5	mA
I_{OZH}	Three-State Output Leakage Current. V_{OH} = V_{DD} = 3.0 ~ 3.6 V.	–	10	µA
	Three-State Output Leakage Current. V_{OH} = V_{DD} = 4.5 ~ 5.5 V.	–	10	µA
I_{OZL}	Three-State Output Leakage Current. V_{OL} = V_{SS}. V_{DD} = 3.0 ~ 3.6 V.	-1	–	µA
	Three-State Output Leakage Current. V_{OL} = V_{SS}. V_{DD} = 4.5 ~ 5.5 V.	-10	–	µA
	Three-State Output Leakage Current. V_{OL} = V_{SS} (50 kΩ Pull-Up). V_{DD} = 3.0 ~ 3.6 V.	-240	-15	µA
	Three-State Output Leakage Current. V_{OL} = V_{SS} (50 kΩ Pull-Up). V_{DD} = 4.5 ~ 5.5 V.	-250	-20	µA
	Three-State Output Leakage Current. V_{OL} = V_{SS} (3 kΩ Pull-Up). V_{DD} = 3.0 ~ 3.6 V.	-4	-0.25	mA
	Three-State Output Leakage Current. V_{OL} = V_{SS} (3 kΩ Pull-Up). V_{DD} = 4.5 ~ 5.5 V.	-5	-0.5	mA
I_{DDQ}	Stand-By Current. Output Open. V_{IL} = V_{SS}. V_{IH} = V_{DD} = 3.0 ~ 3.6 V.	–	20	µA
	Stand-By Current. Output Open. V_{IL} = V_{SS}. V_{IH} = V_{DD} = 4.5 ~ 5.5 V.	–	20	µA

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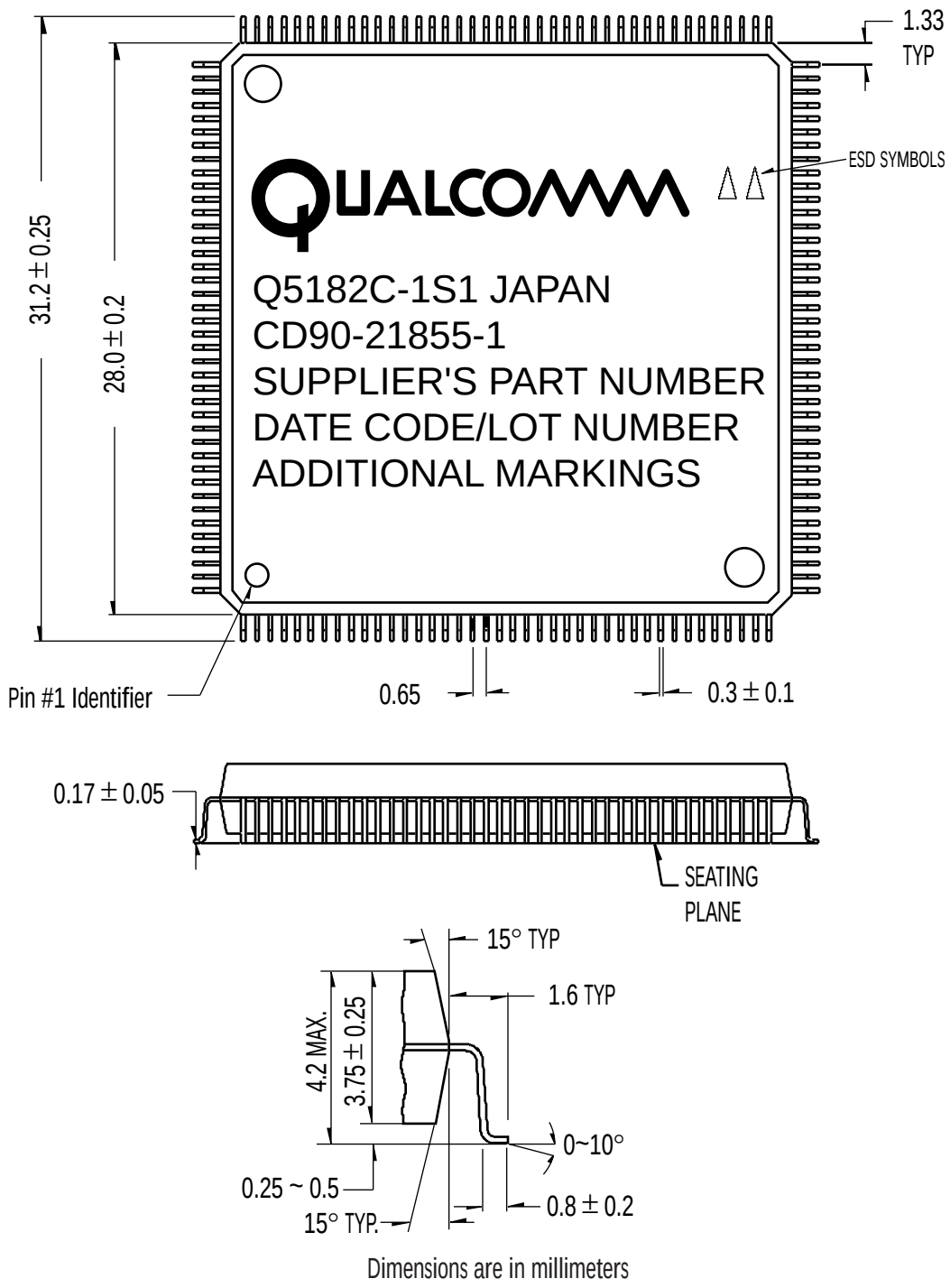
MECHANICAL AND MARKING SPECIFICATION

The Q5182 is packaged in a 160-pin Plastic Quad Flat Pack (PQFP) shown in Figure 2.

Figure 2. Q5182 FIRM ASIC 160-pin PQFP Package Outline



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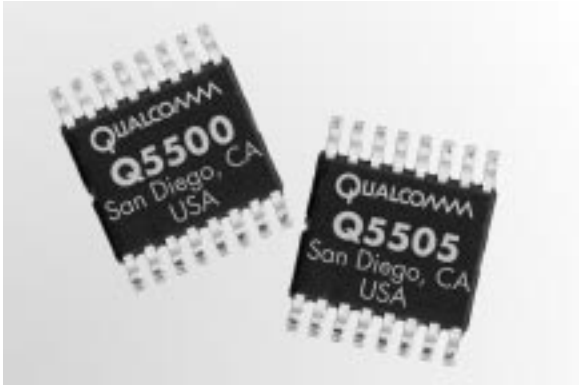
Q5500 IF RECEIVE AGC AMPLIFIER /

Q5505 IF TRANSMIT AGC AMPLIFIER



FEATURES

Q5500 FEATURES

- Supports Dual Mode Operation
- Single +3.6 V Power Supply
- Enhanced Performance over Temperature and Supply Voltage
- -45 to +45 dB Gain Control Range
- 10 MHz to 300 MHz Operation
- Low Power Consumption
- Silicon BiCMOS Process

Q5505 FEATURES

- Supports Dual Mode Operation
- Single +3.6 V Power Supply
- Enhanced Performance over Temperature and Supply Voltage
- -45 to +40 dB Gain Control Range
- 10 MHz to 250 MHz Operation
- Silicon BiCMOS Process

APPLICATIONS

- Digital Cellular Systems (dual-mode CDMA/FDM or TDMA/FDM)
- Analog Cellular Systems (AMPS, TACS)
- Analog and Digital Cordless Telephones
- Wireless Data Systems (WAN/LAN)
- Personal Communicators
- Specialized Mobile Radios (SMR)
- General Purpose Voltage-variable Linear IF Amplifier/Attenuator

GENERAL DESCRIPTION

The Q5500 Receive (Rx) and Q5505 Transmit (Tx) Variable Gain Amplifiers (VGA) are designed specifically for the receive and transmit section, respectively, of dual-mode CDMA/FM cellular applications. They provide variable gain control to IF signals with extremely wide dynamic range requirements. Noise Figure (NF), Third Order Intercept (IP3) and other specifications are designed to be compatible with the IS-95 Standard for CDMA cellular communications and remain remarkably consistent over temperature and supply voltage fluctuation. In such a dual-mode system, the Rx and Tx VGAs handle a narrowband frequency range for the IF signal processing. The Q5500 and Q5505, however, are also quite suitable for variable gain operation across a broadband frequency range. These devices can provide linear gain control for IF frequencies up to 300 MHz in general purpose Automatic Gain Control (AGC) amplifier loops. The VGAs maintain consistent NF and IP3 performance in an AGC system because these parameters exhibit low sensitivity to temperature variation. A generic system implementation for the Q5500 and Q5505 VGAs are shown in Figure 1. The differential inputs and outputs of the Q5500 and Q5505 allow a direct connection to differential downconverters/upconverters and discrete or SAW bandpass filters. Differential signals in these circuit elements reduce the effects of common-mode noise. The Q5500 and Q5505 are fabricated using a silicon BiCMOS process, operate from a single +3.6 VDC supply and come packaged in a standard 16-pin Shrink Small Outline Package (SSOP).

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Figure 1a. Generic Receive AGC Block Diagram with Q5500

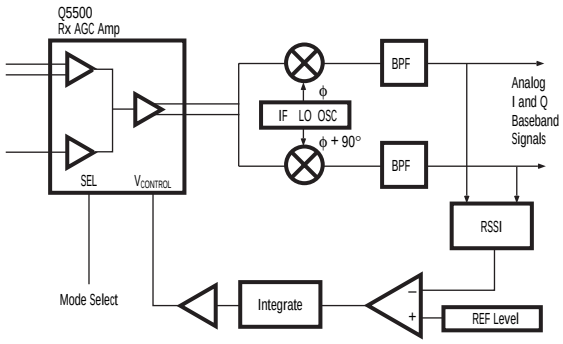
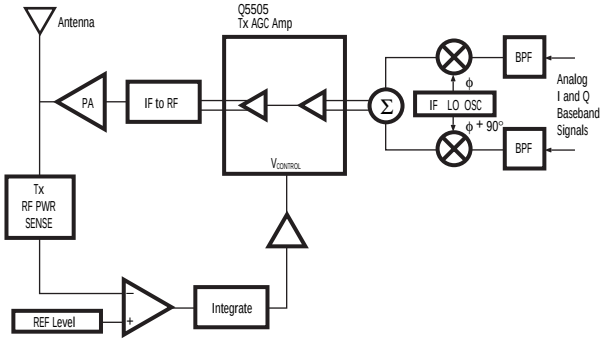


Figure 1b. Generic Transmit AGC Block Diagram with Q5505



Q5500 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent and functional damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect device reliability.

Table 1. Q5500 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T_{STO}	-55	+150	°C	
Junction Temperature	T_J	-55	+150	°C	
Supply Voltage (Relative to GND)	V_{CC}		+7.0	V	
Continuous RF Input Power			-10	dBm	
DC Voltage on any Non RF Input Pin (Relative to GND)	V_{IN}	-0.5	V_{CC} + 0.5	V	
Latchup Insensitivity	I_{TRIG}	±200		mA	1
ESD Protection	V_{ESD}	±500		V	2

NOTES:

1. Method meets the intent of JEDEC STD 17 Publication and is the maximum allowable current flow through the input and output protection diodes.
2. Method meets the intent of MIL-STD-883. Method 3015.

Table 2 Q5500 Operating Range

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature (Case)	T_C	-30	+80	°C
Operating Voltage (Relative to GND)	V_{CC}	+3.42	+3.78	V

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Table 3. Q5500 DC Electrical Parameters

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Select Input High Input Voltage	I_{CC}	3.4		V	
Select Input Low Input Voltage	V_{IL}		0.5	V	
Select Input High Input Current	V_{IH}		+100	μA	5
Select Input Low Input Current	I_{IL}	-50		μA	6
Supply Current (CDMA Mode)	I_{CC}		15	mA	
Supply Current (FM Mode)	I_{CC}		15	mA	

Table 4. Q5500 AC Electrical Parameters

PARAMETER		VALUE	NOTES
RX AGC Frequency		85.38 MHz and 210.38 MHz	
Gain Flatness (± 630 kHz)		±0.25 dB	
Gain		$V_{CONTROL}$ = 0.1 V, G< -45 dB $V_{CONTROL}$ = 3.0 V, G> 45 dB	1, 3, 6
Gain Slope		60 dB/V Maximum 20 dB/V Minimum	1, 3, 8
Gain Slope Linearity (Over any 6 dB Gain Segment)		± 3.0 dB/V	8
Gain Control Pin Input Current		< 0.1 mA @ $V_{CONTROL}$ = (0.1 - 3.0) V < 50 pF Capacitive	
NF For CDMA and FM		Figure 7a - 7f, Table 5	1, 3, 7
IIP3 For CDMA and FM		Figures 8a and 8b Respectively	1, 2, 3, 7,9
Desense (Change in Small Signal Gain)	Max Gain (G=45 dB) Input Jammer Power = -57 dBm Jammer Offset 900 kHz	FM Mode Δ G < 0.45 dB	
		CDMA Mode Δ G < 0.75 dB	
P_{1dB}	CDMA Input Min Gain (G=-45 dB)	-15.5 dBm ≤ P_{1dB}	
	FM Input (G < -27 dB)	-22.0 dBm ≤ P_{1dB}	
Isolation AGC-1 Between AGC-2		30 dB	1
CDMA Input Impedance (Differential)		1K Ω ± 15%, < 1 pF Capacitive	3
FM Input Impedance (Single Ended)		865 Ω ± 15%, < 1.5 pF Capacitive	3
Output Impedance		> 5 kΩ, < 1 pF Capacitive	3
Stability		Over Full AGC Range With Source and Load VSWR 10:1 All Angles Spurious < -70dBm	

NOTES:

1. $Z_S = Z_L$ = 250 Ω. Manufacturer to recommend Z_S and Z_L.
2. IIP3 = IMR3/2 + P_{IN}, where IIP3 is the input third order intercept, in dBm, IMR3 is the third order intermodulation product rejection in dB, and P_{IN} is the sum power of the two input tones.
3. See Figures 2a, 2b and 2c.
4. $V_{IH} = V_{CC}$ = 3.78V.
5. V_{IL} = 0V, V_{CC} = 3.78 V.
6. P_{OUT} = -57 dBm, or $P_{IN\ MAX}$ = -12 dBm if in compression.
7. Over Specified Gain Range of -45 dB to +45 dB.
8. In Linear Operating Range.
9. P_{IN} total maximum = -23 dBm, and P_{OUT} total maximum = -57 dBm.

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Figure 2a. Definition of FM Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

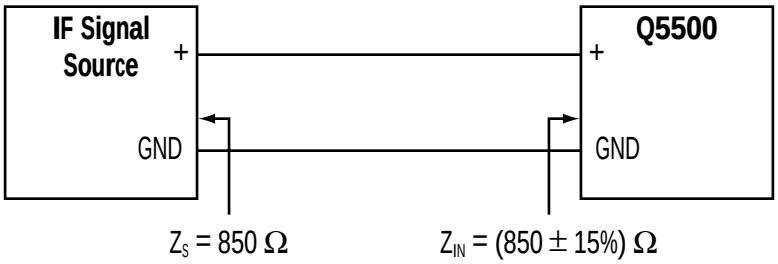


Figure 2b. Definition of CDMA Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5500

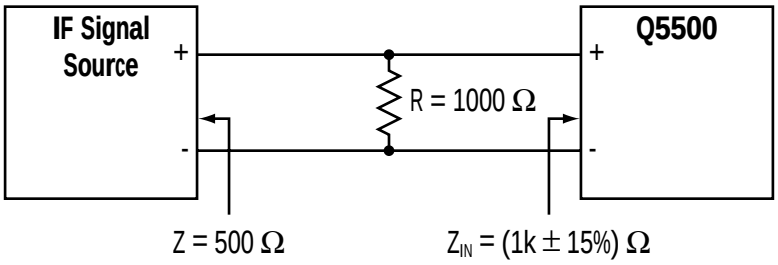
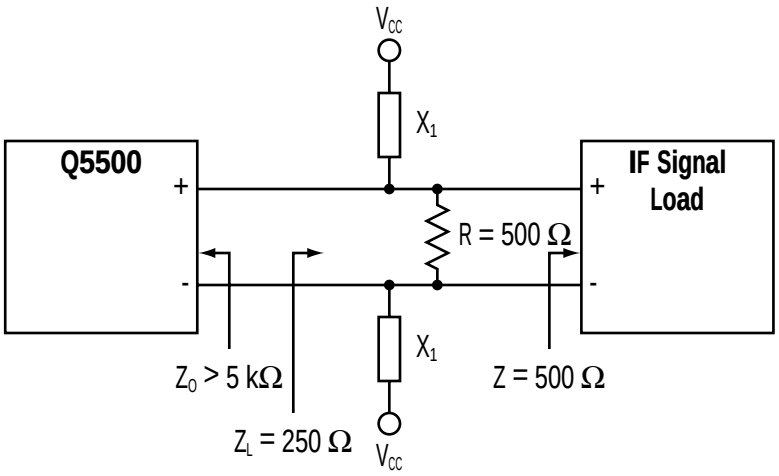


Figure 2c. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5500



Note: X_1 can be a resistor or an inductor.
If it is a resistor, X_1 = 250 Ω and the 500 Ω resistor will not be used.
If it is an inductor, L = 2.7 μH.

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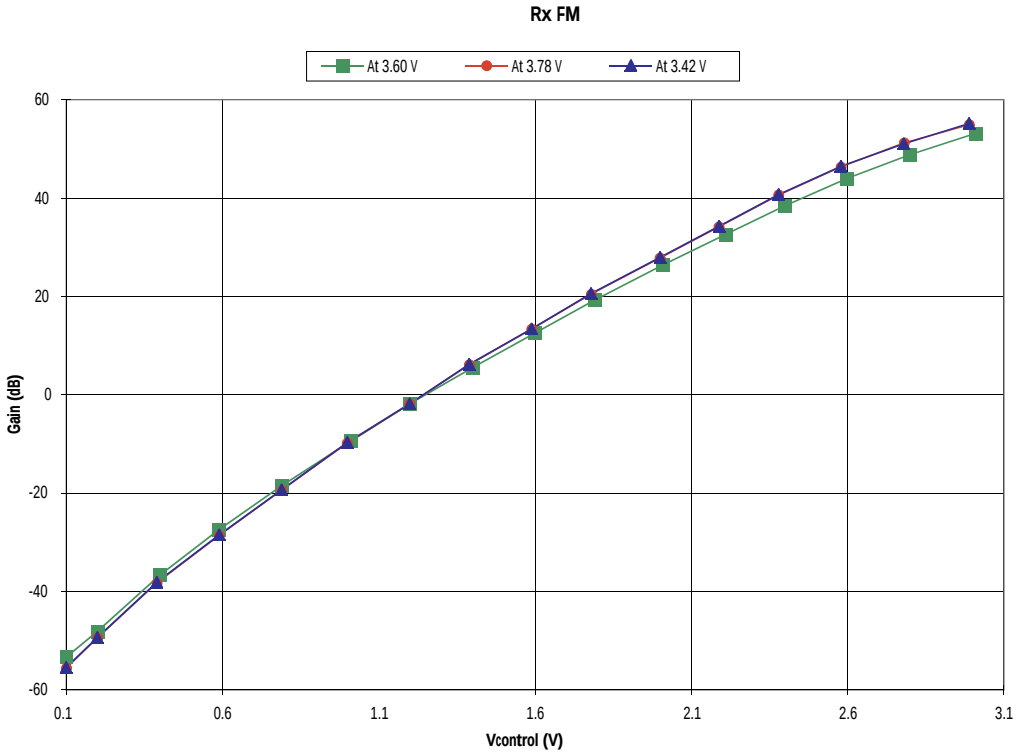
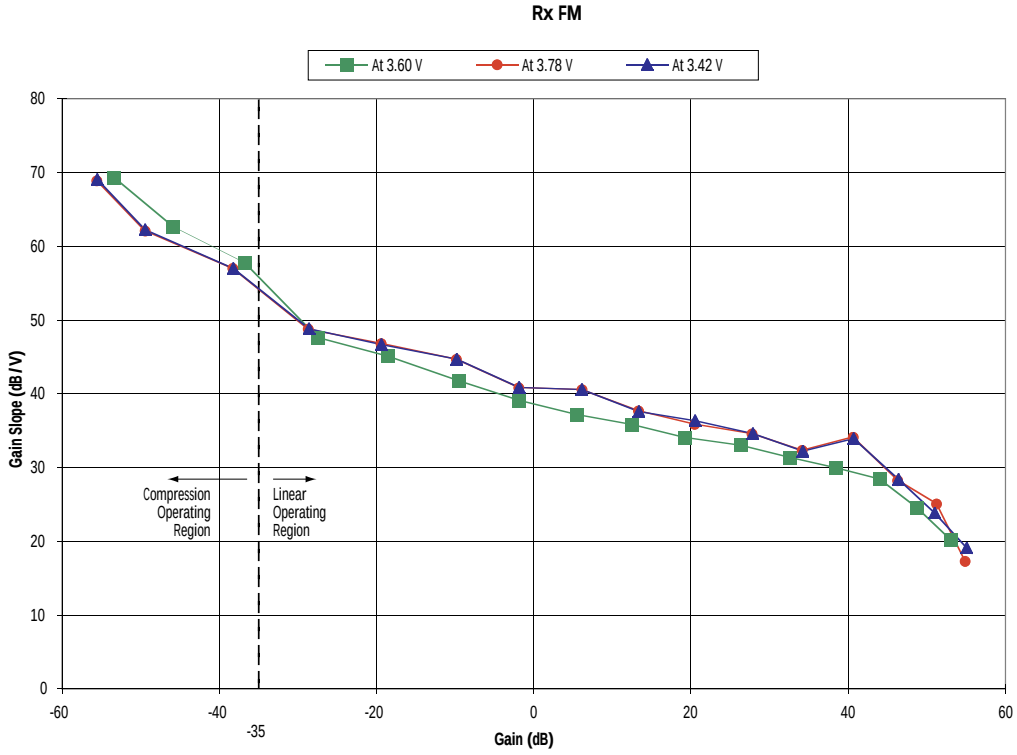
Figure 3a-e. Typical Q5500 Performance Characteristics Over Supply Voltage Range, FM Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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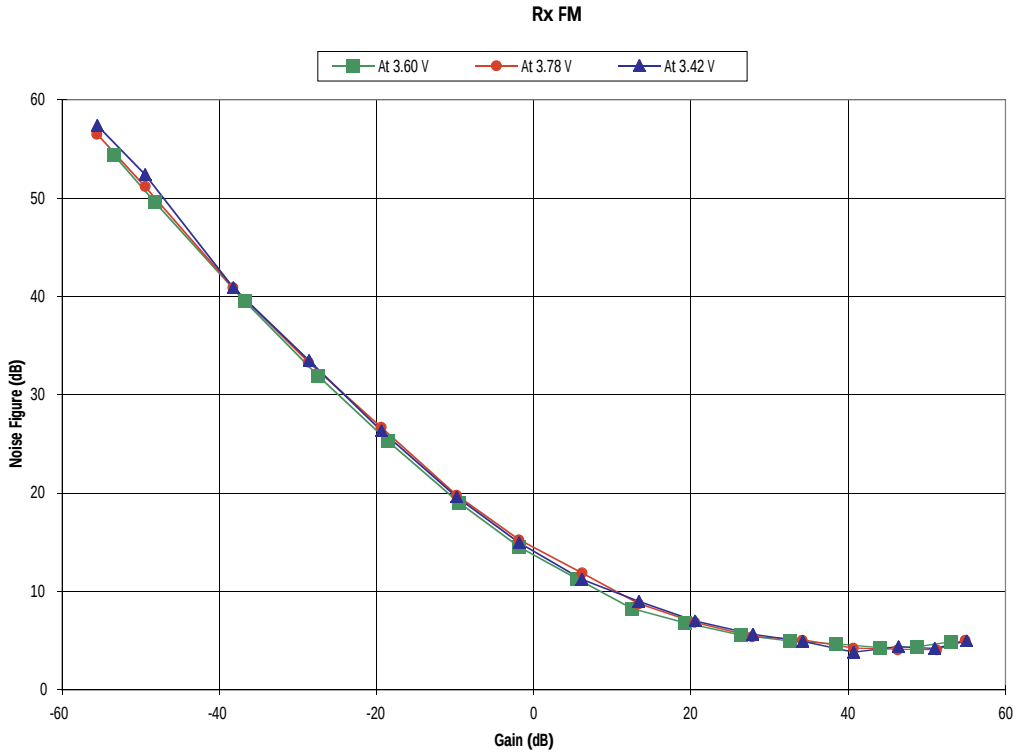
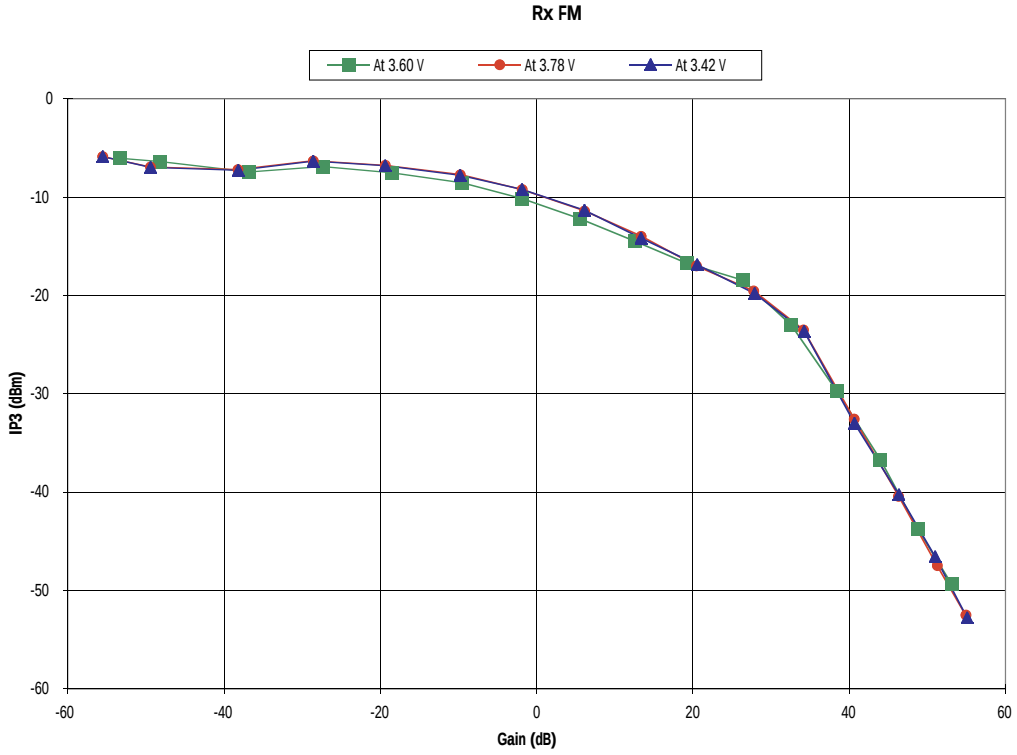


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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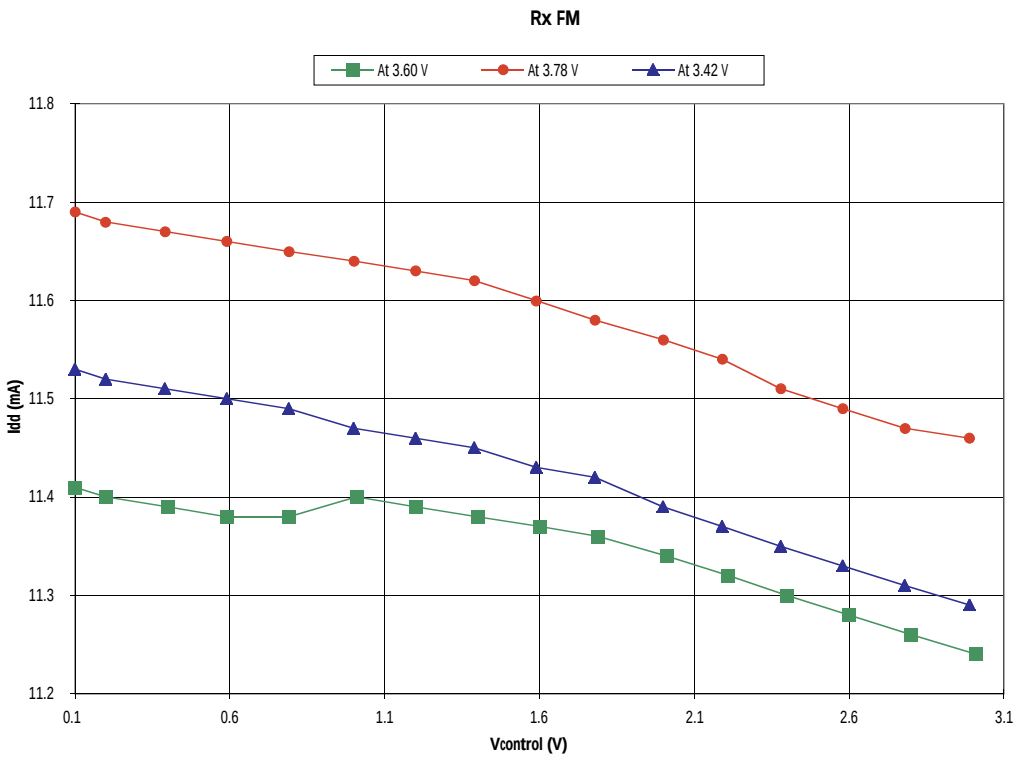

e. Supply Current vs. Control Voltage

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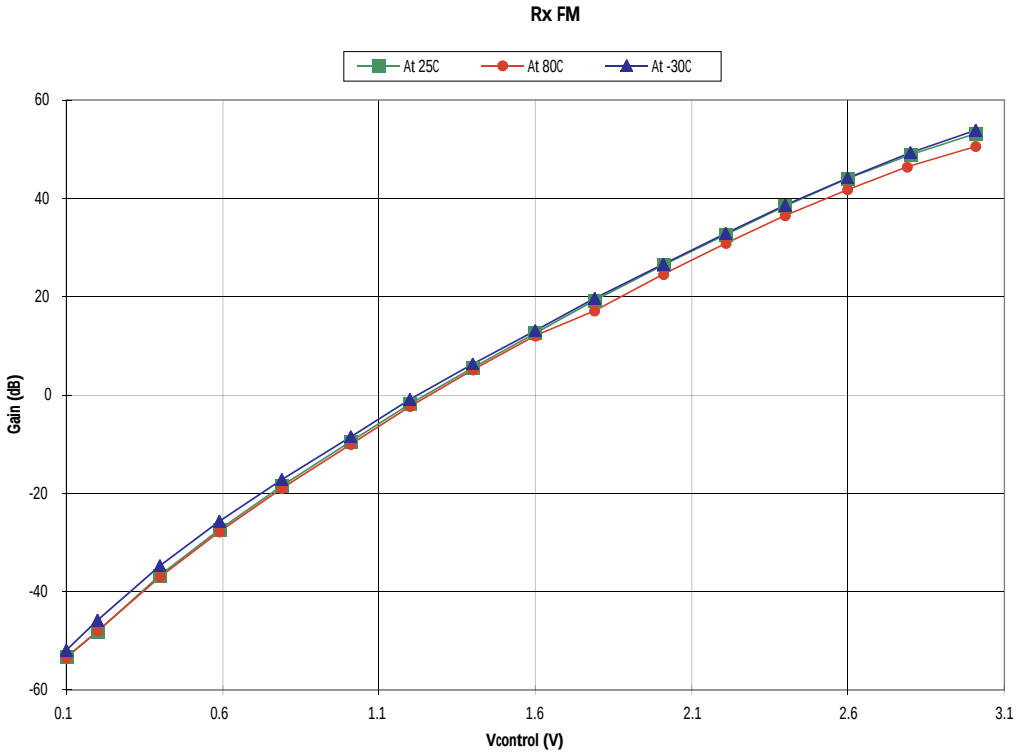
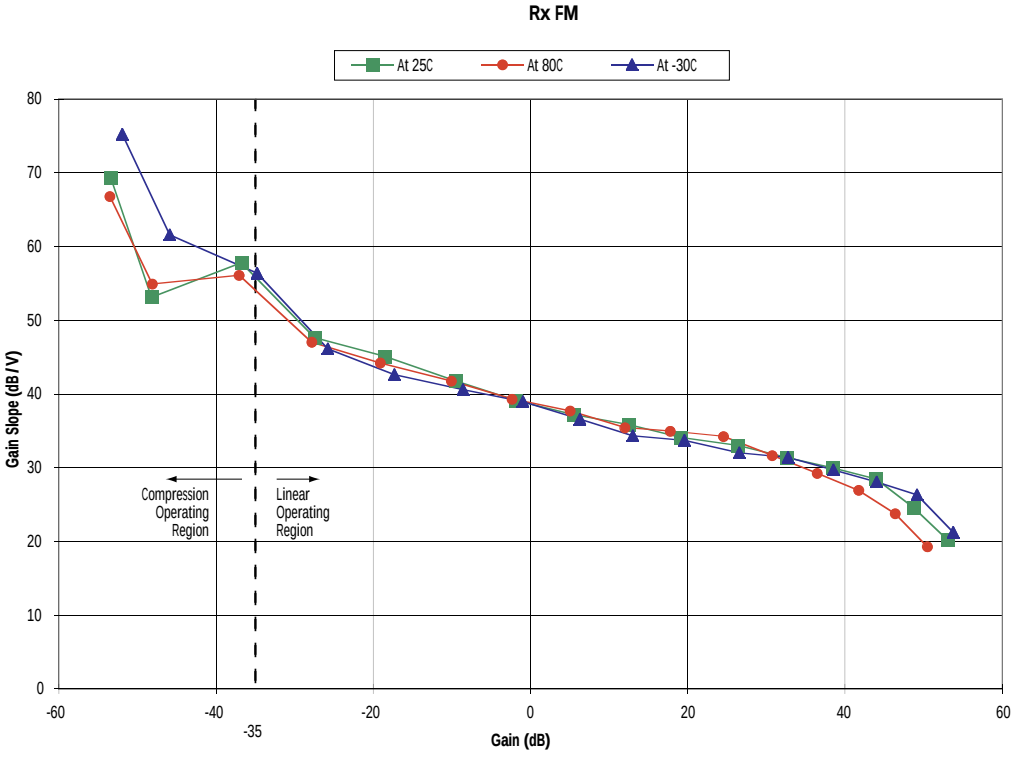
Figure 4a-e. Typical Q5500 Performance Characteristics Over Operating Temperature Range, FM Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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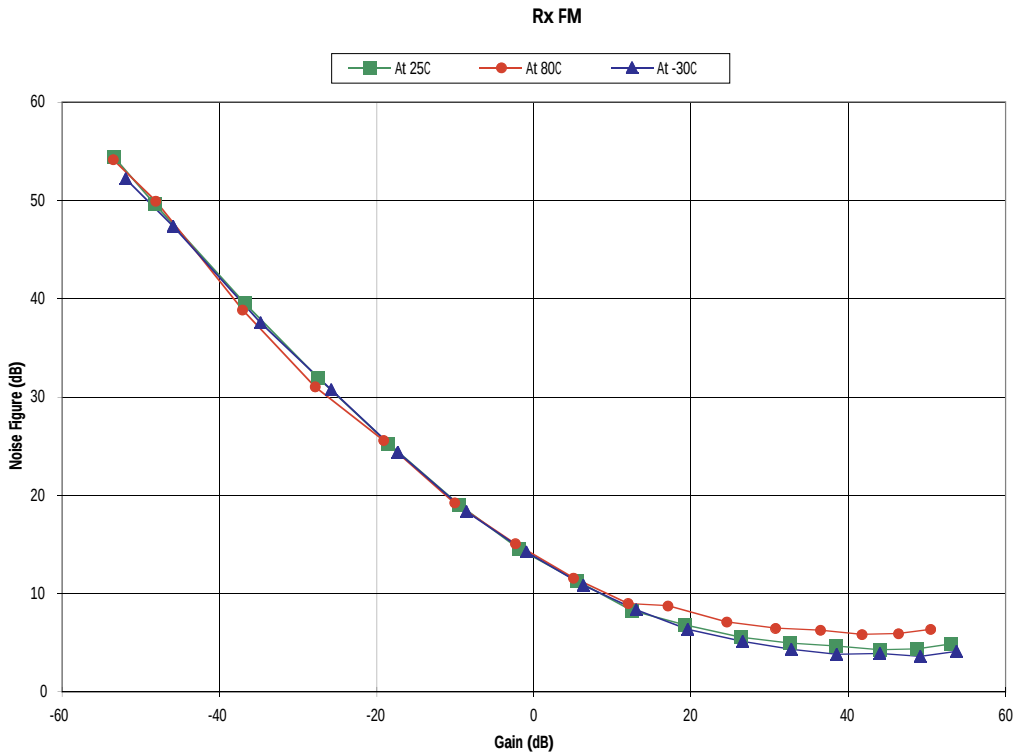
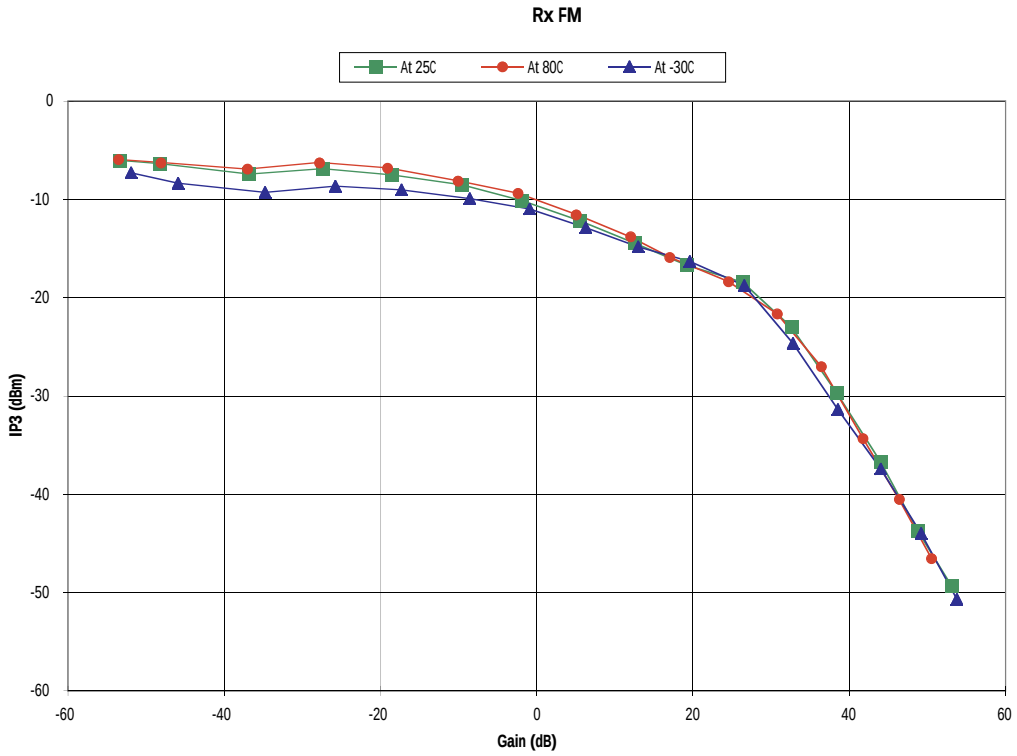


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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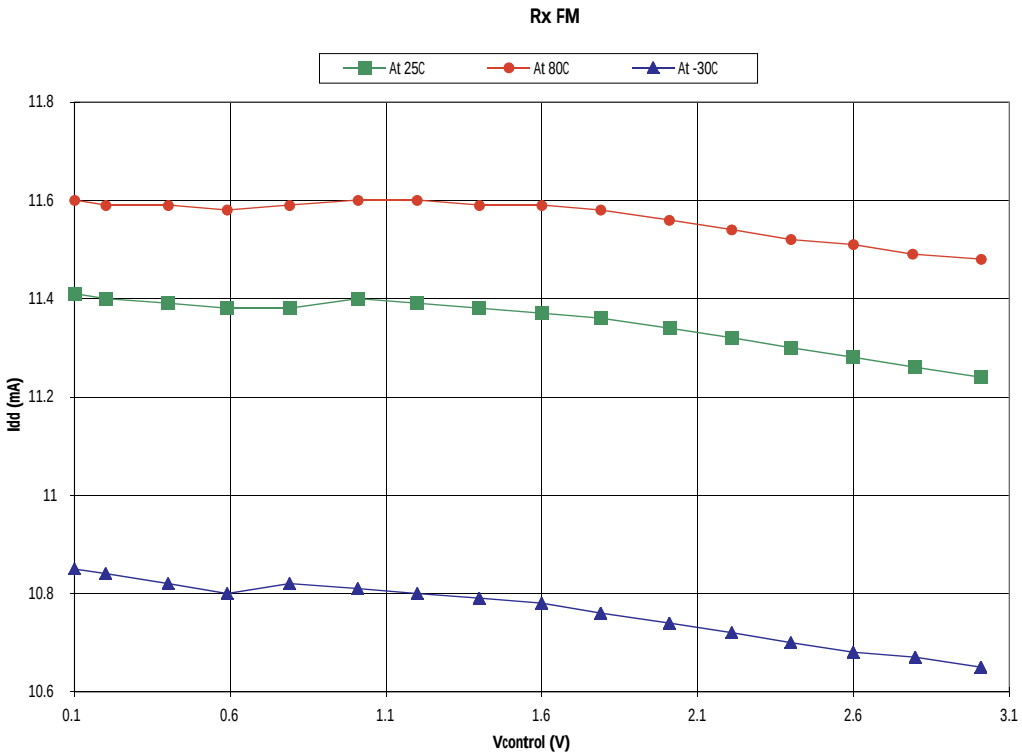

e. Supply Current vs. Control Voltage

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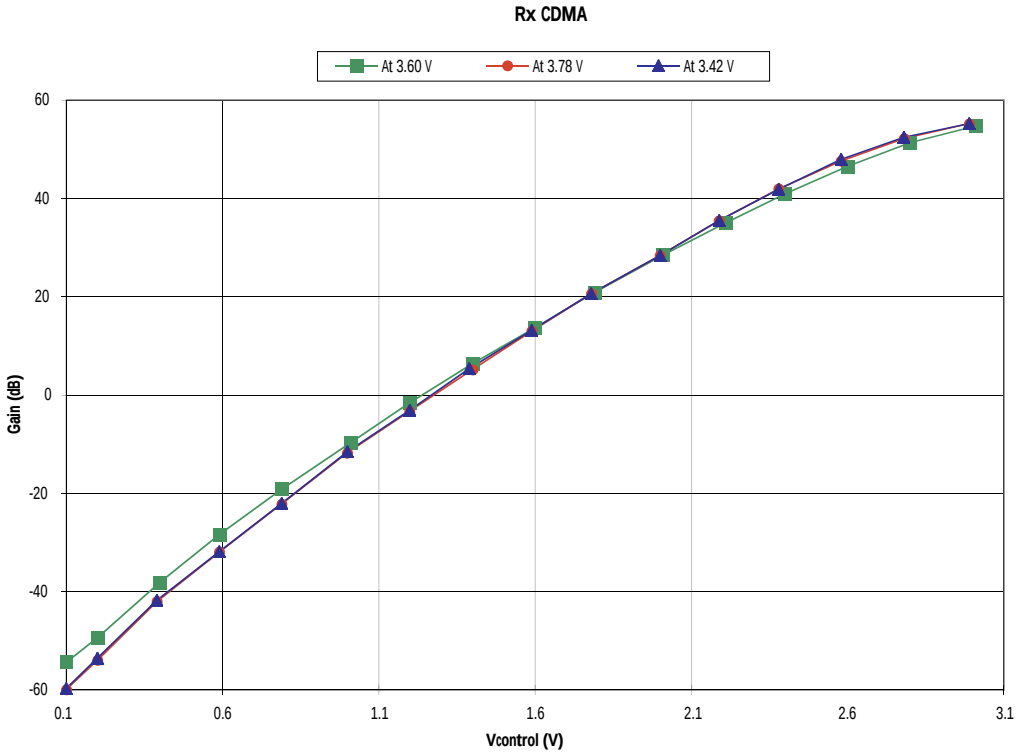
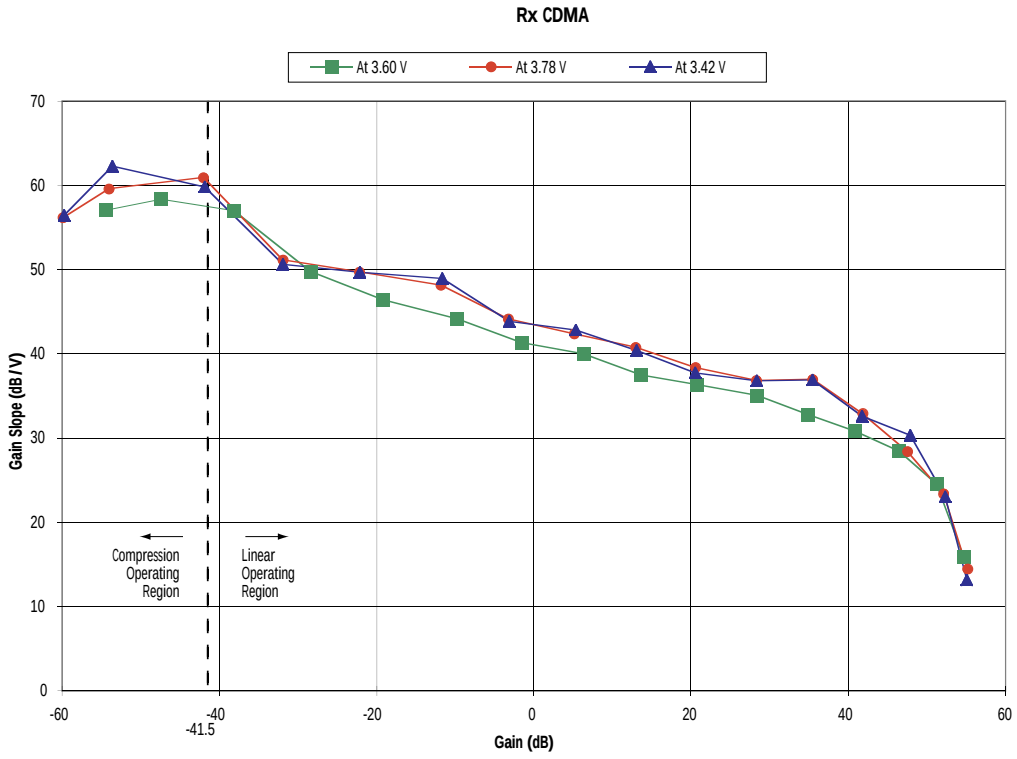
Figure 5a-e. Typical Q5500 Performance Characteristics Over Supply Voltage Range, CDMA Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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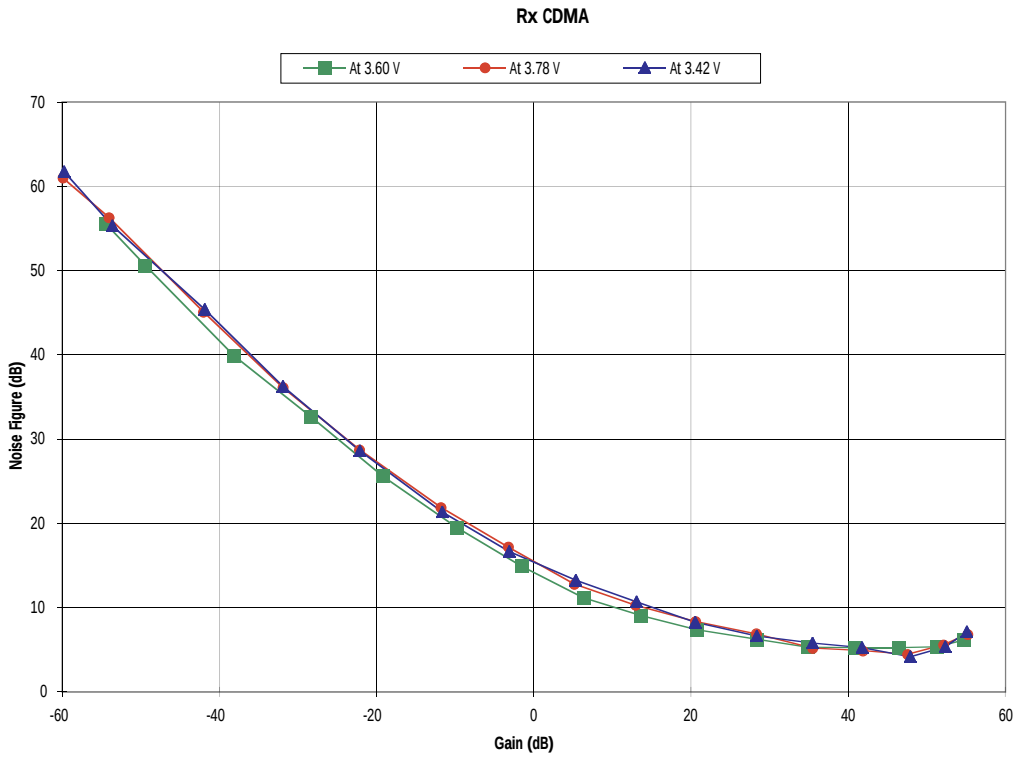
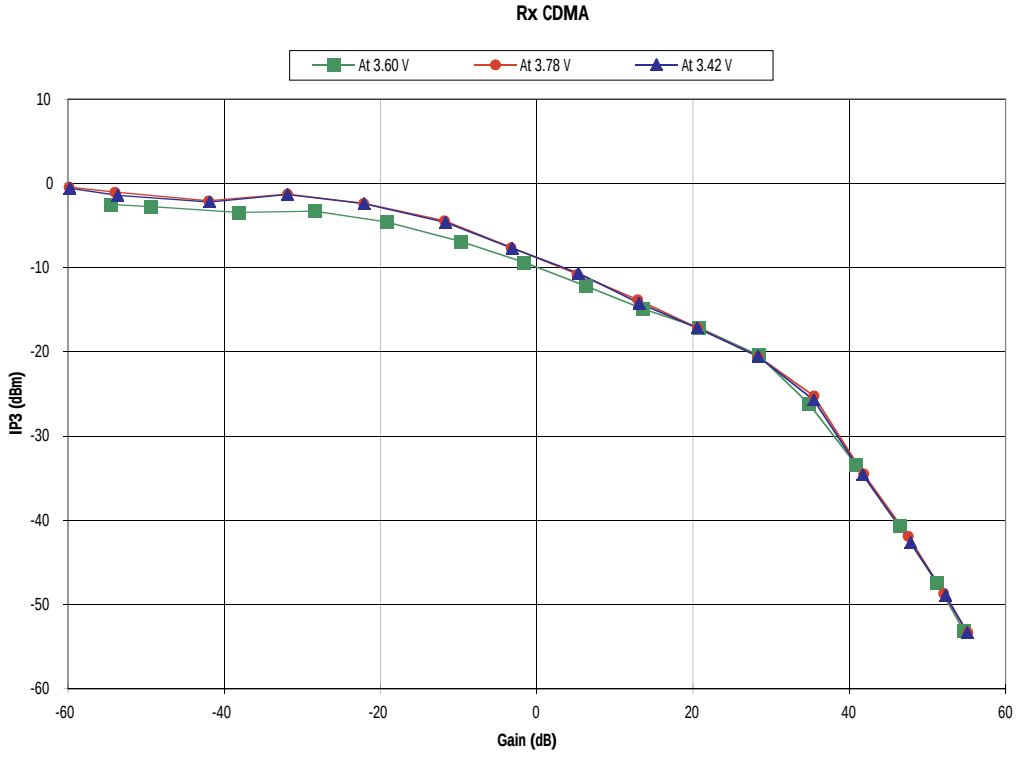


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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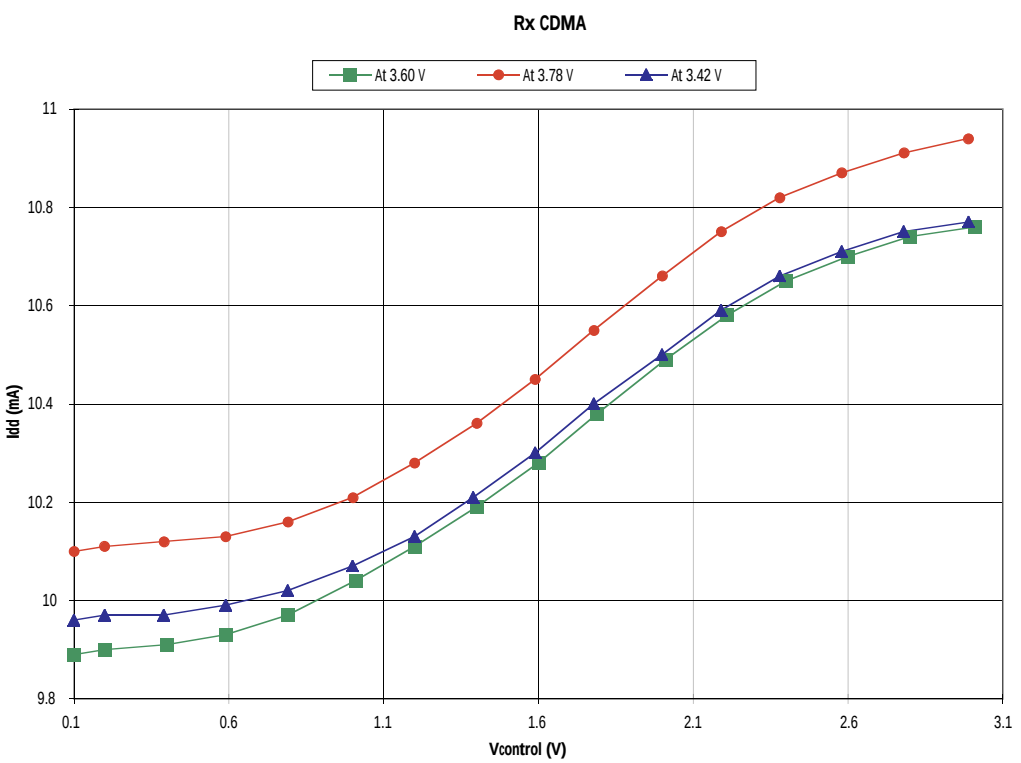

e. Supply Current vs. Control Voltage

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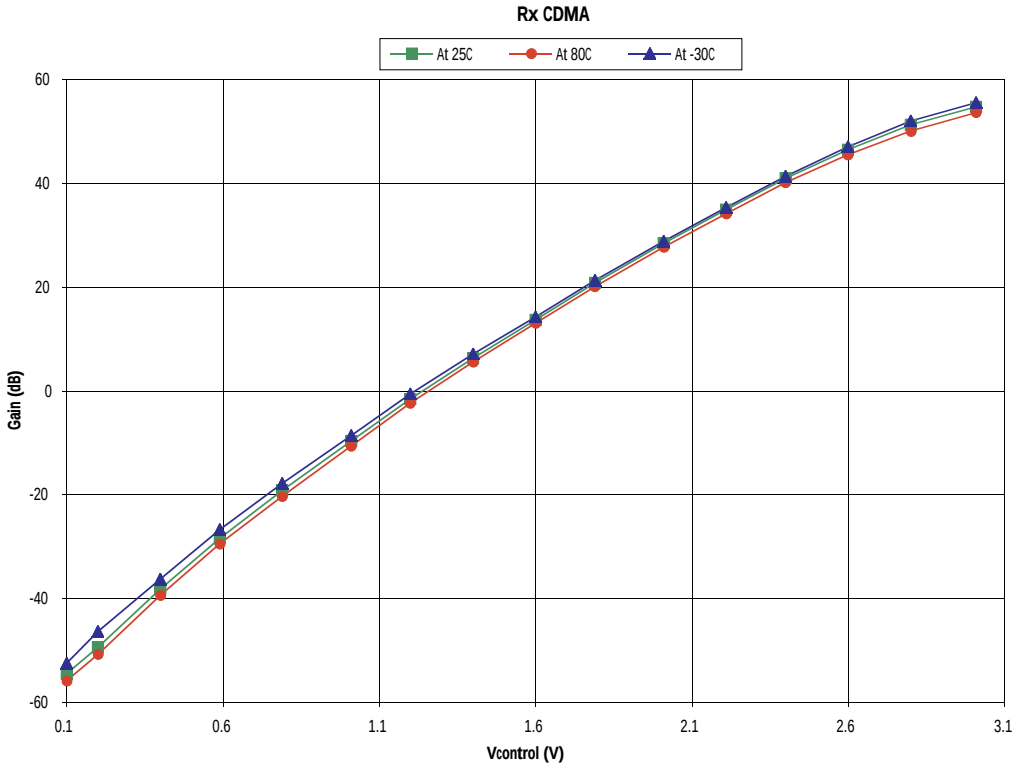
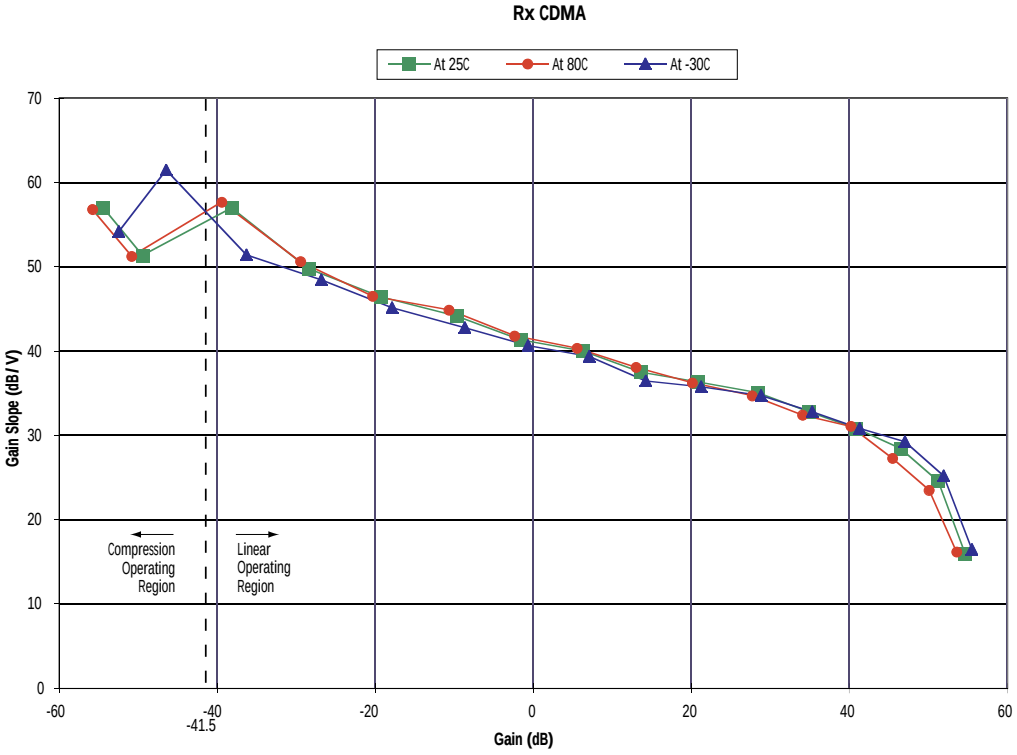
Figure 6a-e. Typical Q5500 Performance Characteristics Over Operating Temperature Range, CDMA Mode



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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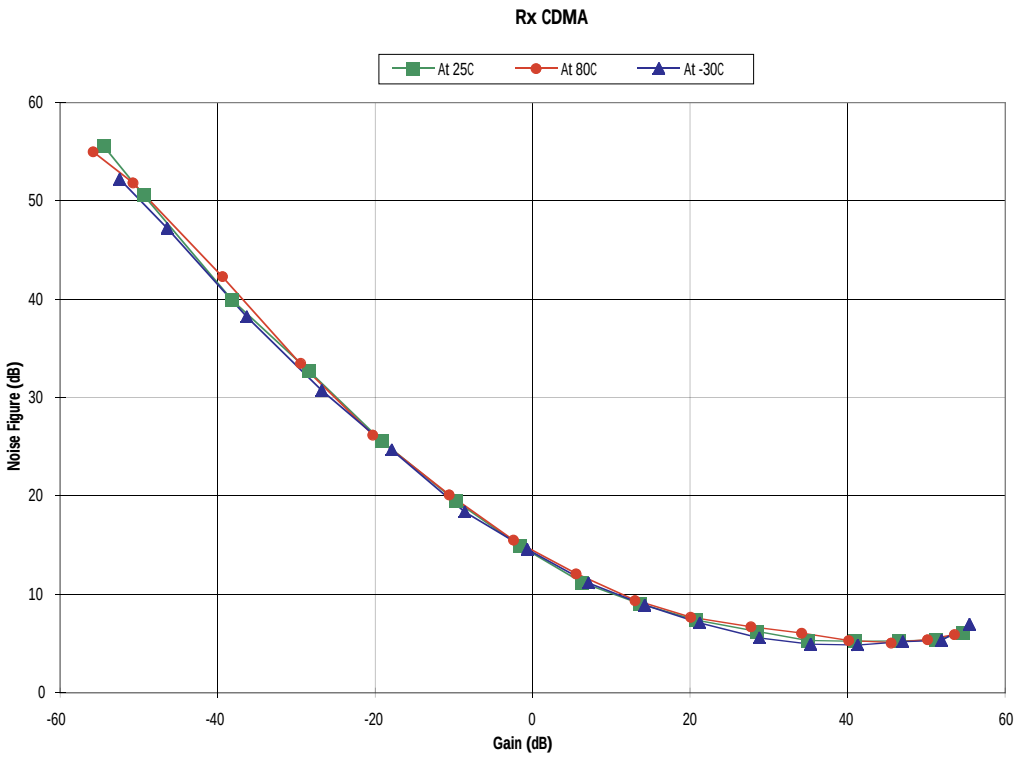
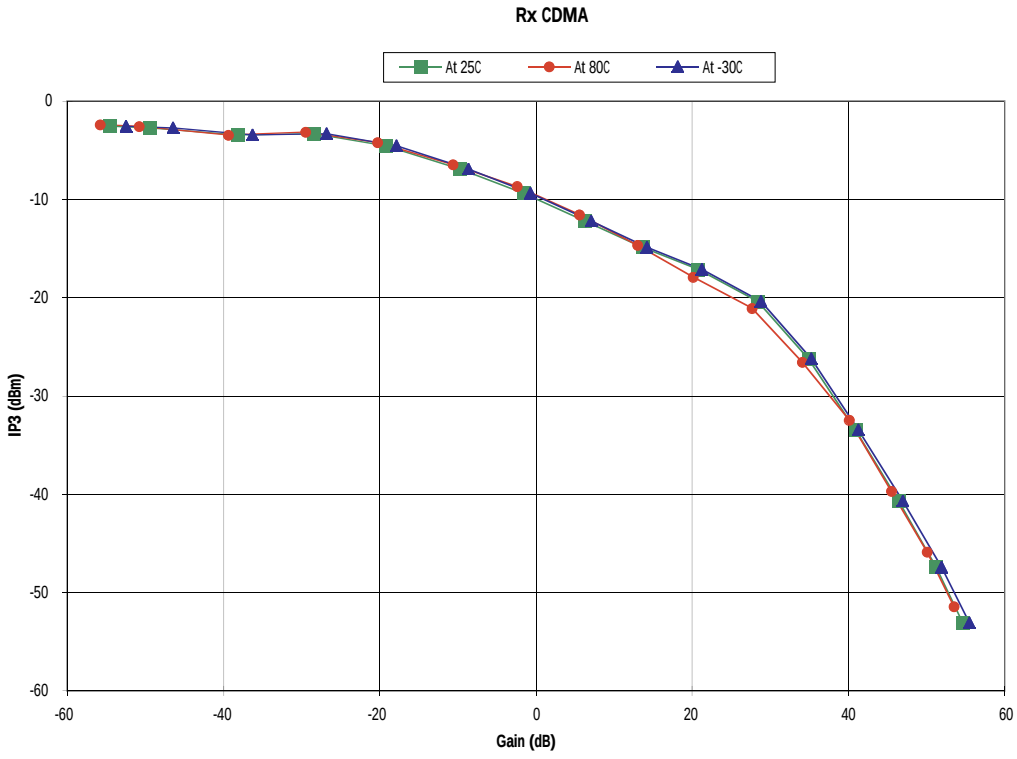


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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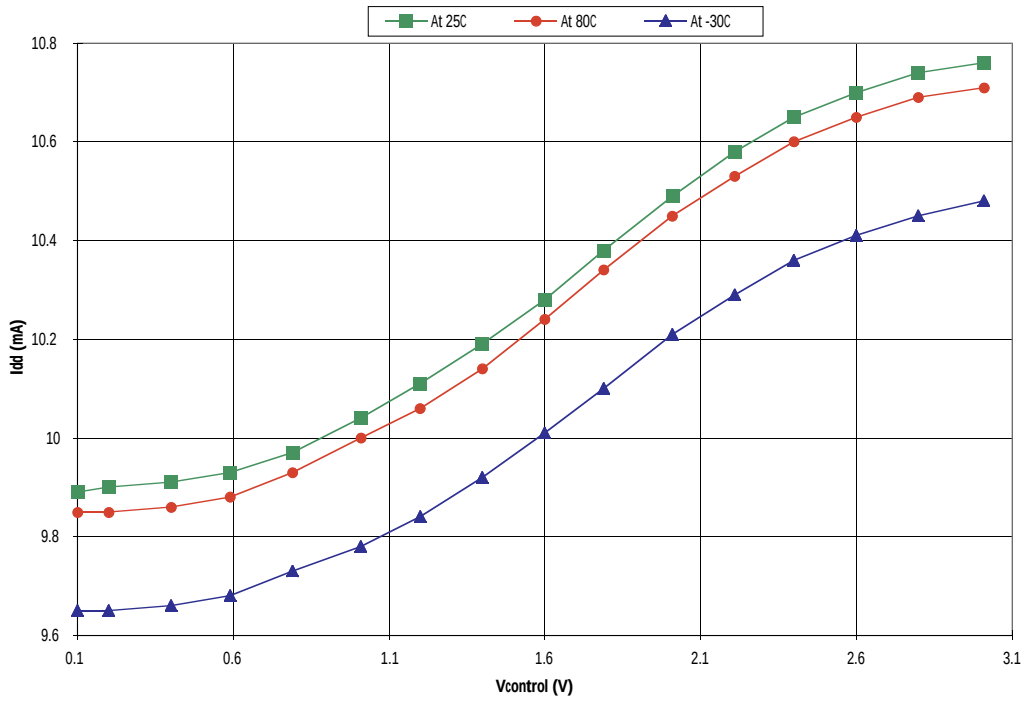

e. Supply Current vs. Control Voltage

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Table 5. Q5500 Noise Figure Standard Deviation X3

Gain (dB)	FM Mode Standard Deviation X3	CDMA Mode Standard Deviation X3
-45	2.85	3
-40	2.55	2.6
-35	2.55	2.6
-30	2	2.1
-25	2	2.1
-20	1.5	1.6
-15	1.5	1.6
-10	1.3	1.5
-5	1.3	1.5
0	1.2	1.3
5	1.2	1.3
10	1.2	1.1
15	1.2	1.1
20	0.9	0.8
25	0.9	0.8
30	0.55	0.55
35	0.55	0.55
40	0.4	0.4
45	0.3	0.3

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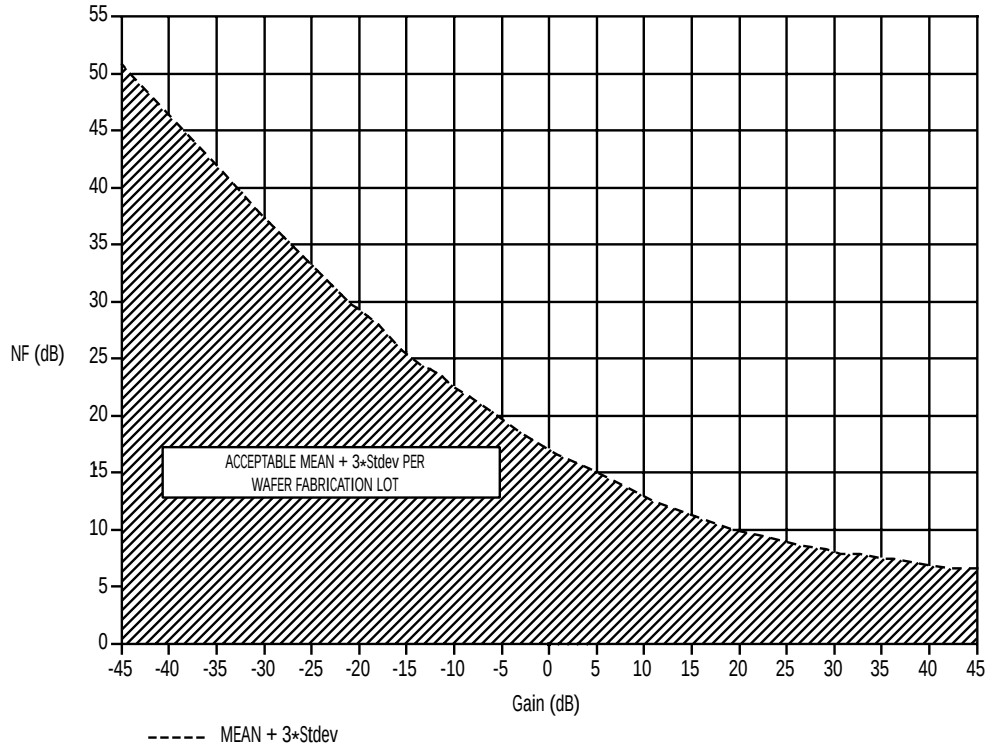
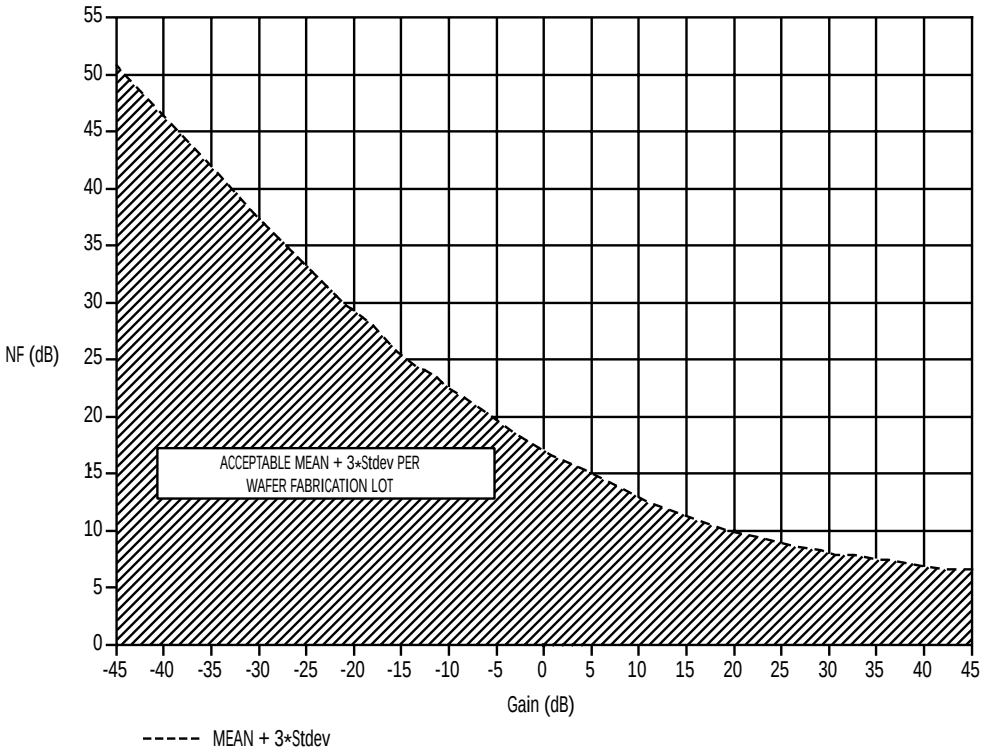
Figure 7a. Q5500 CDMA Mode Noise Figure Mean + 3*Stdev@ -30C



NF Typical = -4.039092 e - 09*G^5 - 4.164094e-07*G^4 + 7.80438e-06*G^3 + 6.321204e-03*G^2 - 0.466927*G + 15.7323

Figure 7b. Q5500 CDMA Mode Noise Figure Mean + 3*Stdev@ 25C



NF Typical = -1.499369e-09*G^5 - 4.456002e-07*G^4 + 1.677515e-06*G^3 + 6.355075e-03*G^2 - 0.454722*G +15.8378

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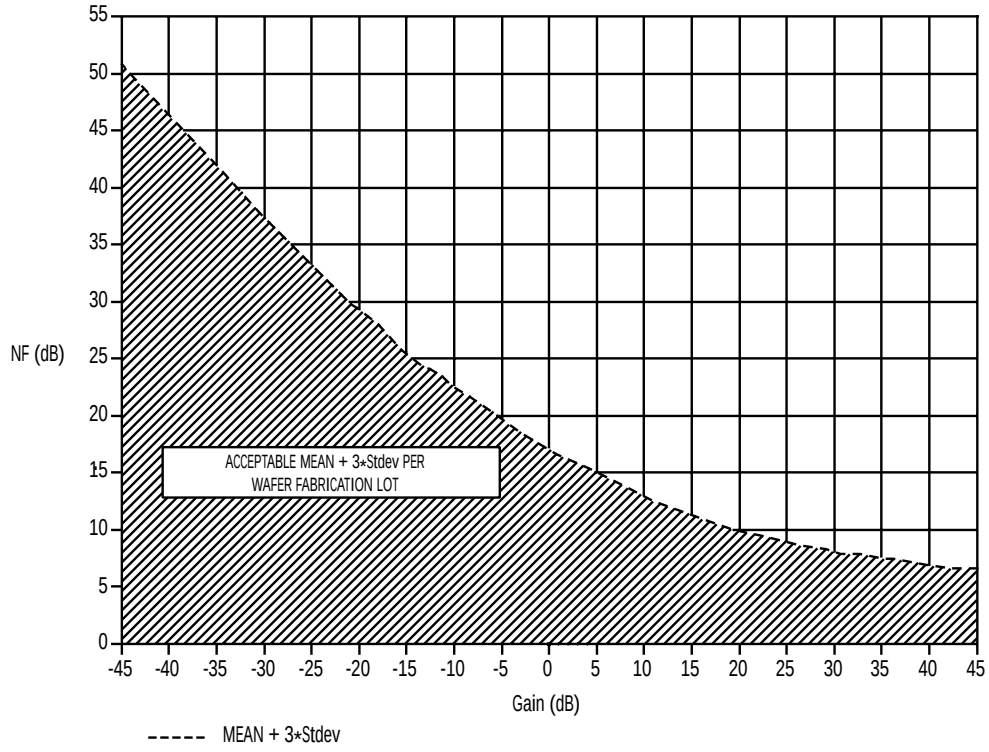
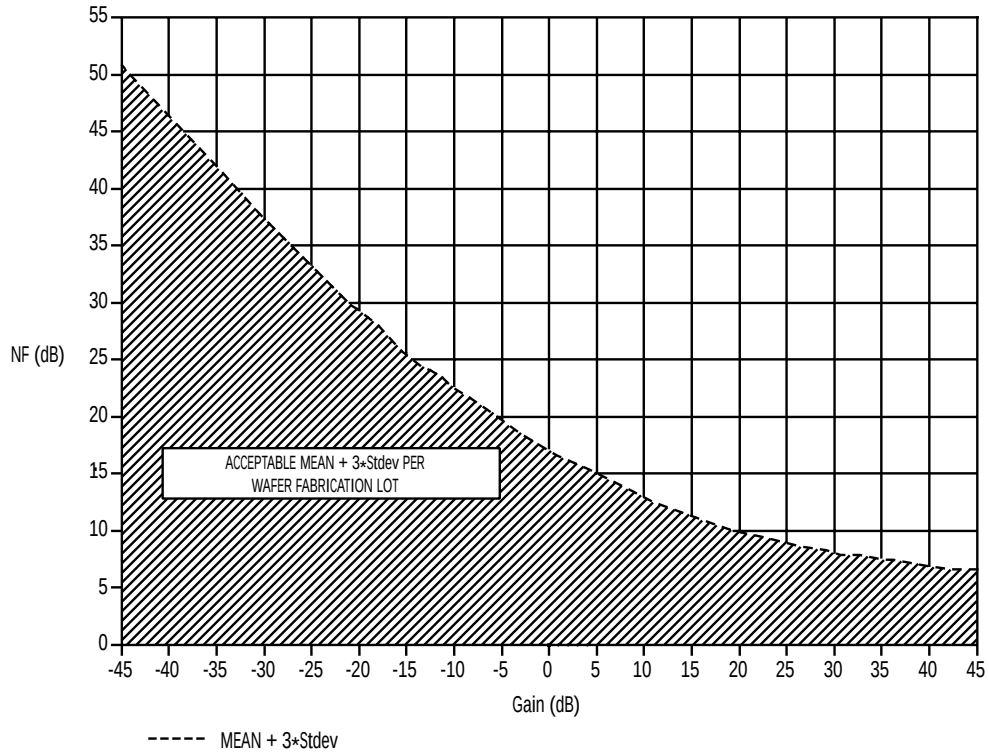
Figure 7c. Q5500 CDMA Mode Noise Figure Mean + 3*Stdev@ 80C



NF Typical = $4.211023e\text{-}10*G^5 - 6.676453e\text{-}07*G^4 - 7.945305e\text{-}06*G^3 + 7.236486e\text{-}03*G^2 - 0.448823*G + 16.0300$

Figure 7d. Q5500 FM Mode Noise Figure Mean + 3*Stdev@ -30C



NF Typical = $-1.765908e\text{-}08*G^5 - 1.538293e\text{-}07*G^4 + 5.645998e\text{-}05*G^3 + 5.891888e\text{-}03*G^2 - 0.518637*G + 15.3817$

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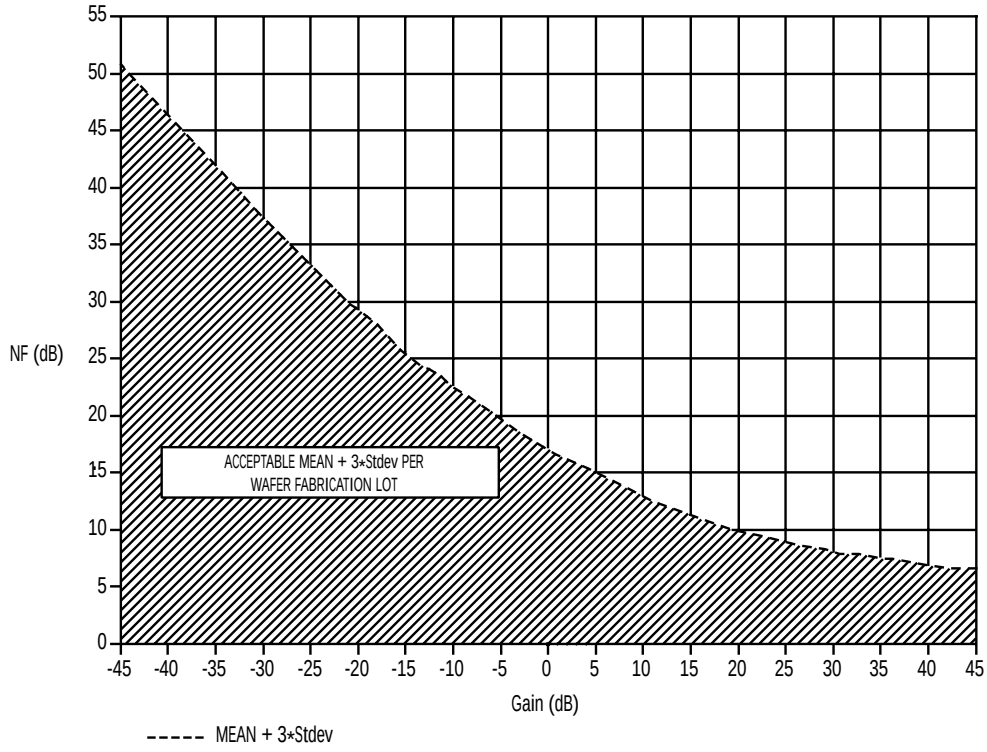
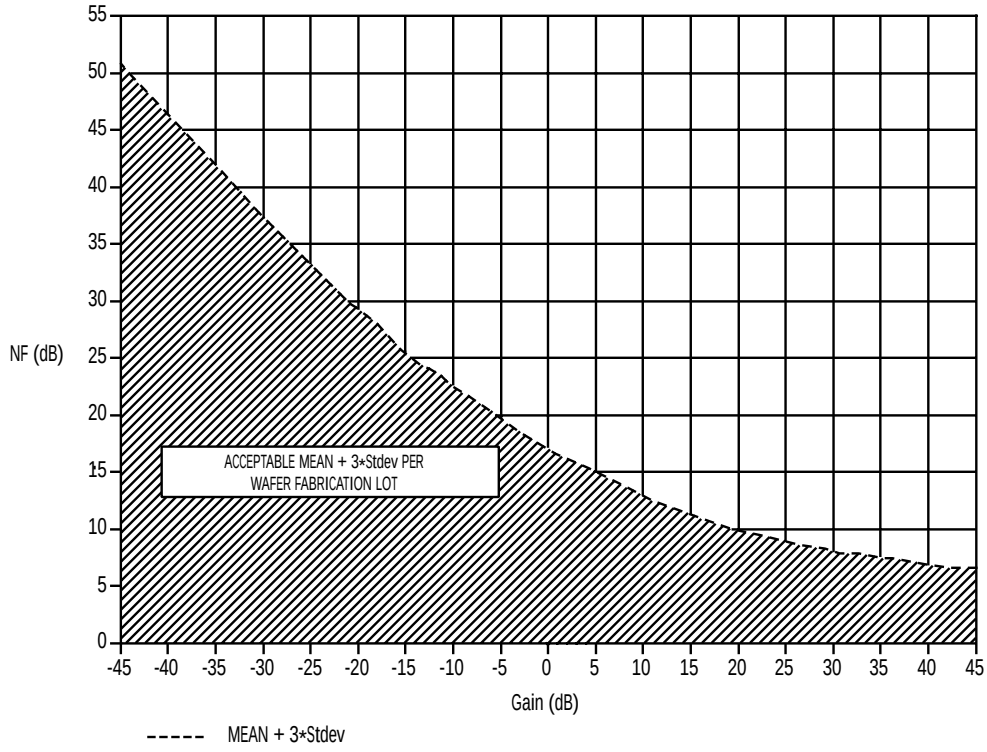
Figure 7e. Q5500 FM Mode Noise Figure Mean + 3*Stdev@ 25C



NF Typical = $-1.194405e-08*G^5 - 2.862301e-07*G^4 + 3.824693e-05*G^3 + 6.253457e-03*G^2 - 0.493354*G + 15.2345$

Figure 7f. Q5500 FM Mode Noise Figure Mean + 3*Stdev@ 80C



NF Typical = $-1.099614e-08*G^5 - 3.403353e-07*G^4 + 3.183561e-05*G^3 + 6.640703e-03*G^2 - 0.489305*G + 15.4513$

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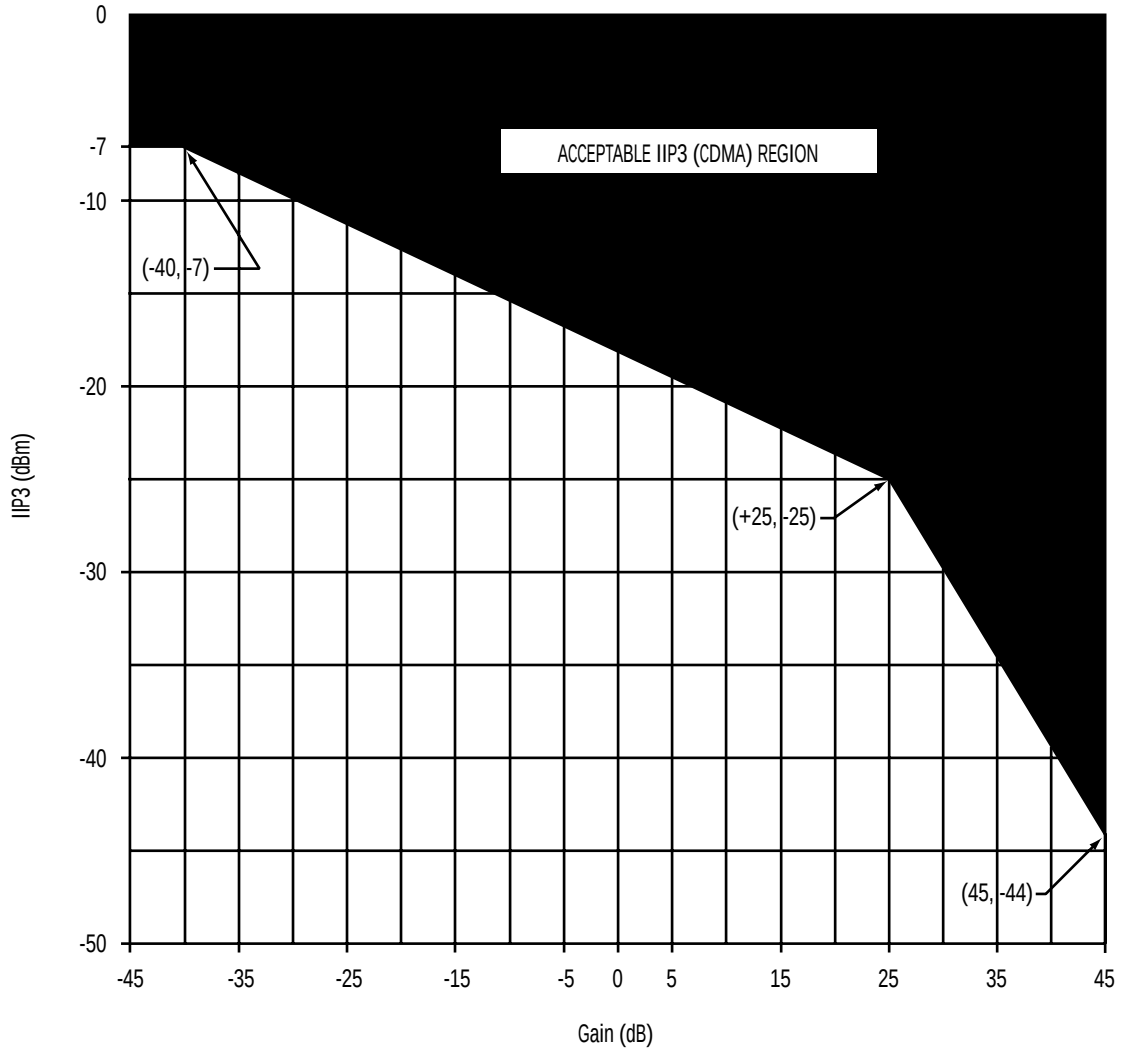
Figure 8a. Q5500 IIP3 (CDMA Mode)



IIP3 ≥ -7 dBm (-45 ≤ Gain ≤ -40 dB)

IIP3 ≥ -0.276923 * Gain - 18.07692 dBm (-40 ≤ Gain ≤ 25 dB)

IIP3 ≥ -0.95 * Gain - 1.25 dBm (25 ≤ Gain ≤ 45 dB)

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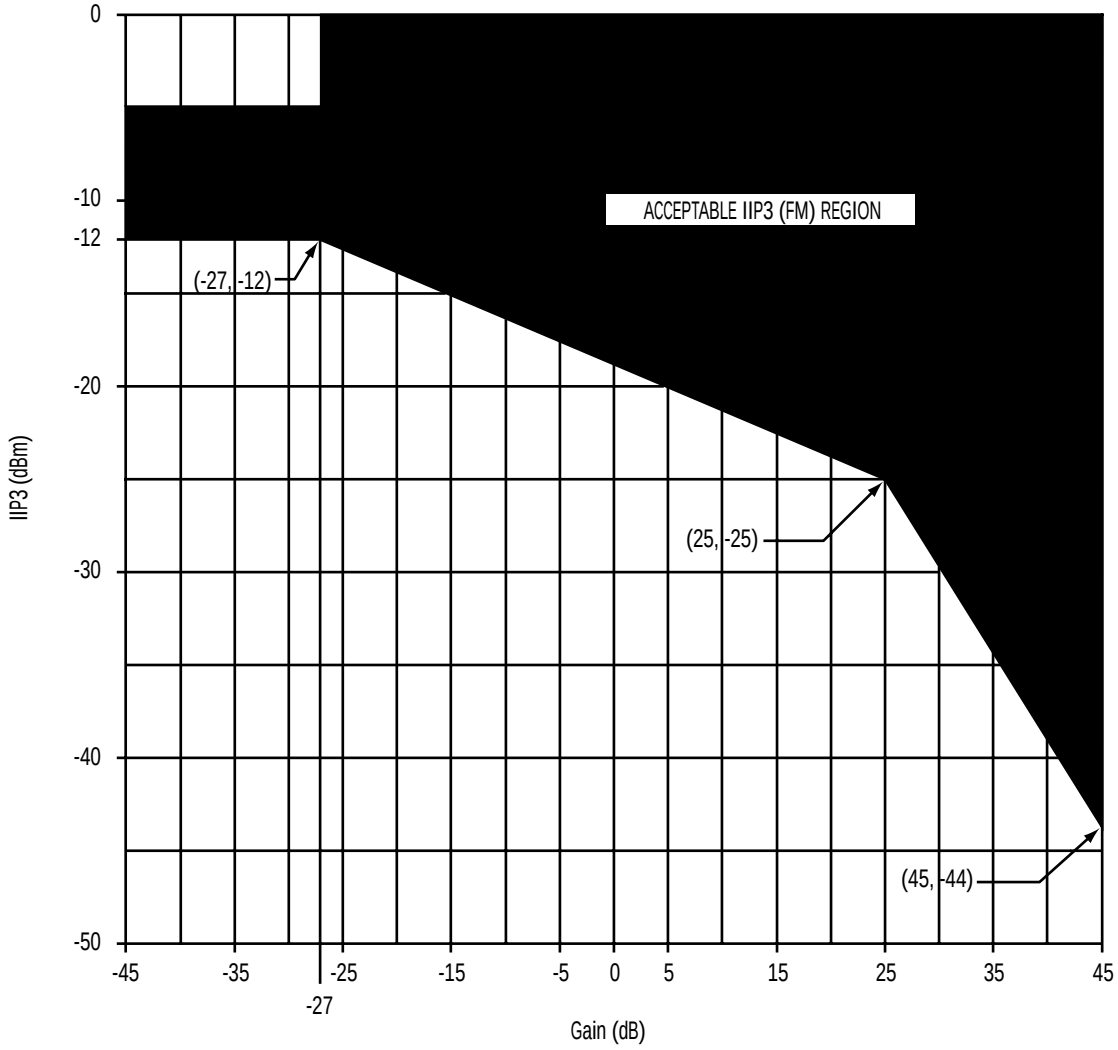
Figure 8b. Q5500 IIP3 (FM Mode)



-12 ≤ -5 dBm (-45 ≤ Gain ≤ -27 dB)

IIP3 ≥ -0.25 * Gain -18.75 dBm (-27 < Gain ≤ 25 dB)

IIP3 ≥ -0.95 * Gain - 1.25 dBm (25 < Gain ≤ 45 dB)

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Table 6a-g. Description of Q5500 Pin Functions

a. Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
IN +	1	Differential Input	Positive Differential Input
IN –	2	Differential Input	Negative Differential Input

b. Low-Gain Analog Mode Single Ended Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
FM IN +	4	Single Ended AC Input	Single Ended Analog Input

c. Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ – Analog Gain Control Input $V_{CONTROL}$ = 0.1 V, Low Gain Rail, $V_{CONTROL}$ = 3.0 V, High Gain Rail

d. Analog / Digital Mode Select Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
SEL	7	CMOS Input	$V_{SELECT} \geq +3.4$ V, Digital Mode Select $V_{SELECT} \leq +0.5$ V, Analog Mode Select

e. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output
OUT –	9	Differential Output	Analog Negative Differential Output

f. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin

g. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply
GND	3, 6, 11, 12	Ground	Ground Connection
AC GND	5	AC Ground	Analog Ground Connection

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Figure 9. Q5500 Functional Block Diagram

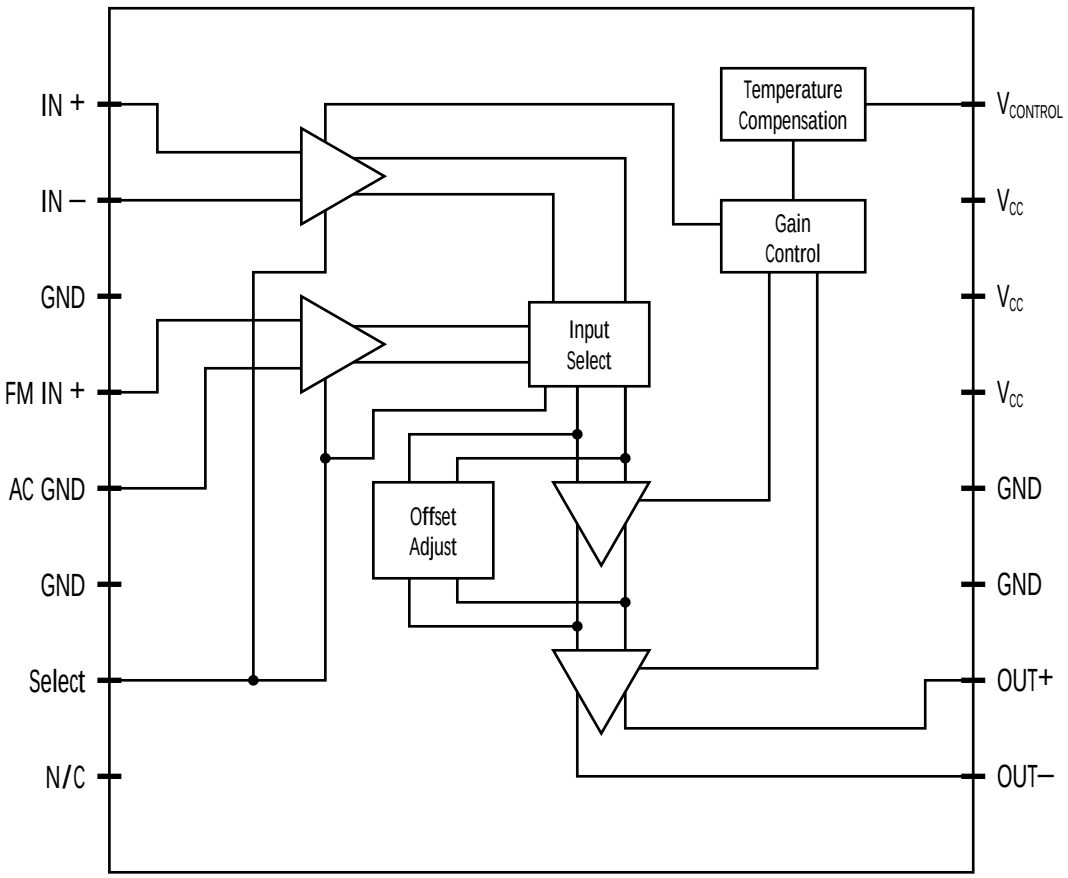

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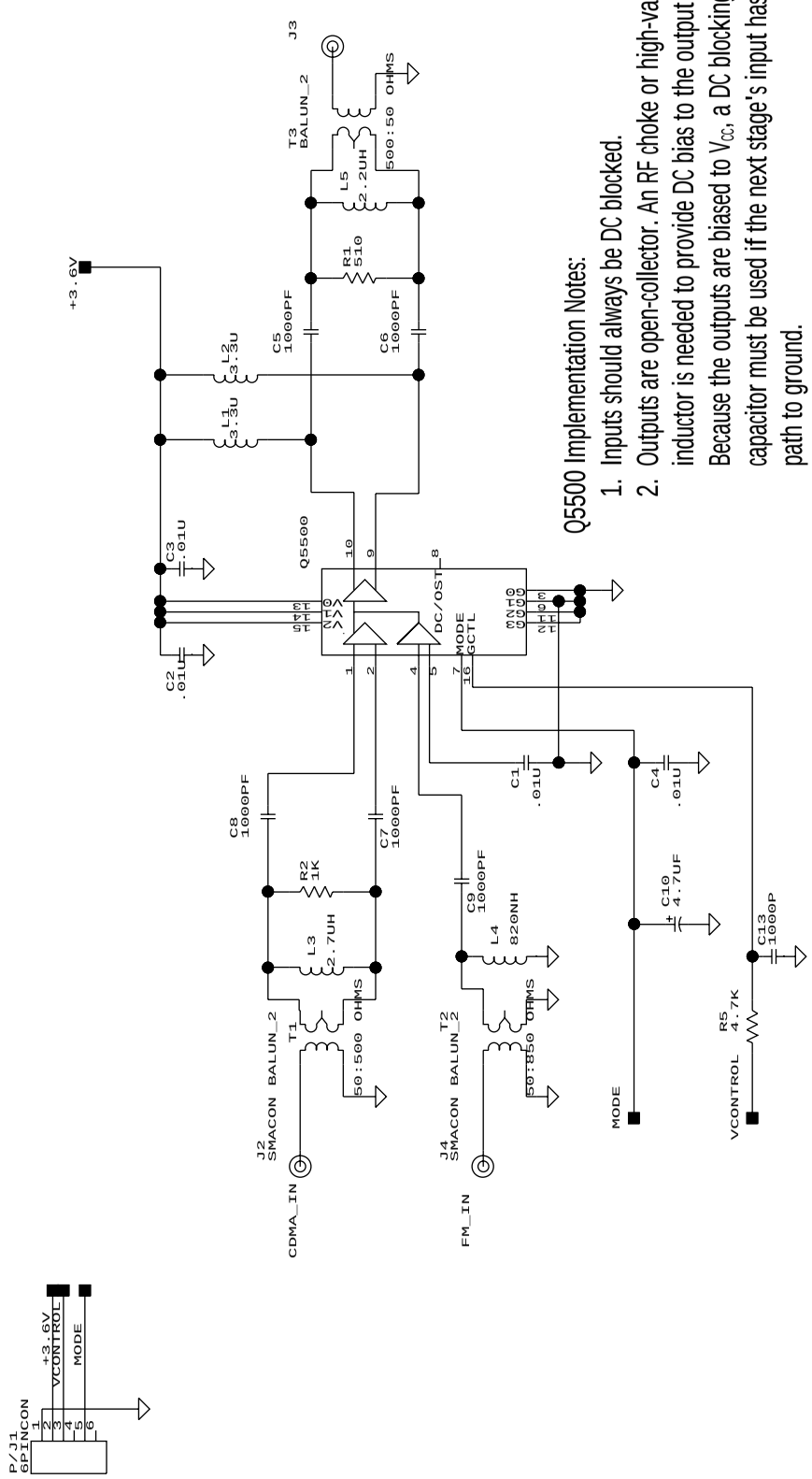
Figure 10. Q5500 Test Schematic



Q5500 Implementation Notes:

1. Inputs should always be DC blocked.
2. Outputs are open-collector. An RF choke or high-valued inductor is needed to provide DC bias to the output pins. Because the outputs are biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.
3. The input/output interface may require matching networks, however this requirement is very system dependent. The bias inductor is typically incorporated in the matching network between the output and next stage.
4. V_{CC} inputs should be bypassed to ground with about a 0.01µF capacitor, keeping trace connections to a minimum length.

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Q5505 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent and functional damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond the min/max ranges indicated in the operational sections of this specification is not implied. Exposure exceeding absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Q5505 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Storage Temperature	T_{STO}	-30	+125	°C	
Junction Temperature	T_J	-30	+125	°C	
Supply Voltage (Relative to GND)	V_{CC}		+8.5	V	
Continuous RF Input Power			-15	dBm	
DC Voltage on any Non RF Input Pin (Relative to GND)	V_{IN}	-0.5	V_{CC} + 0.5	V	
Latchup Insensitivity	I_{TRIG}	±200		mA	1
ESD Protection	V_{ESD}	±250		V	2

NOTES:

1. Method meets the intent of JEDEC STD 17 Publication and is the maximum allowable current flow through the input and output protection diodes.
2. Method meets the intent of MIL-STD-883. Method 3015.

Table 8. Q5505 Operating Range

PARAMETER	SYMBOL	MIN	MAX	UNIT
Operating Temperature (Case)	T_C	-30	+80	°C
Operating Voltage (Relative to GND)	V_{CC}	+3.42	+3.78	V

Table 9. Q5505 DC Electrical Parameter

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Supply Current	I_{CC}		25	mA	

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Table 10. Q5505 Electrical Characteristics

PARAMETER	VALUE	NOTES
TX AGC Frequency	130.38 MHz	
Gain Flatness (± 630 kHz)	±0.25 dB	
TX Power Gain	$V_{CONTROL}$ = 0.1 V, G< -45 dB $V_{CONTROL}$ = 3.0 V, G> 40 dB	1, 4 3, 5
Power Gain Slope	70 dB/V Maximum Over Specified Gain Region (-45 to +40 dB) 0 dB/V Minimum Over Specified Gain Region (-45 to +40 dB)	1, 4, 3
Power Gain Slope Linearity (Over and 6 dB Gain Segment)	± 3.0 dB/V	
NF for AGC Input	Figure 14	1
IIP3	Figure 15	1, 2, 3
IF Input Impedance (Differential)	1k ± 15%, < 1 pF Capacitive	4
IF Output Impedance	> 10 k Ω, < 1 pF Capacitive	4
Gain Control Pin Input Impedance	> 30 kΩ, < 50 pF Capacitive	
Stability	Over Full AGC Range With Source and Load VSWR 10:1 All Angles Spurious < -70 dBc	

NOTES:

1. Z_S = 1 kΩ, Z_{Leff} = 500 Ω, Z_L = 1 kΩ (see Figures 11a and 11b).
2. IIP3 = IMR3/2 + P_{IN} dBm, where IIP3 is the input third order intercept in dBm, IMR3 is the third order intermodulation product rejection in dB, and P_{IN} is the total power of the two input tones in dBm.
3. Input Power level = -38 dBm.
4. See Figures 11a and 11b.
5. $V_{CONTROL}$ Source Impedance must be 3.3 k ± 5%.

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Figure 11a. Definition of Source Impedance, Z_S, and Input Impedance, Z_{IN}, for Q5505

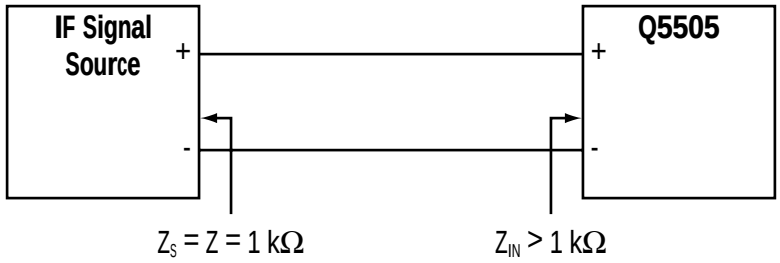

Figure 11b. Definition of Load Impedance, Z_L, and Output Impedance, Z_O, for Q5505

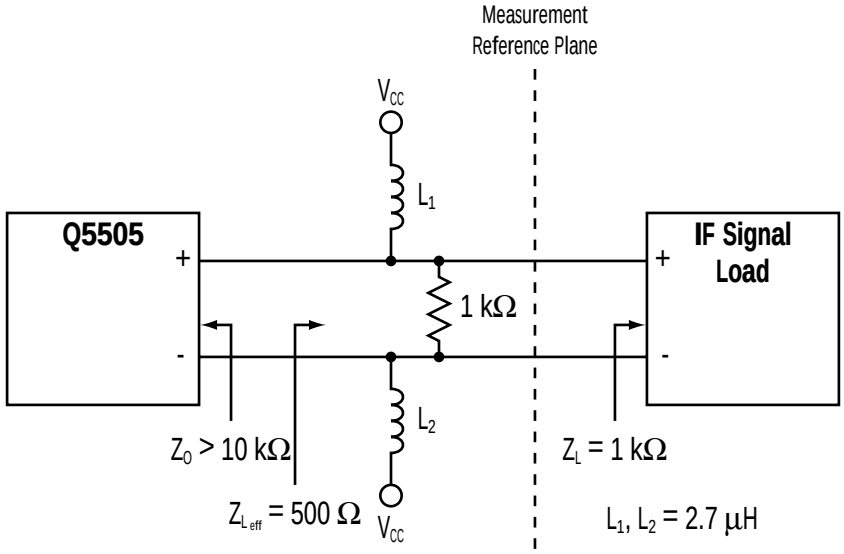

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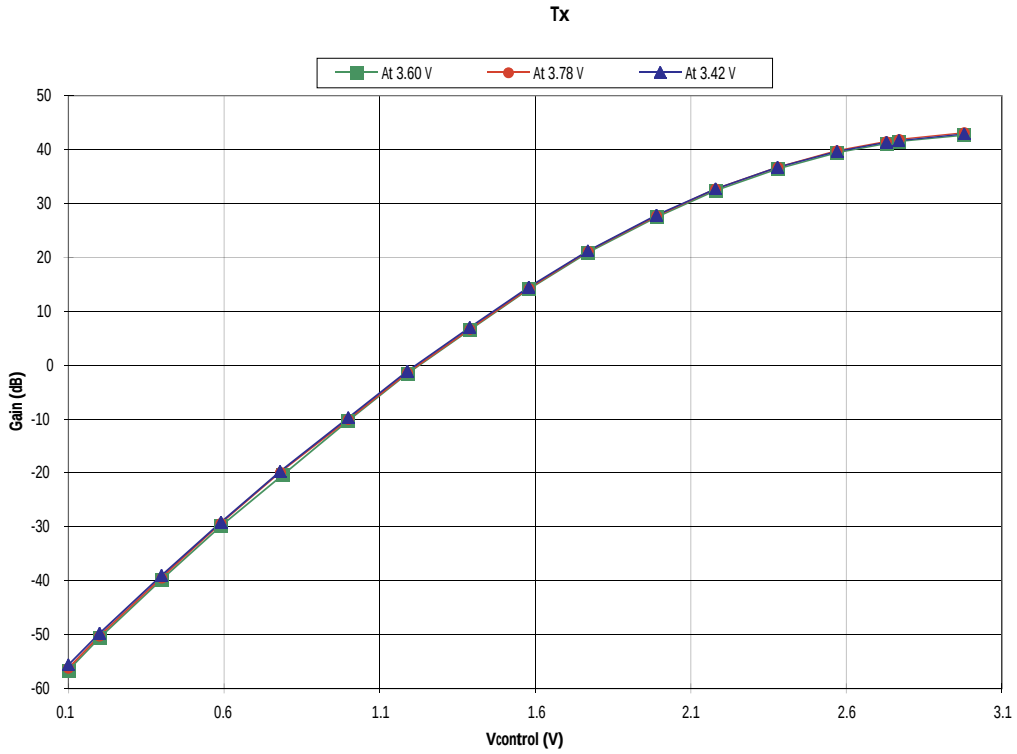
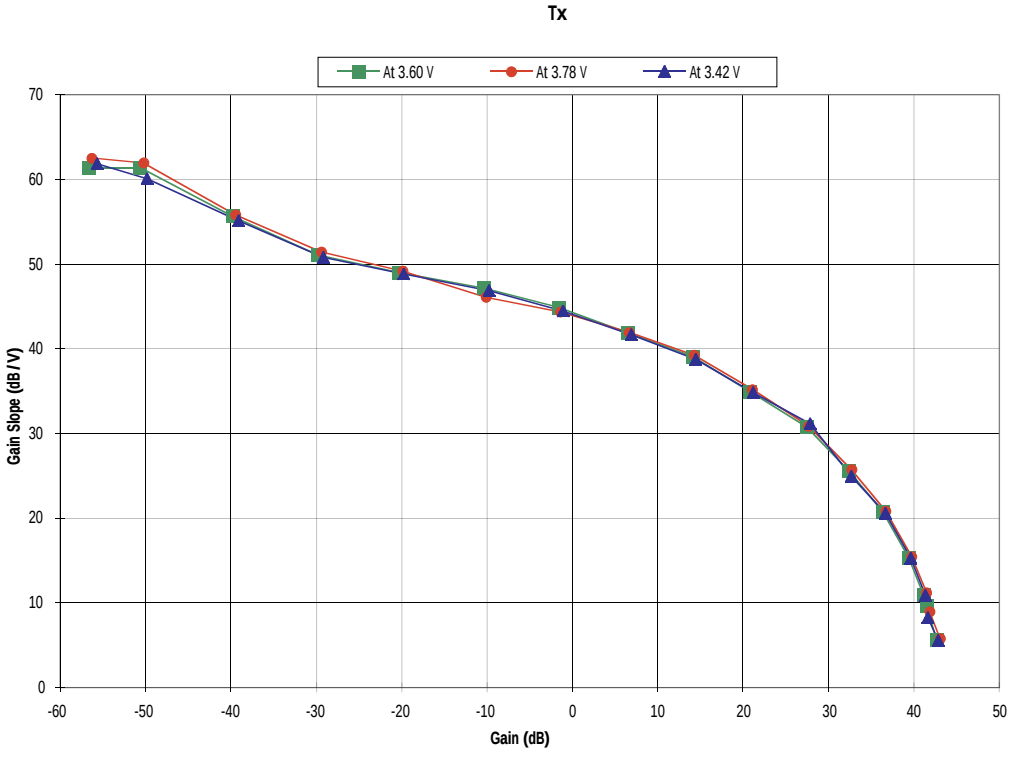
Figure 12a-e. Typical Q5505 Performance Characteristics Over Supply Voltage Range



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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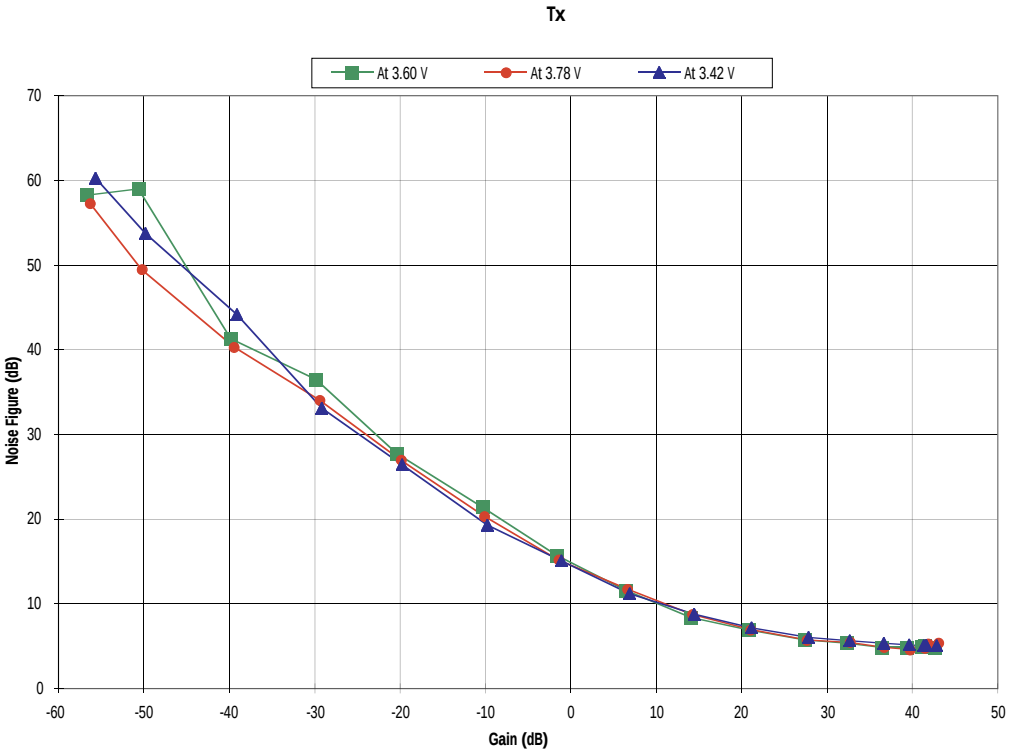
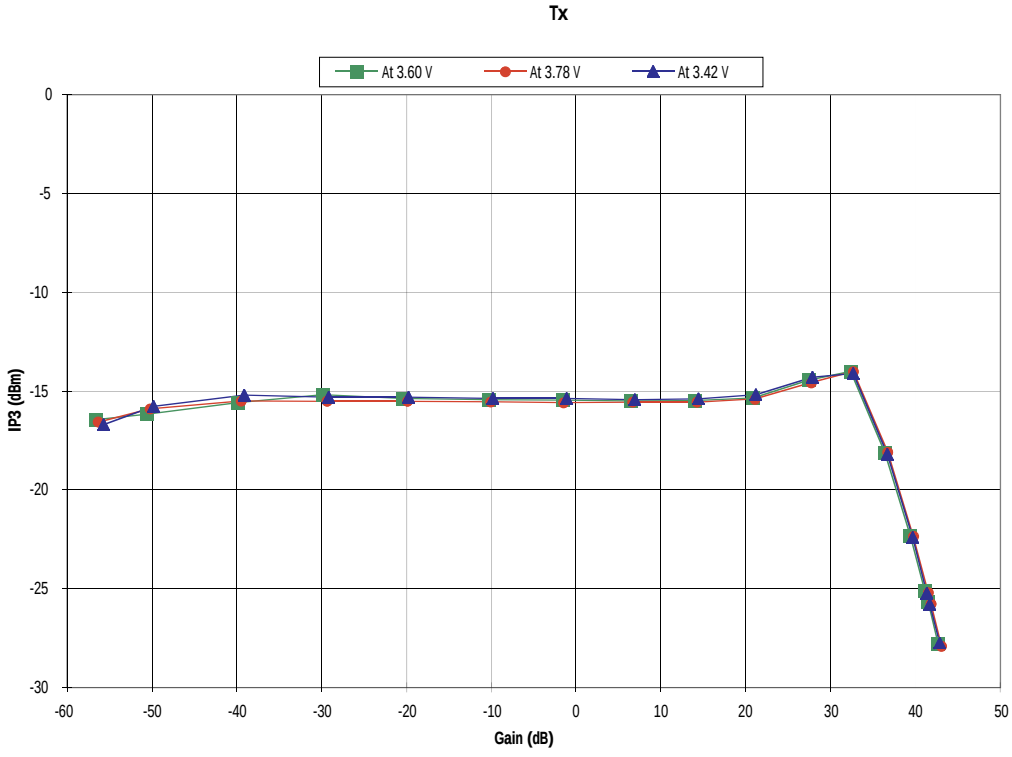


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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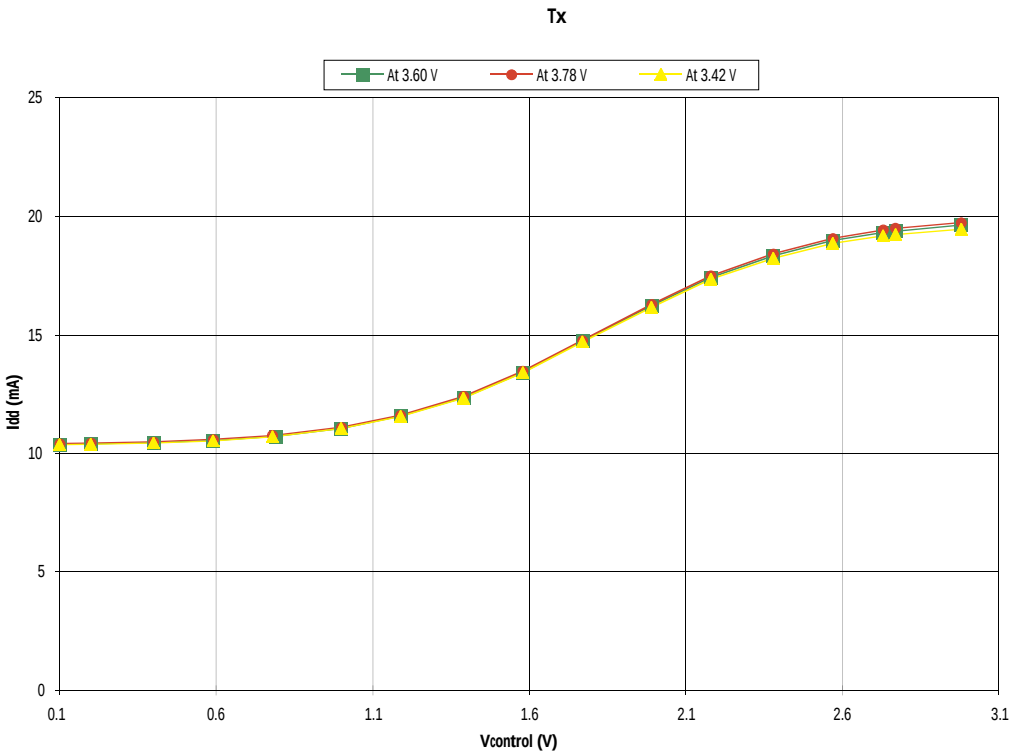

e. Supply Current vs. Control Voltage

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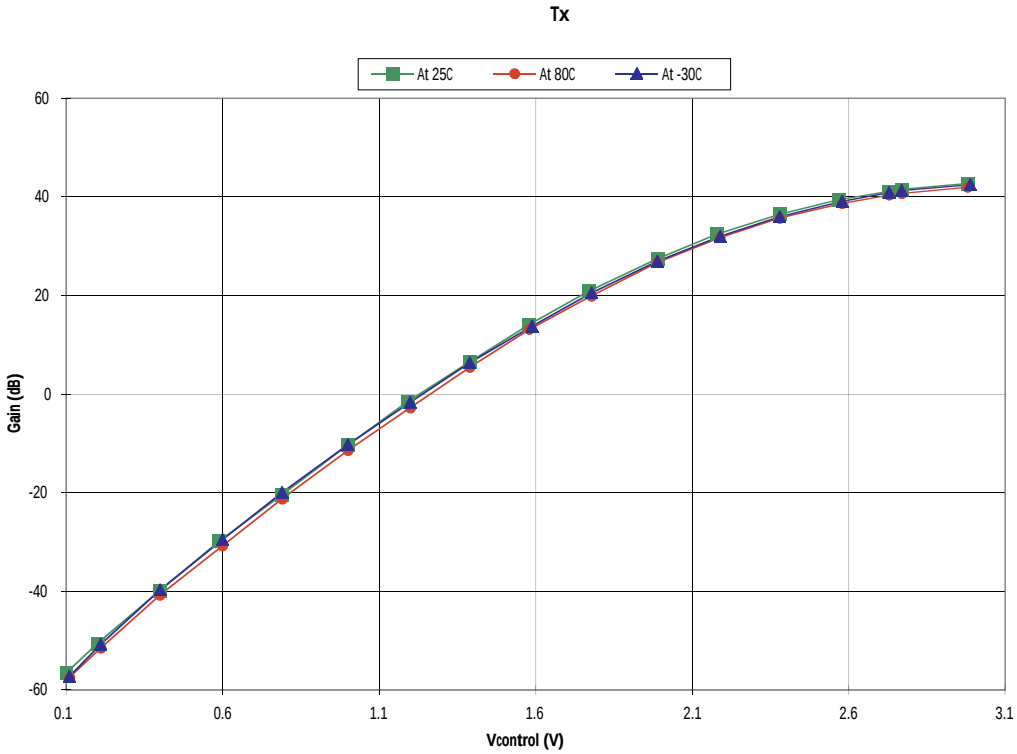
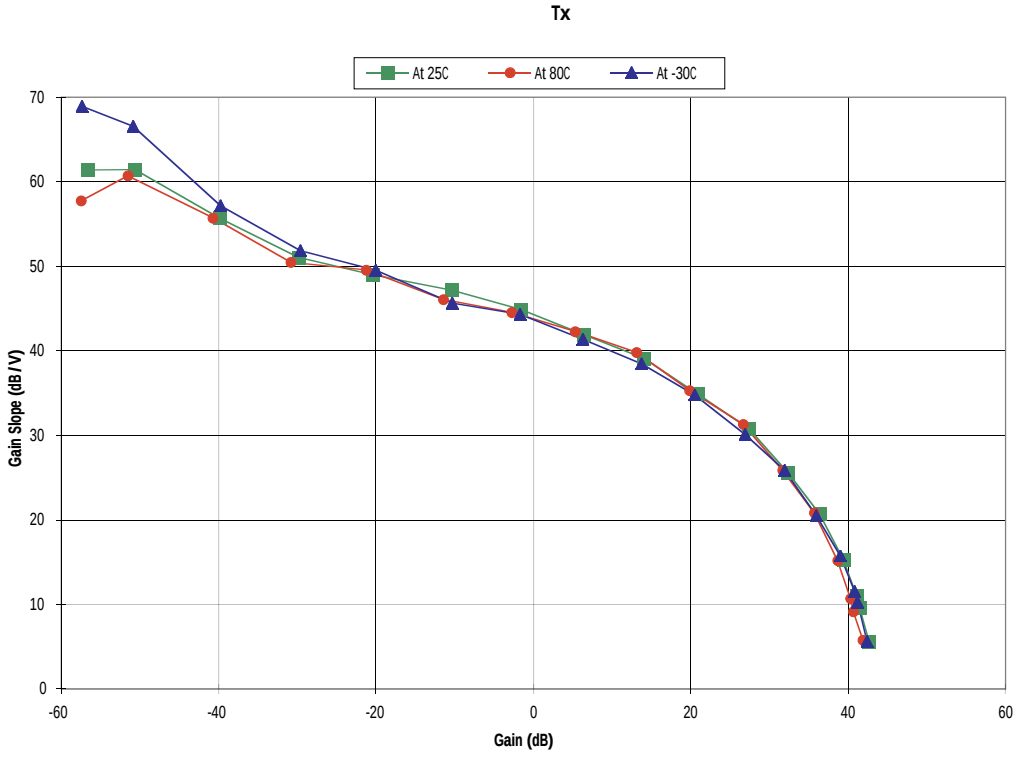
Figure 13a-e. Typical Q5505 Performance Characteristics Over Operating Temperature Range



a. Gain vs. Control Voltage



b. Gain Slope vs. Gain

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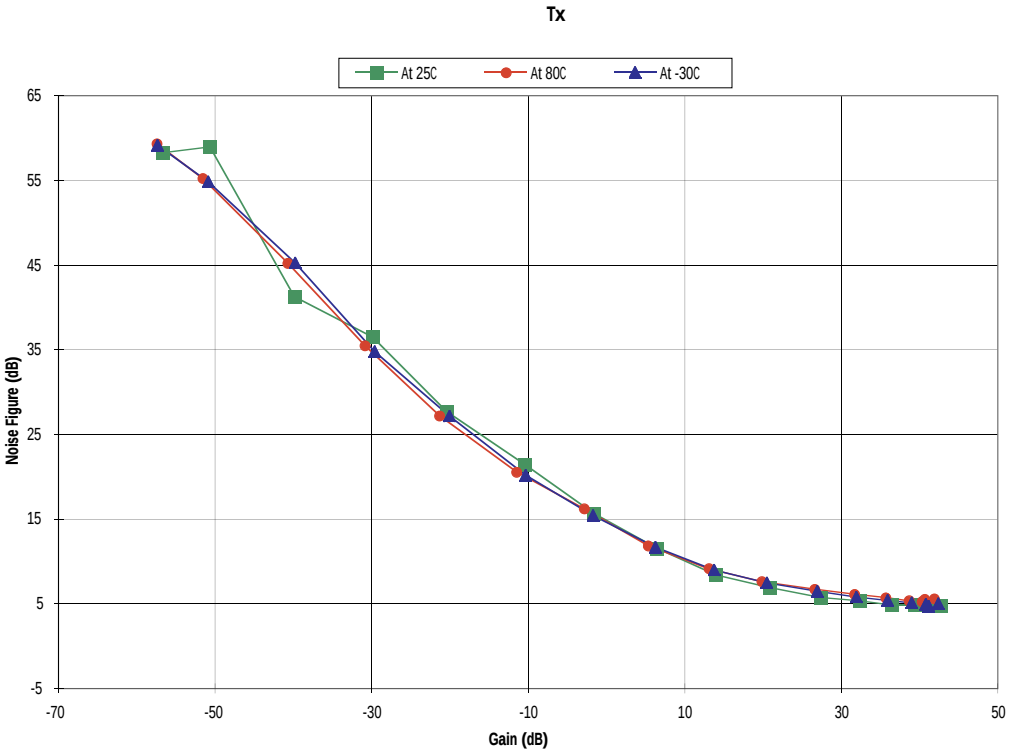
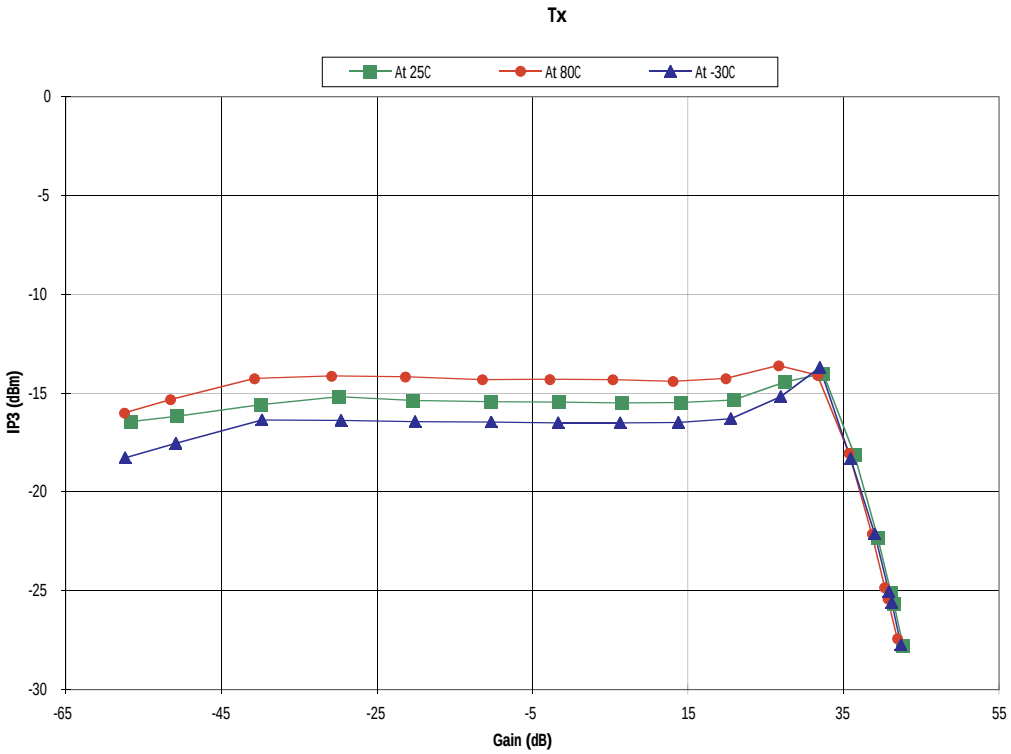


c. Noise Figure vs. Gain



d. Input IP3 vs. Gain

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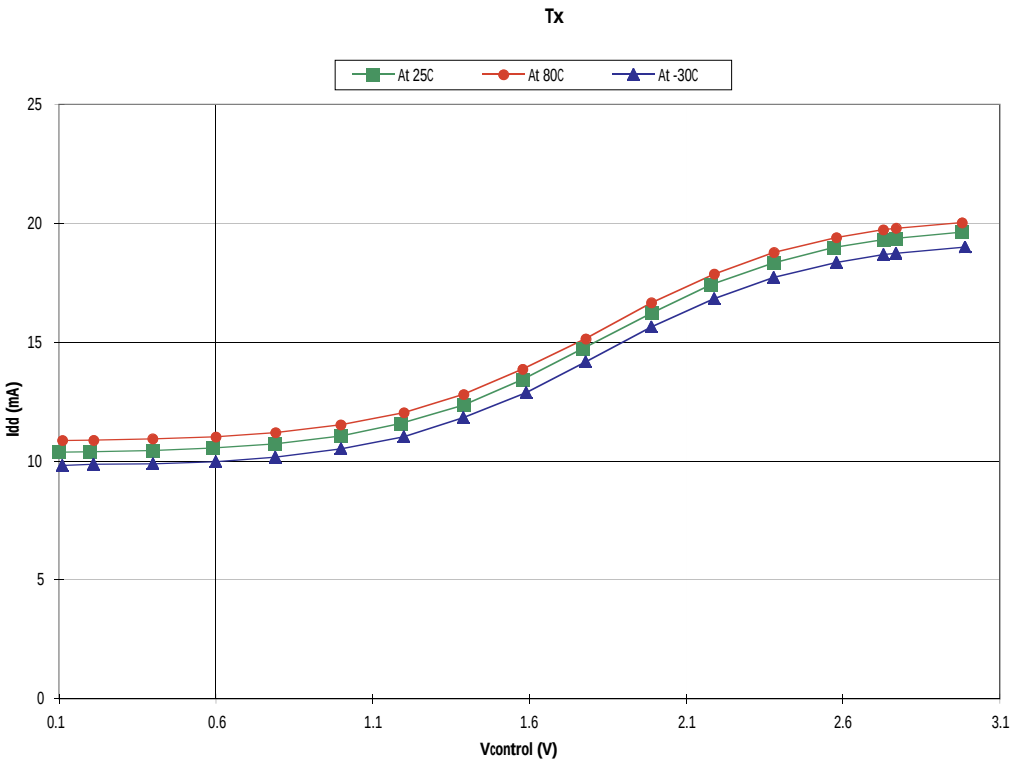

e. Supply Current vs. Control Voltage

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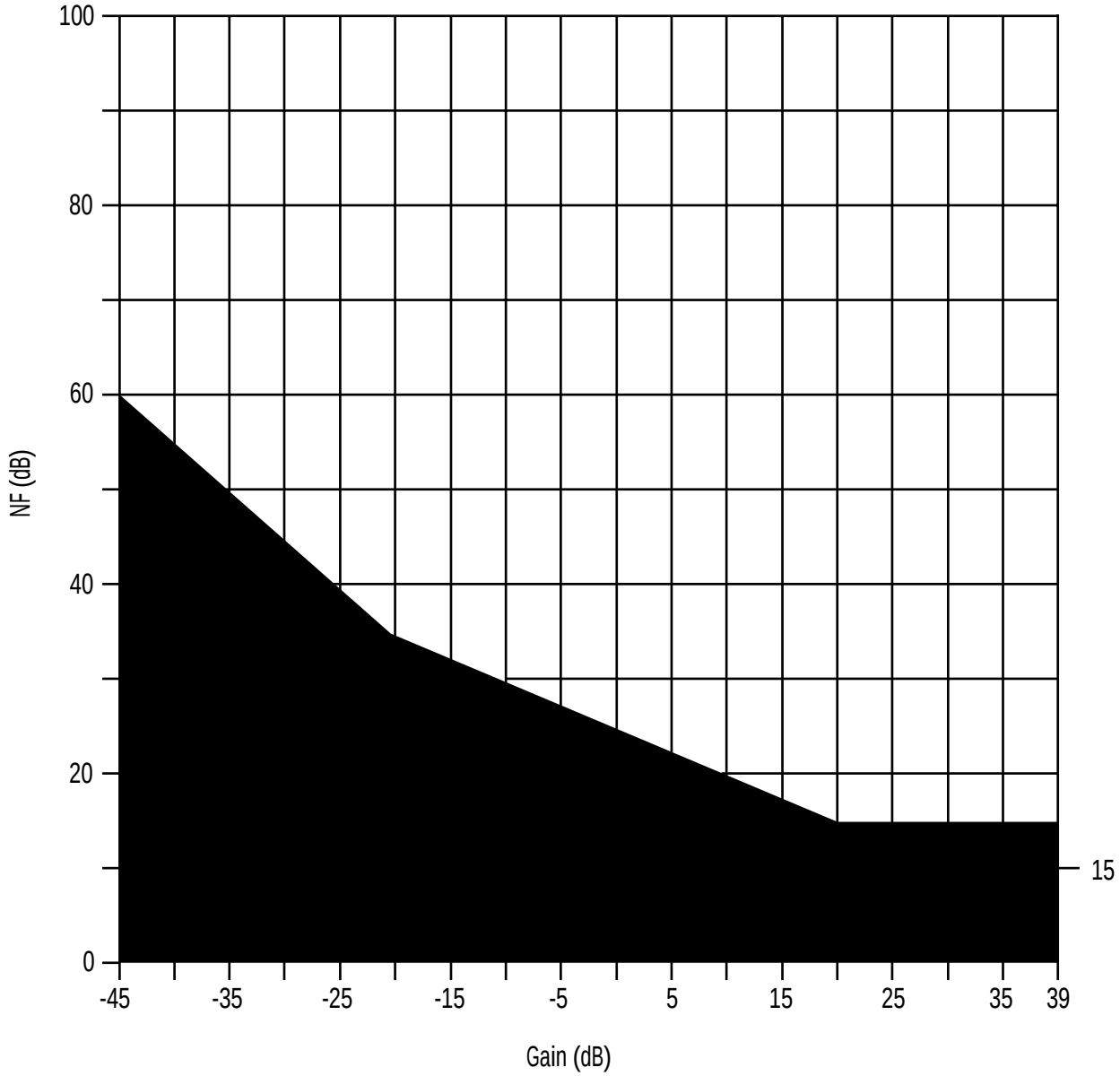
Figure 14. Q5505 Cascaded NF Model



NF < 14.5 - G (-45 < G < -20 dB) Gain
NF < 24.75 -0.4875* G (-20 ≤ G ≤ +20 dB)
NF < 15 (20 < G < 40 dB)

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Figure 15. Q5505 Cascaded IIP3 Model

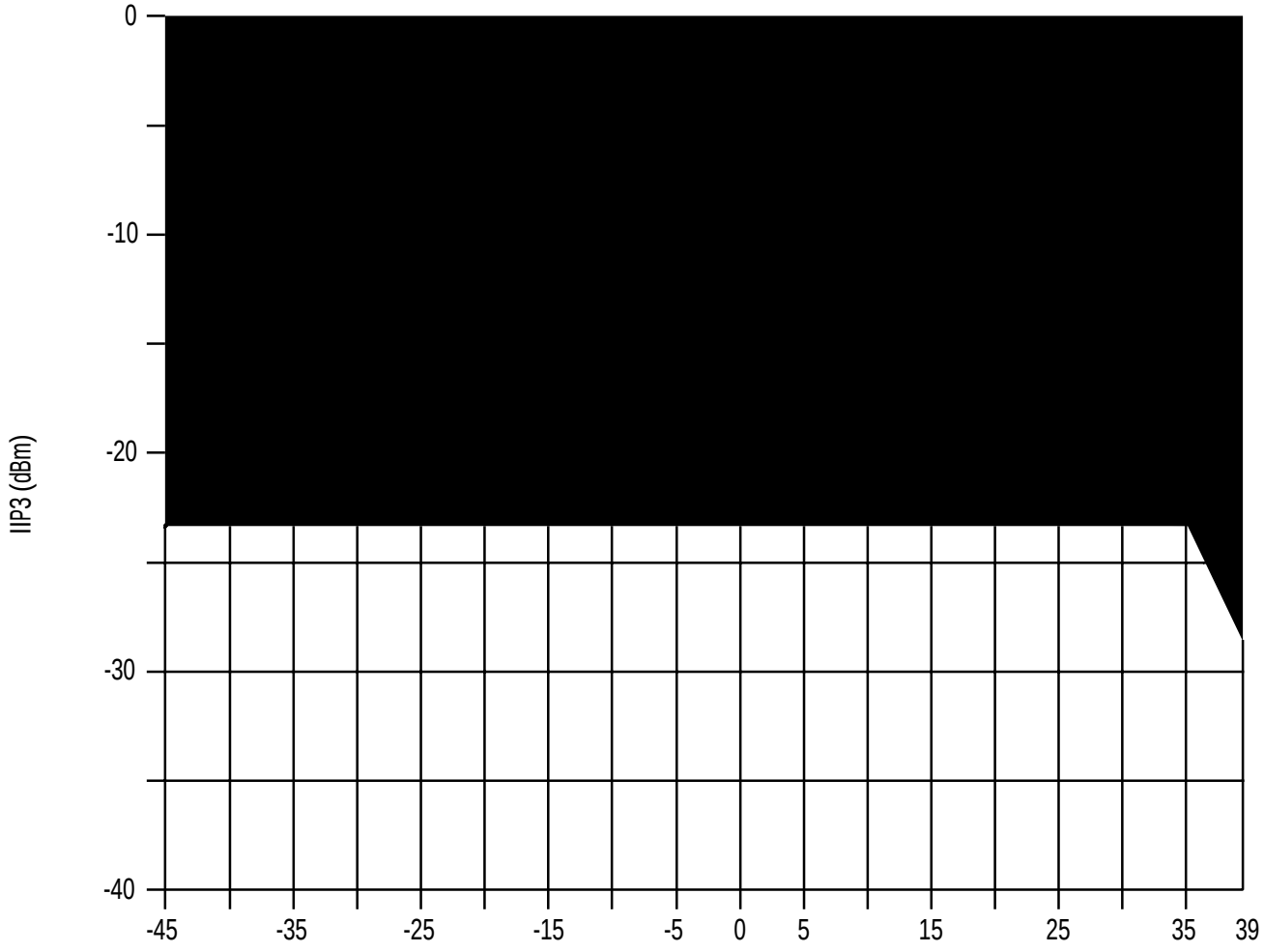

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Table 11a-e. Description of Q5505 Pin Functions

a. Hi-Gain Digital Mode Differential Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
IN +	1	Differential Input	Positive Differential Input
IN –	2	Differential Input	Negative Differential Input

b. Analog Gain Control Input Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
$V_{CONTROL}$	16	DC Input	$V_{CONTROL}$ = Analog Gain Control Input $V_{CONTROL}$ = 0.1 V, Low Gain Rail, $V_{CONTROL}$ = 3.0 V, High Gain Rail

c. Analog Differential Output Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
OUT +	10	Differential Output	Analog Positive Differential Output
OUT –	9	Differential Output	Analog Negative Differential Output

d. Unconnected Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
–	8	N/C	Unconnected Pin

e. Voltage Supply Pin Functions

SYMBOL	PINS	I/O Type	FUNCTION
V_{CC}	13, 14, 15	Power	V_{CC} Power Supply
GND	3, 4, 5, 6, 7, 11, 12	Ground	Ground Connection

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Figure 16. Q5505 Functional Block Diagram

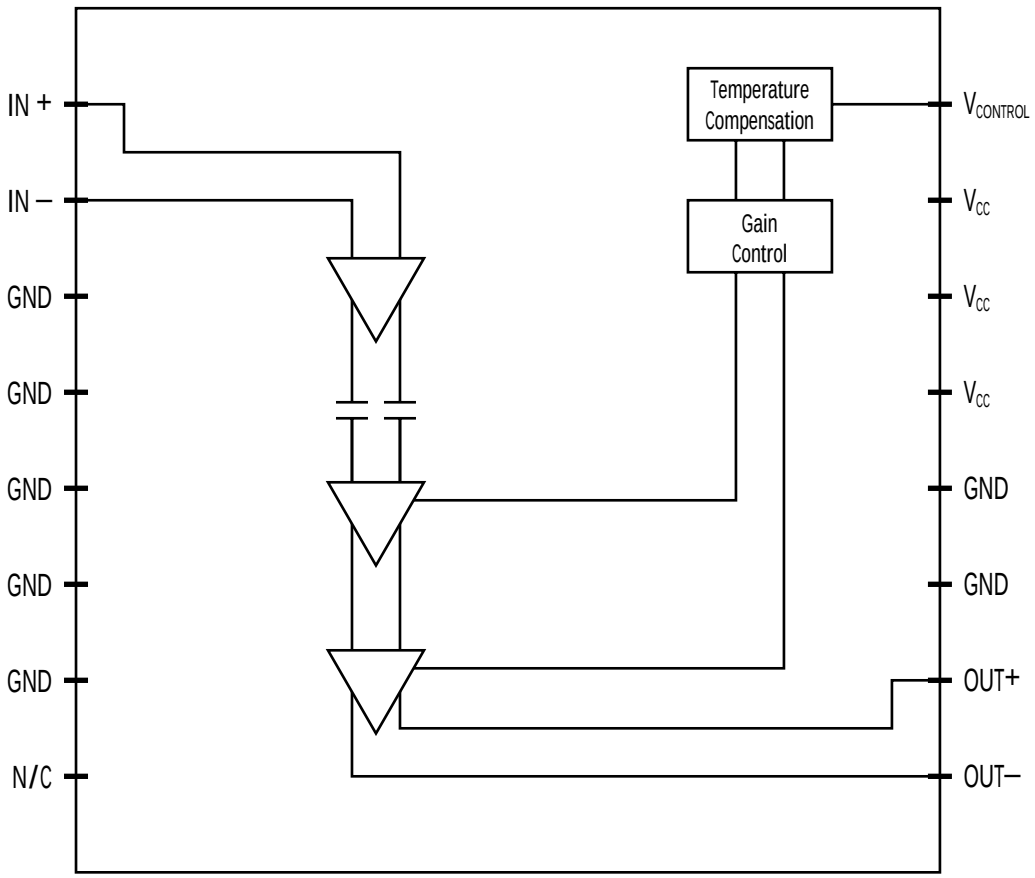

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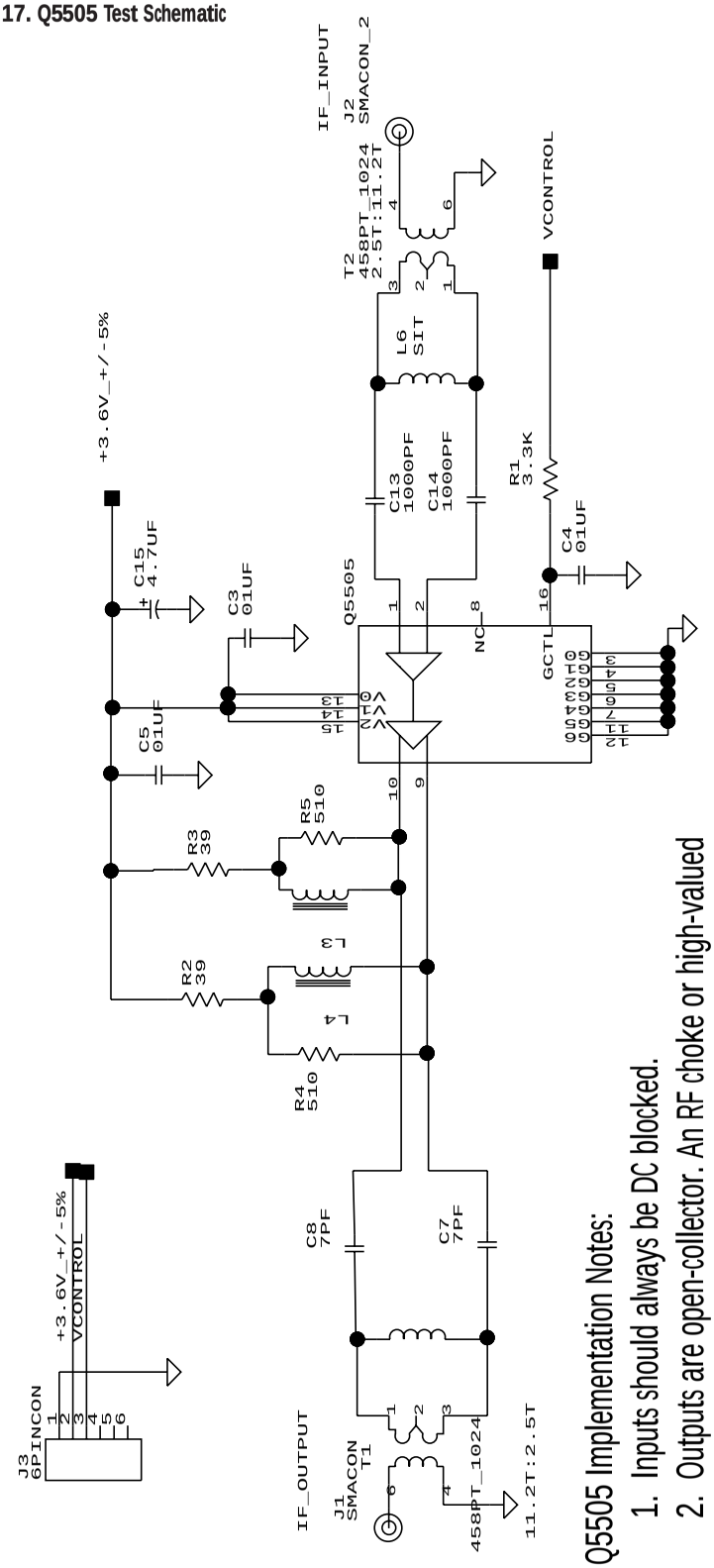
Figure 17. Q5505 Test Schematic



Q5505 Implementation Notes:

1. Inputs should always be DC blocked.
2. Outputs are open-collector. An RF choke or high-valued inductor is needed to provide DC bias to the output pins. Because the outputs are biased to V_{CC}, a DC blocking capacitor must be used if the next stage's input has a DC path to ground.
3. The input/output interface may require matching networks, however this requirement is very system dependent. The bias inductor is typically incorporated in the matching network between the output and next stage.
4. V_{CC} inputs should be bypassed to ground with about a 0.01µF capacitor, keeping trace connections to a minimum length.

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INPUT IMPEDANCE MATCHING

As with all active and passive components in the signal paths of the RF subsystem, the impedance levels in the signal path should be controlled and matched to minimize losses. The input impedance of the CDMA inputs to the Q5500 and Q5505 is specified as 1000 Ω ±15%. When driving the Q5500 from a 500 Ω differential source impedance, a 1000 Ohm resister should be connected between the IN+ and IN- inputs. This will set the effective input impedance to 500 Ω ± 8% (assuming a stable and accurate 1000 Ω external resister).

The FM inputs of the Q5500 are differential but may be used with a single-ended input signal. In the single-ended case, pin 5 should be connected to ground through a 0.01 µF capacitor. This causes pin 5 to be an AC ground pin. The single-ended input impedance for the FM+ input is 850 Ohms ±15%. If driven from a 500 Ω source, an external resistor of 1.2 kΩ connected between the FM+ input and ground will set the effective single-ended FM input impedance to 500 Ω ±10%.

The Q5500 and Q5505 amplifiers include temperature-compensated input biasing circuits that maintain the DC input level of the IN+, IN-, FM+ and FM- inputs. The application circuit should AC-couple the IF signals into the AGC amplifiers. No DC biasing circuits are required.

OUTPUT IMPEDANCE MATCHING

The output devices of the Q5500 and Q5505 OUT+ and OUT- pins are open-collectors of NPN transistors. This allows the differential output impedance (the impedance between the OUT+ and OUT- pins) of the amplifier to be set to various levels and controlled by external components. The open-collector outputs require a DC path to VCC. The DC path requirement is satisfied by connecting either a resistor or an inductor between the OUT pin and VCC.

Resistive collector loads on the OUT+ and OUT- pins set the differential output impedance to the sum of the two load resistors. For example, if 250 Ω resistors are used for developing the output signal, the differential output impedance of the circuit will be (250 + 250) = 500 Ω. Resistive loads on the open collector outputs have disadvantages. Current flowing through the resistors carries with it a component at the IF frequency. This high-frequency component can add to power supply noise and require a more complex power supply decoupling network. Additionally, noise already on the power suppy voltage may be injected into the IF output signal through the collector load resistors.

An alternate method for loading the open-collector outputs of the AGC amplifiers is to employ relatively high-inductance “chokes” instead of resistors (see Figures 18 and 19). An inductor between the OUT and VCC pins meets the DC path requirement but blocks the IF frequency from the power supply voltage and blocks power supply noise from the amplifier’s output signal. Inductor values on the order of 2.7 µH work well here. Inductive loads do not significantly contribute to the differential output impedance because their reactance at IF frequencies is high. When using inductive loads, the differential output impedance is set by connecting a resistor between the OUT+ and OUT- pins. The value of the resistor becomes the differential output impedance.

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Figure 18. Application Schematic for the Q5500 Rx AGC Amplifier

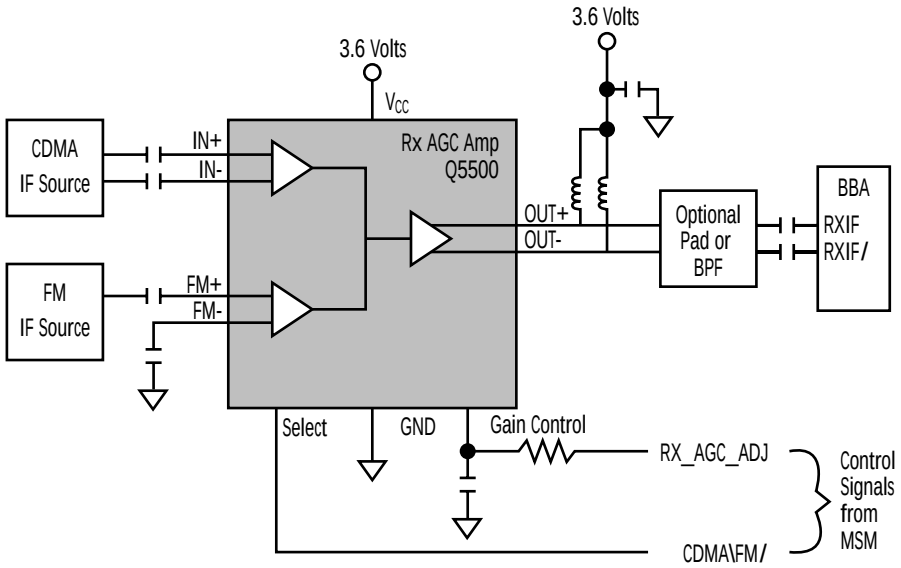
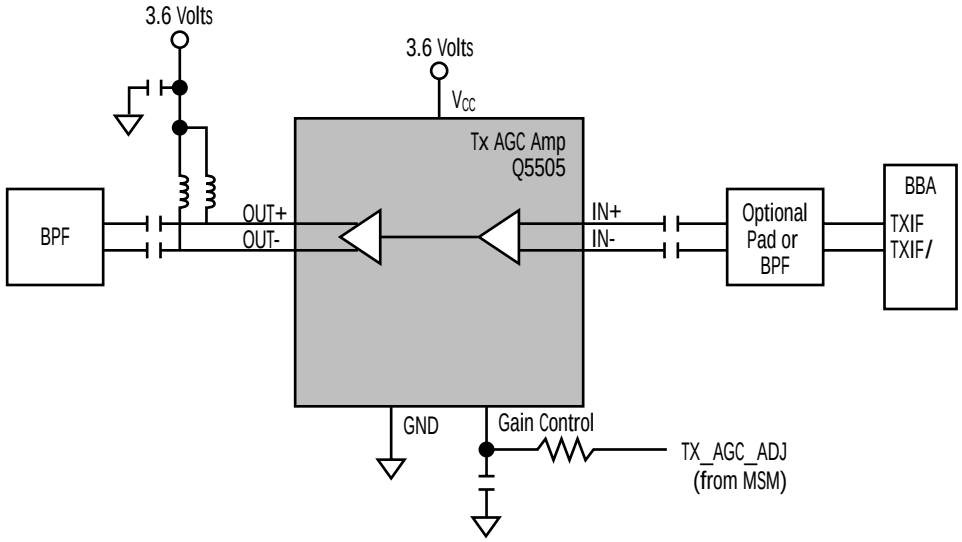


Figure 19. Application Schematic for the Q5505 Tx AGC Amplifier



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CDMA APPLICATIONS

The AGC circuits are critical in maintaining consistent power levels with the changing distances between subscriber handsets and base stations in a cellular network. Figure 20 shows the basic distribution of control signals from the Mobile Station Modem (MSM) RF interface to the Analog Baseband Processor (BBA) and AGC components in the analog and RF sections of the QUALCOMM subscriber unit. The RF interface of the MSM is made up of several completely digital circuit blocks that monitor and control analog parameters. One of the important functions of the RF interface of the MSM is analog signal gain control. The RF interface communicates with the BBA and AGC circuits via Pulse Density Modulation (PDM). PDM signals require only 2 passsive components, a resistor and a capacitor, to provide a low-ripple DC control voltage for the Q5500/Q5505 VGAs and other analog circuit functions.

The basic structure of the Rx AGC loop (lower half of Figure 20) is the same as the architecture of the general AGC loop except that all of the functions such as RSSI estimation and generation of the VGA control voltage ($V_{CONTROL}$) are done by digital circuits. The Rx Signal-to-Noise Ratio (SNR) in the subscriber unit is optimized by controlling the gain of analog RF and IF stages in the receive signal path. CDMA receivers must operate over input signal strengths that range from -113 dBm to -25 dBm. The Rx AGC loop varies the Q5500 amplifier gain to compensate for the variation in power level of the incoming RF. The purpose of the receive AGC loop is to keep the signal amplitude high and power level consistent at the demodulator input without distorting and overdriving the demodulator. The Q5500's gain range of -45 to +45 dB attenuates or amplifies the IF signal so that the power level of the I and Q components at the input to the CDMA demodulator is constant. The Q5500 is required to operate in both FM and CDMA Modes. The main difference between FM and CDMA Modes is that the linearity requirement is less stringent for FM than for CDMA. Also, the FM input is single-ended while the CDMA input is balanced. The gain control section of the Q5500 processes the gain control voltage, $V_{CONTROL}$, so the overall IF signal gain, measured in dB, is approximately a linear function of $V_{CONTROL}$ and also provides temperature compensation.

The CDMA transmit AGC loop is part of the power control system that distinguishes CDMA from other multiple-access telecommunications protocols. The Tx AGC loop (upper half of Figure 20) is closed by communication with the base station. In CDMA, the base station controls the RF power output of all subscriber units. The signal strength of the subscriber unit is measured at the base station and varies widely due to the changing distance from the subscriber unit to the base station, multipath fading, terrain topology, and environmental conditions. The purpose of the Tx AGC control loop on the MSM is to provide a linear variable RF output power level to the subscriber unit antenna to compensate for these effects. The subscriber unit receives power control information from the base station which increases or decreases the subscriber unit Tx power. The base station maintains the Tx power level of each subscriber unit in the cell so that the received power from each subscriber unit is the same. For both CDMA and FM Modes in the subscriber unit, the Q5505 is the primary gain control element in the Tx signal path between the BBA and the upconverter. The signal which controls the gain of the Q5505 is a lowpass filtered PDM signal obtained from the MSM. The linearity of the VGA used in the path of a CDMA transmit AGC loop is typically depicted with an Adjacent Channel Power Rejection (ACPR) response to an input CDMA waveform. This provides a figure of merit for evaluating a VGA's nonlinearity at various gain settings. Figure 21 shows the Q5505's typical ACPR response at higher operating gains where device linearity is stressed the most.

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Figure 20. CDMA Subscriber Unit Simplified Block Diagram

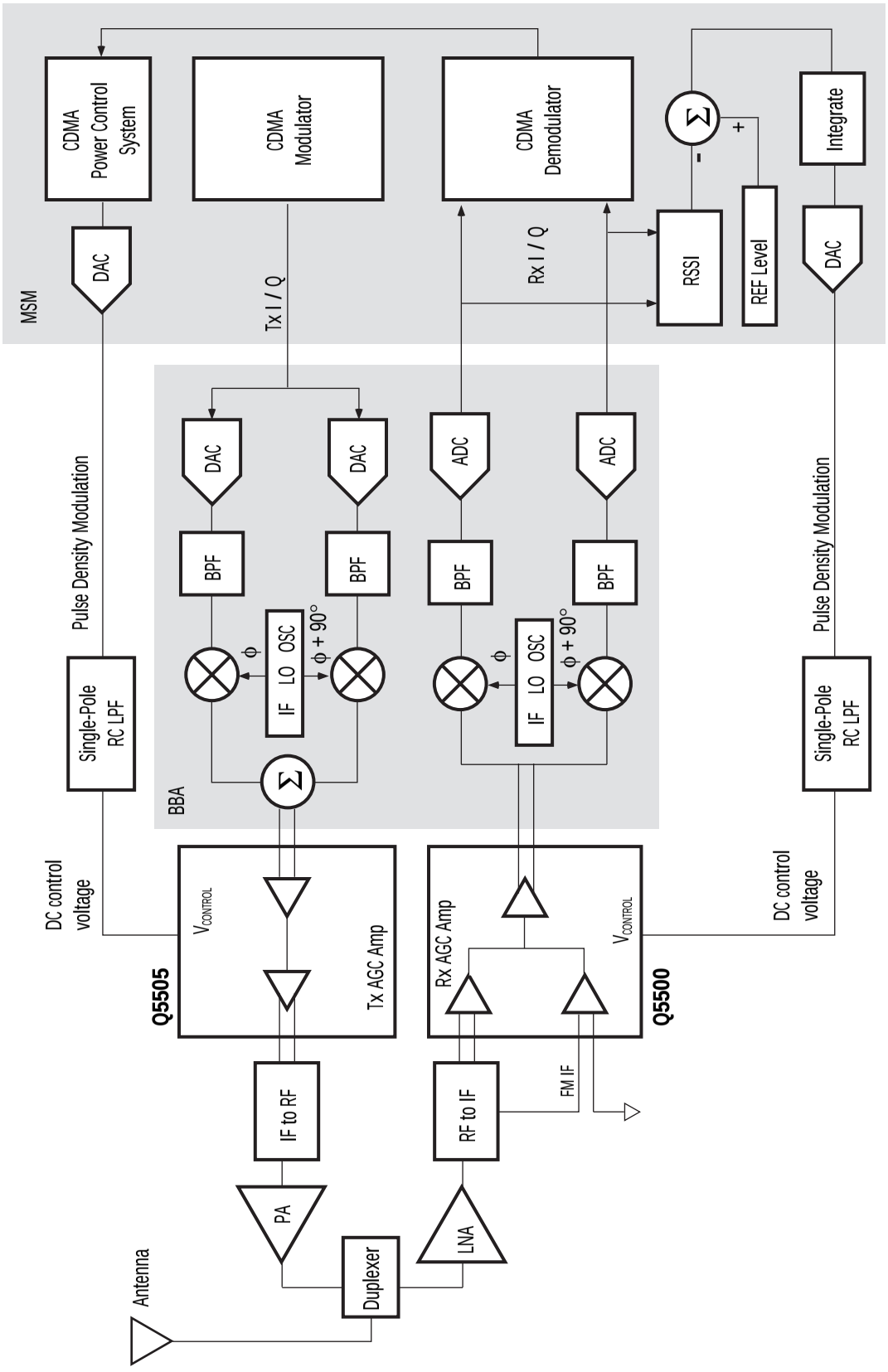

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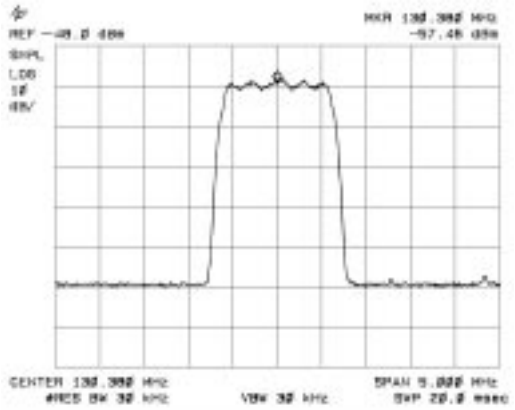
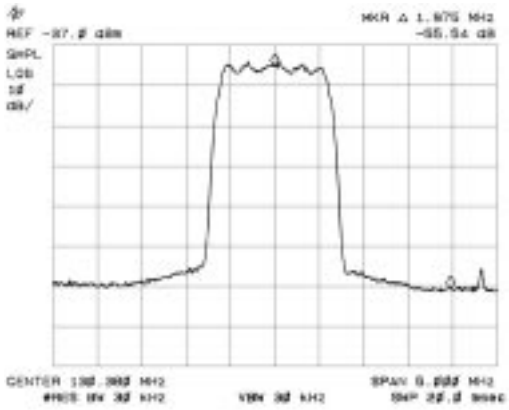
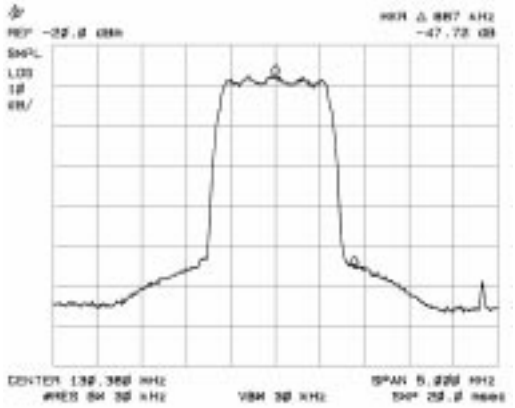
Figure 21a-d. Adjacent Channel Power Rejection (ACPR) Response of Q5505 to CDMA Waveform



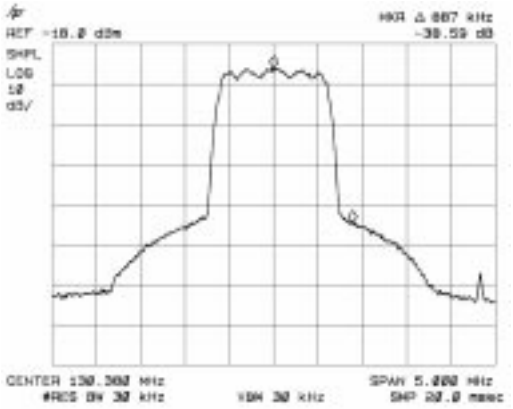
a. CDMA Input to Q5500



b. ACPR Response @ G = + 20 dB



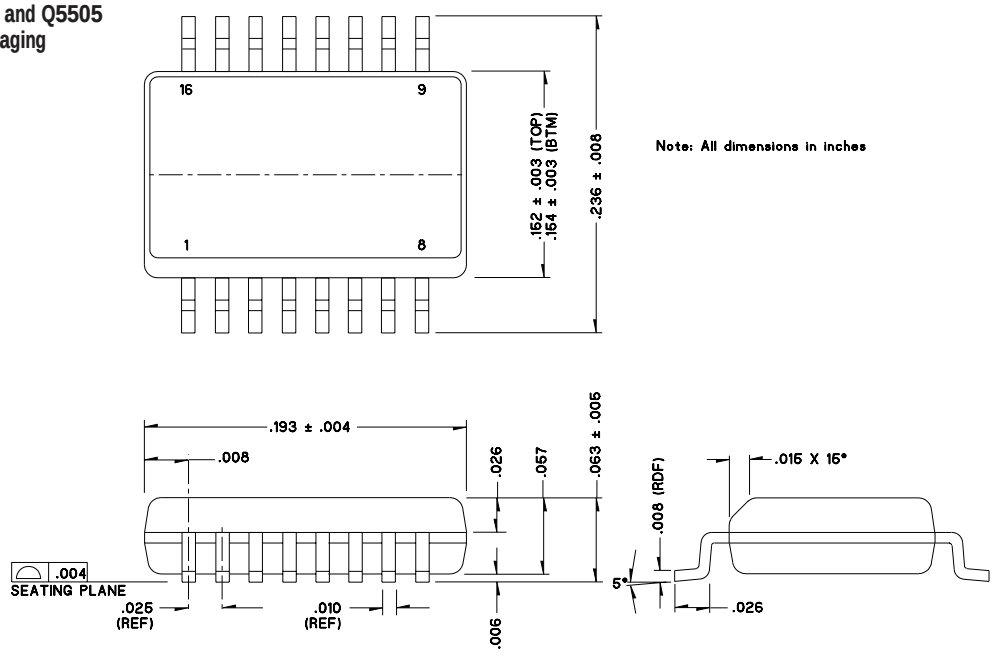
c. ACPR Response @ G = + 35 dB



d. ACPR Response @ G = + 39 dB

Test Conditions: Input Power @ - 42.2 dBm
VCC Supply @ 3.6 V

Figure 22. Q5500 and Q5505 16-pin SSOP Packaging



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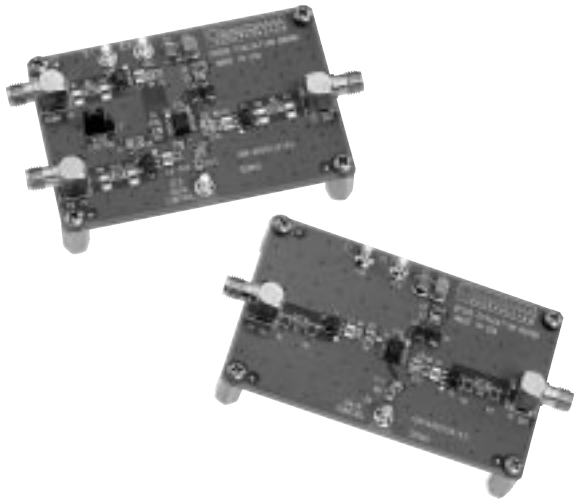
Q0500 RX AGC EVALUATION BOARD / Q0505 TX AGC EVALUATION BOARD

USER'S GUIDE



CONTENTS

1.0 INTRODUCTION

The Q0500 Receive and Q0505 Transmit Automatic Gain Control (AGC) Amplifier Evaluation Boards are compact printed circuit card assemblies designed specifically to demonstrate the performance of the QUALCOMM Q5500 Rx and Q5505 Tx AGC amplifiers. These general purpose linear IF (Intermediate Frequency) AGC amplifiers function in many wireless applications including analog cellular systems, cordless telephones, specialized mobile radios, wireless data systems and digital cellular systems.

The Q0500 Receive AGC Evaluation Board consists of separate analog and digital differential input signal paths which are selectable via a mode control jumper. The Q0505 Transmit AGC Evaluation Board consists of a single differential signal path. Amplifier gain for both boards is established by a voltage applied to the Gain Control input. The Q0500 and Q0505 are powered by a +3.6 V power supply. All IF inputs and outputs are matched to 50 Ω impedance to maximize power transfer throughout the signal path.

Minimal equipment is needed to demonstrate the functionality of the evaluation board, and to verify the high degree of linearity of the Q5500 and Q5505 AGC amplifiers over their wide dynamic range. The Q0500 and Q0505 Evaluation Boards are useful for measuring and verifying gain versus control-voltage performance of the Q5500 Receive and Q5505 Transmit AGC amplifiers. Both evaluation boards can be used as functional AGC modules or as daughter boards within a larger phone reference design.

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2.0 GETTING STARTED

It is very simple to demonstrate the performance of the Q0500 and Q0505 Evaluation Boards. An IF/RF signal is applied to the board's input via a signal generator. This signal is either amplified or attenuated by the AGC amplifier by means of a control voltage applied to the board's Gain Control input. The amplifier's output signal is then measured by a spectrum analyzer. Test signals enter and exit the board via coax cables with SMA connectors. Power is supplied to the V_{CC} and Gain Control pins via separate power supplies. Functional block diagrams of the Q0500 Evaluation Board with its associated test equipment are shown in Figures 1 (CDMA input) and 2 (FM input). A similar block diagram of the Q0505 Evaluation Board and equipment is shown in Figure 3.

Figure 1. Q0500 Rx AGC Functional Block Diagram, CDMA Mode

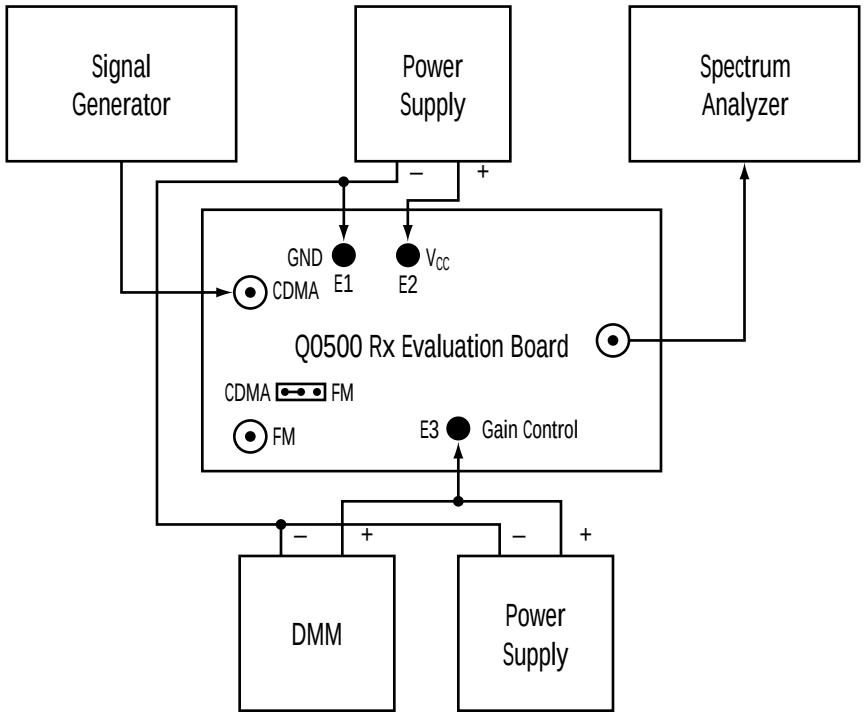

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Figure 2. Q0500 Rx AGC Functional Block Diagram, FM Mode

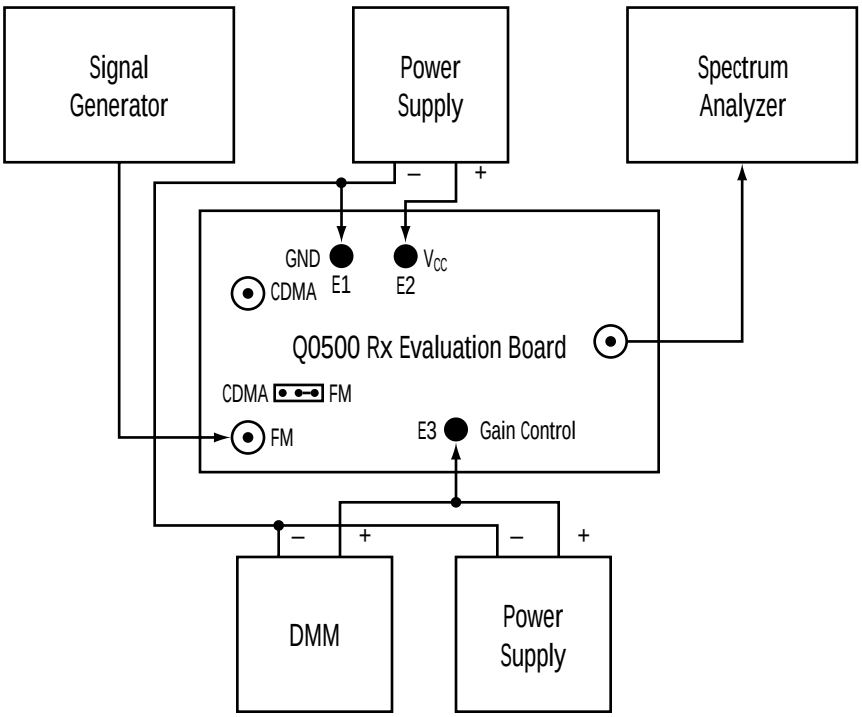
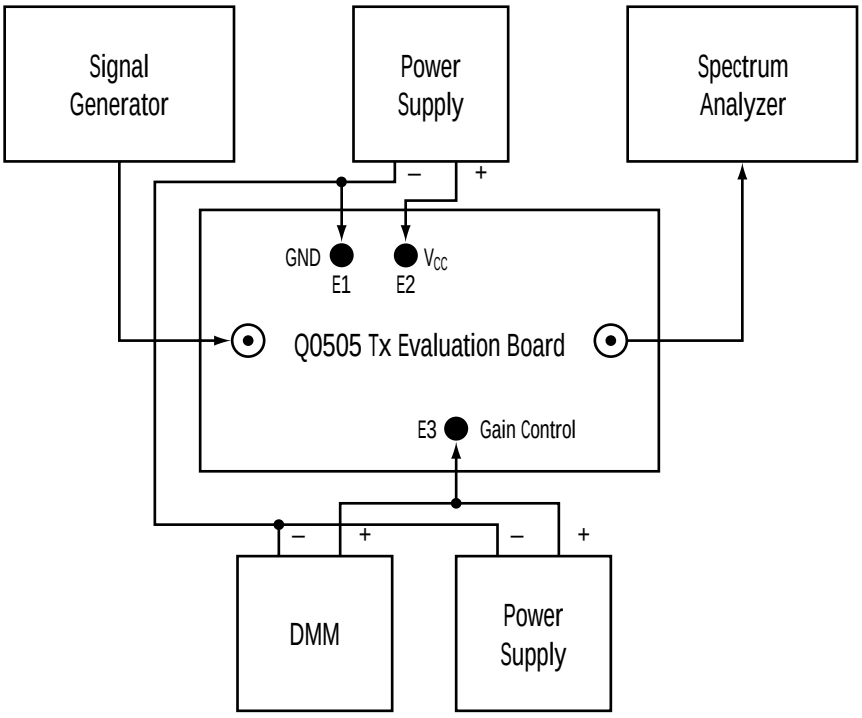


Figure 3. Q0505 Tx AGC Functional Block Diagram



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2.1 EQUIPMENT REQUIRED

The Q0500 and Q0505 Evaluation Boards come fully configured for operation with minimal assembly. The following list of standard test equipment is provided as a baseline. If specific equipment is not available, equipment with equivalent functionality may be substituted.

Spectrum Analyzer	Advantest R3361B
Signal Generator	HP8648C
Power Supplies (2)	Leader LPS-152
Digital Multimeter (DMM)	HP34401A
Coax cables (2)	With SMA connectors and signal generator/spectrum analyzer fittings
Pair of test leads (3)	With banana fittings on one end and grabbers on the other

2.2 Q0500 AND Q0505 EVALUATION BOARD SETUP

Power supplies and test equipment should be connected to the appropriate evaluation board as shown in Figures 1, 2 or 3. The Q0500 offers a choice of either CDMA or FM input signal paths. Figure 1 shows the Q0500 setup using the CDMA signal path, while Figure 2 shows a comparable setup using the FM signal path.
Figure 3 illustrates the setup of the Q0505. One coax cable is connected between the board's input SMA (Q0500 - J1 or J4; Q0505 - J1) and the signal generator. The other coax cable is connected between the board's output SMA (Q0500 - J3; Q0505 - J2) and the spectrum analyzer. An input signal via the CDMA signal path is applied to the Q5500 amplifier differentially, whereas a signal in the FM signal path is applied single ended (differentially with one end AC grounded). For the Q0500, the Mode Control Jumper (J2) is positioned to the CDMA or FM position corresponding to the CDMA or FM signal path selected. A +3.6 V power supply voltage is applied to the turret labeled VCC (E2), and 0.1 to 3.0 V to the turret labeled GAIN CONTROL (E3). For both V_{CC} and Gain Control power supplies, the ground terminal of each supply should be connected to the turret labeled GND (E1).

Before applying power, verify that V_{CC} is set at +3.6 V and that the Gain Control voltage is set to less than 3.0 V. The spectrum analyzer and signal generator yield more accurate measurements if they have temperature stabilized.

3.0 EVALUATION BOARD OPERATION

Figures 4 and 5 show the Q0500 and Q0505 Evaluation Board block diagrams. The following paragraphs describe the function and operation of the circuit elements of each board. Unless otherwise specified, the functionality, operation and pin designation of individual circuit elements are identical for both the Q0500 and Q0505 Evaluation Boards.

Figure 4. Q0500 Rx AGC Evaluation Board Block Diagram

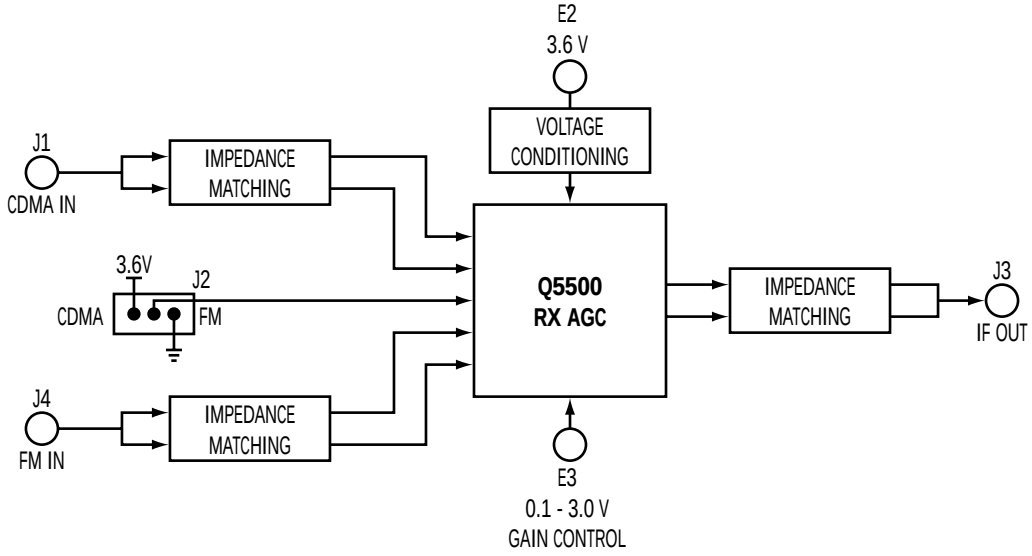
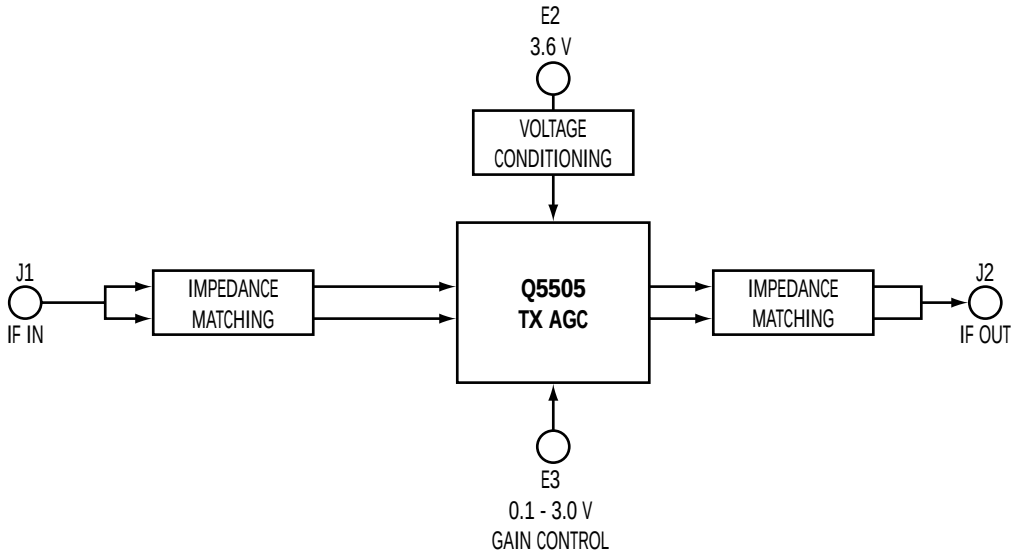


Figure 5. Q0505 Tx AGC Evaluation Board Block Diagram



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3.1 INPUTS

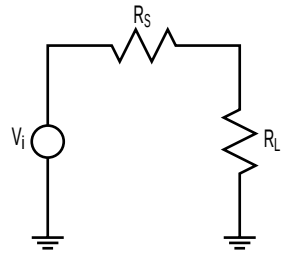
3.1.1 POWER SUPPLY REQUIREMENTS

One dual or two single variable voltage (50 mA capability) power supplies are required to operate the Q0500 or Q0505 AGC Evaluation Boards. One supply provides 3.6 V to V_{CC} and the other supplies 0.1 to 3.0 V to the Gain Control pin on the evaluation board. There are no visual indications on the evaluation boards showing that power has been applied or that it is at the appropriate voltage level. Supply voltage is conditioned by on-board inductors and capacitors to filter unwanted noise and to isolate the signal path from the power supply.

3.1.2 POWER TRANSFER TO THE Q0500 / Q0505

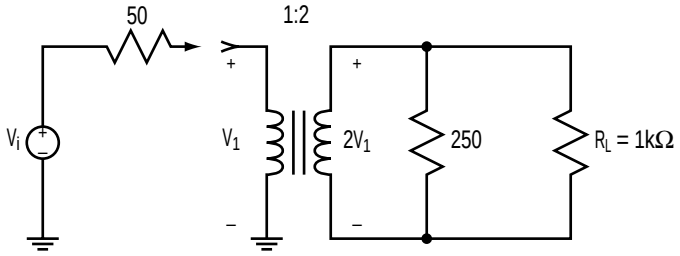
An RF signal applied to either the Q0500 or Q0505 will experience power loss due to the impedance mismatch between the 50 Ω signal source and the 1000 Ω input impedance (Q0500: FM = 850 Ω) of the AGC amplifiers. To minimize power loss due to impedance mismatch, a resistive matching network, consisting of a transformer and parallel resistor, has been designed into the input stage of both the Q0500 and Q0505. The loss due to each transformer is approximately 0.7 dB. Resistors (R4 and Q0500-R12) were added in parallel with the input impedance of the AGC amplifier to bring the equivalent parallel resistance to 200 Ω. When transformed down by means of the 2-to-1 turns ratio transformer, the 200 Ω impedance is matched to 50 Ω. Combined power losses due to the transformer and resistive matching network are calculated to be approximately 7 dB. Figure 6 shows the impedance matching network and power loss calculations.

Figure 6. Impedance Matching Network and Power Loss Calculations



P_{MAX} when $R_S = R_L$

When $R_S = 50\ \Omega$:



$$P_{LOSS} = P_{TOT} - P_{LOAD}$$

$$P_{LOSS}\ dB = 10 \log \left[\frac{P_{TOT}}{P_{LOAD}} \right]$$

$$P_{TOT} = \frac{V_1^2}{50}$$

$$P_{LOAD} = \frac{(2V_1)^2}{1000}$$

$$P_{LOSS}\ dB = 10 \log \left[\frac{\frac{V_1^2}{50}}{\frac{V_1^2}{250}} \right] = 7dB$$

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3.1.3 Q0500 / Q0505 CURRENT CONSUMPTION

Evaluation board current consumption was measured by connecting ammeters in series with the V_{CC} and Gain Control power supplies for CDMA and FM Modes of operation (Q0505-only IF Mode). Maximum current consumed by the Q0500 and Q0505 Evaluation Boards is provided in Table 1.

Table 1. Maximum Current for 0.1 to 3.0 V Tuning Voltage

DEVICE	OPERATION MODE	CURRENT DRAWN (MAX)
Q0500	CDMA	11.0 mA ± 5%
Q0500	FM	11.5 mA ± 5%
Q0505	–	20.0 mA ± 5%

3.2 OUTPUTS

3.2.1 POWER TRANSFER TO THE OUTPUT

Minimum output impedance of the Q5500 and Q5505 amplifiers is 5 kΩ and 10 kΩ, respectively. In order to maximize the power transferred to the spectrum analyzer, amplifier output impedance must be matched to the input impedance of the device or load receiving the signal, in this case, the spectrum analyzer. Similar to the impedance matching performed at the input to the AGC amplifiers, a transformer and resistor in parallel with the amplifier's output impedance have been added to the output of the AGC amplifiers to match to 50 Ω at the input to the spectrum analyzer.

3.2.2 TUNING VOLTAGE

Q5500 and Q5505 AGC amplifier gain is controlled by applying power supply voltage to the GAIN CONTROL turret (E3) on the Q0500 and Q0505 Evaluation Boards. A control voltage from 0.1 to 3.0 V produces from 45 dB of attenuation to 45 dB of amplification in the Q5500, and from 45 dB of attenuation to 40 dB of amplification in the Q5505. Low-pass filtering between the GAIN CONTROL turret and the input pin to the Q5500/Q5505 amplifiers allow pulse density modulated (PDM) signals to be used in substitution for a supply voltage. PDM signals are a series of fixed-width pulses that vary in density with time. Low-pass filtering of PDM signals presents an averaged DC voltage level to the gain control input of the amplifier and establishes the amplifier gain setting.

3.2.3 TUNE VOLTAGE VERSUS GAIN

Both the Q5500 and Q5505 AGC amplifiers have gain response that is nearly linear over the amplifier's published operating frequencies of 10 MHz to 300 MHz. Figures 7 through 12 show the Q0500/Q5500's and Q0505/Q5505's near linear gain response over the full dynamic range of the amplifiers.

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Figure 7. Q0505 Narrow Band Response

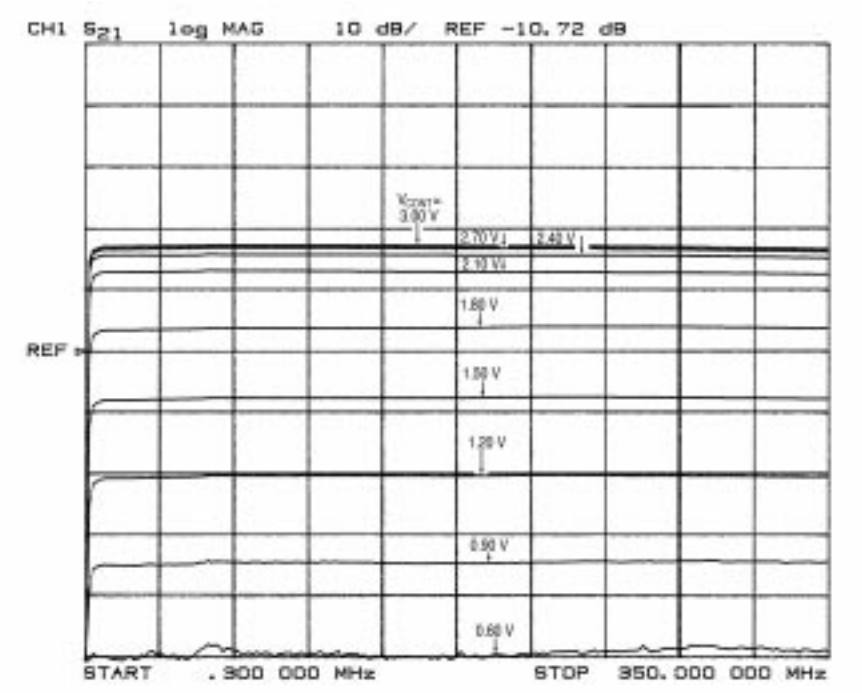

Figure 8. Q0505 Wide Band Response

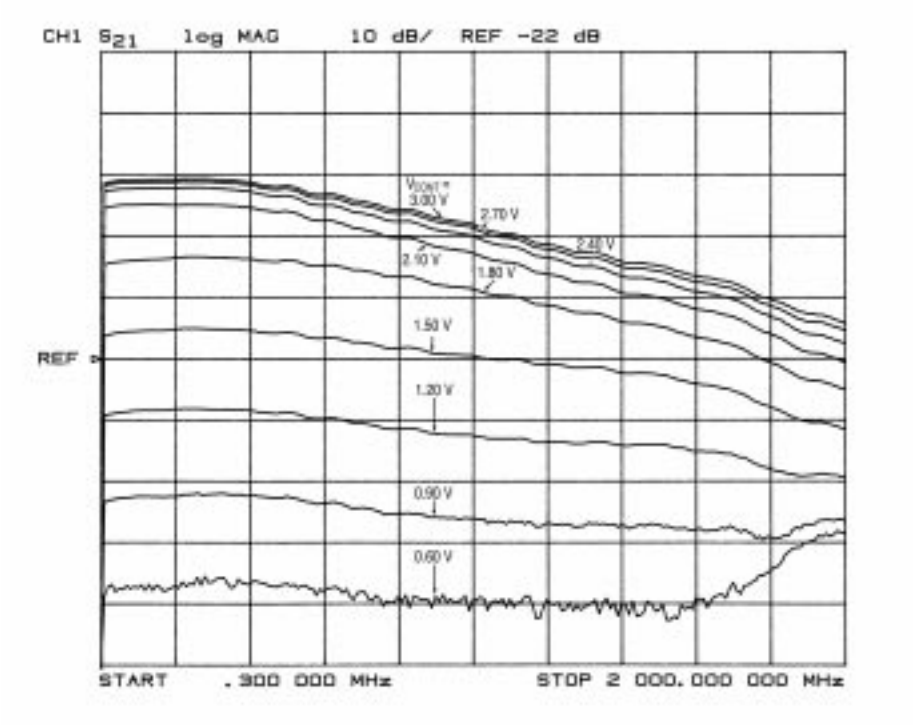

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Figure 9. Q0500 CDMA Channel Narrow Band Response

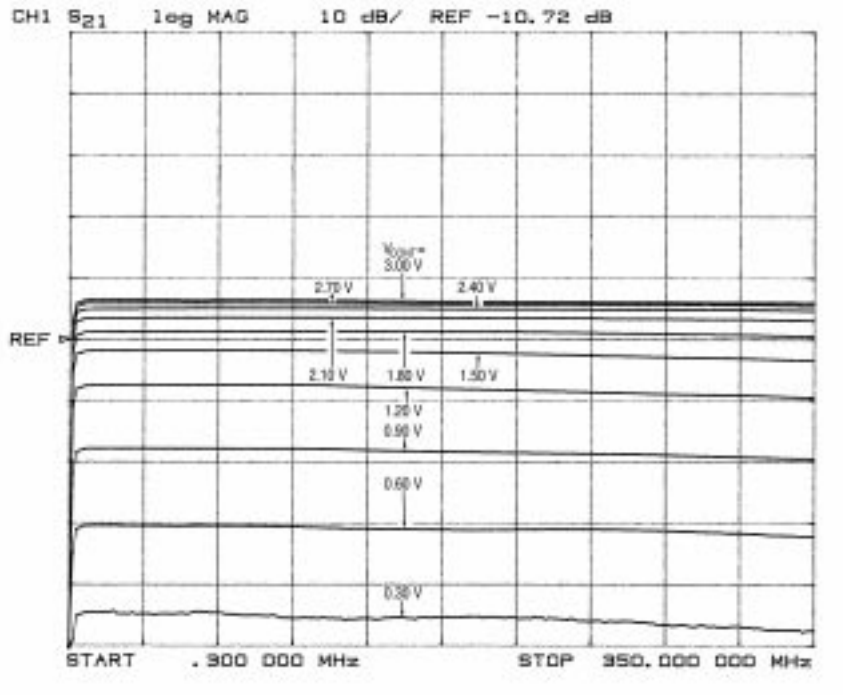

Figure 10. Q0500 CDMA Channel Wide Band Response

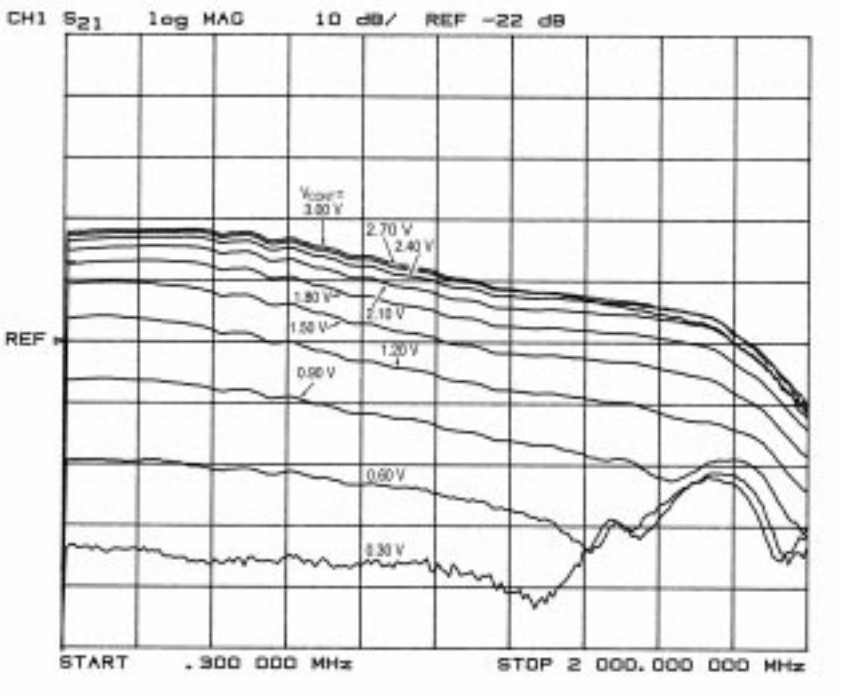

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Figure 11. Q0500 FM Channel Narrow Band Response

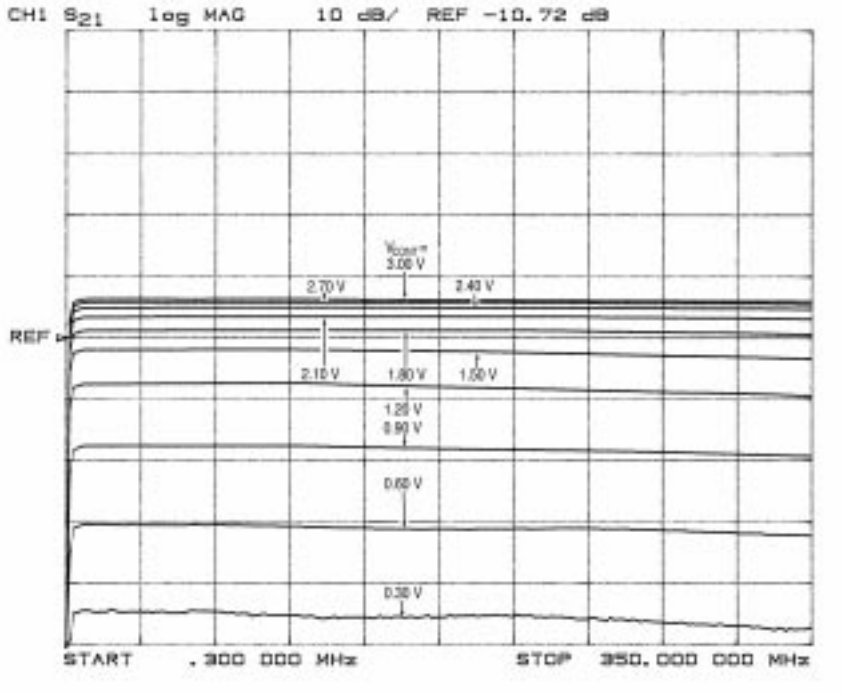
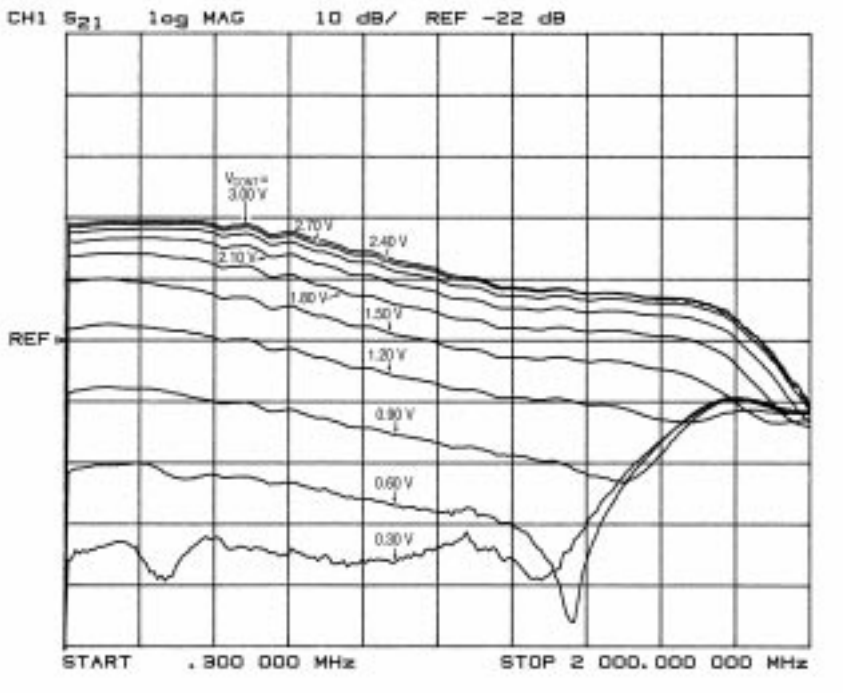


Figure 12. Q0500 FM Channel Wide Band Response



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3.2.4 Q0500 MODE CONTROL

The Q0500 Rx AGC Evaluation Board is configured with two separate signal paths, a differential path for CDMA and a single-ended path (differential with one side AC grounded) for FM. The desired CDMA or FM signal path is selected by placing the Mode Control Jumper (J2) in either the CDMA or FM position. Figure 13 and Table 2 show the Q0500 Mode Control Jumper and setting positions for CDMA and FM Modes of operation. The Q5505 amplifier and Q0505 Evaluation Board have only one signal path and therefore do not need mode control.

Figure 13. Q0500 Mode Control Jumper Setting Positions Diagram

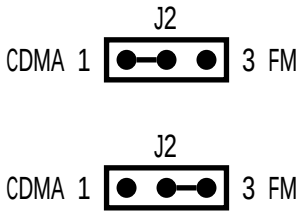

Table 2. Q0500 Mode Control Jumper Setting Positions

MODE	MODE JUMPER POSITION	VOLTAGE LEVEL
CDMA	1, 2	1 = V_{CC}, 2 = Sig Path
FM	2, 3	2 = Sig Path, 3 = GND

4.0 DESIGN HINTS

4.1 POWER SUPPLY CONSIDERATIONS AND DECOUPLING

The Q5500 and Q5505 AGC amplifiers are designed for use in battery operated portable phones. As such, the devices should be powered by regulated +3.6 V power supplies. In the Q0500 and Q0505 AGC Evaluation Boards, standard variable-voltage supplies provide satisfactory operation. In battery powered telephone applications, use of dedicated voltage regulation is strongly recommended. The voltage regulator used by the AGC should be a linear voltage regulator, not a switching regulator, to keep power supply noise on the inputs of the AGC amplifiers as low as possible. The recommended power supply voltage range of the Q0500 and Q0505 AGC Evaluation Boards is 3.42 V to 3.78 V (3.6 V ± 5%). It is recommended that the voltage regulator have a ±2% accuracy, so the proper output voltage can be maintained over the temperature range of the telephone and over the power supply current range of the AGC.

Power supply decoupling on the Q0500 and Q0505 is accomplished using a 0.01 µF ceramic chip capacitor on the V_{CC} pins. Additional 10 µF, 0.47 µF, and 1000 pF decoupling capacitors in parallel with the 0.01 µF capacitor, and a 100 nH choke inductor are used to further reduce noise on the power supply inputs to the AGC amplifiers. On the Q0500 and Q0505, the LC filtering elements just mentioned are arranged in a “pi” configuration as shown in Figure 14.

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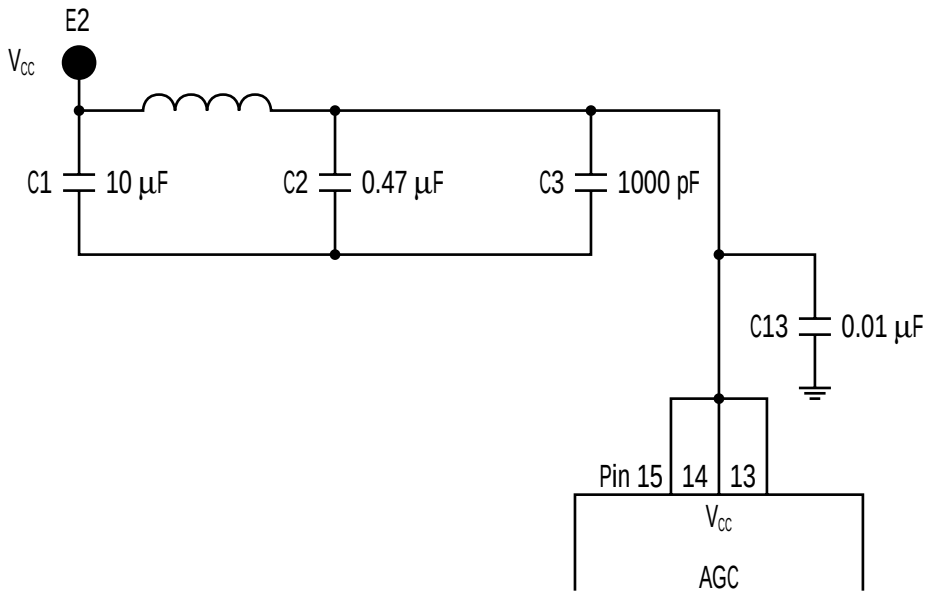
Figure 14. Power Supply LC Filtering Configuration



4.2 RF FILTERING AND ISOLATION

In order for the Q5500 and Q5505 AGC amplifiers to deliver both positive- and negative-going output signals using a single power supply, the differential AGC output pins must be DC-biased to a voltage level allowing full signal swing. In the case of the Q0500 and Q0505 Evaluation Boards, + 3.6 VDC biasing is applied to the amplifier output pins by means of RF-filtering 3.3 nH "chokes" or chip inductors connected between V_{CC} and the output pins. These two inductors provide an electrical connection for supply voltage to bias the amplifier outputs while isolating them from unwanted RF energy present at the power supply. The RF isolation also works to prevent AGC signal energy from contaminating the power supply, which may be sourcing power for other circuit blocks.

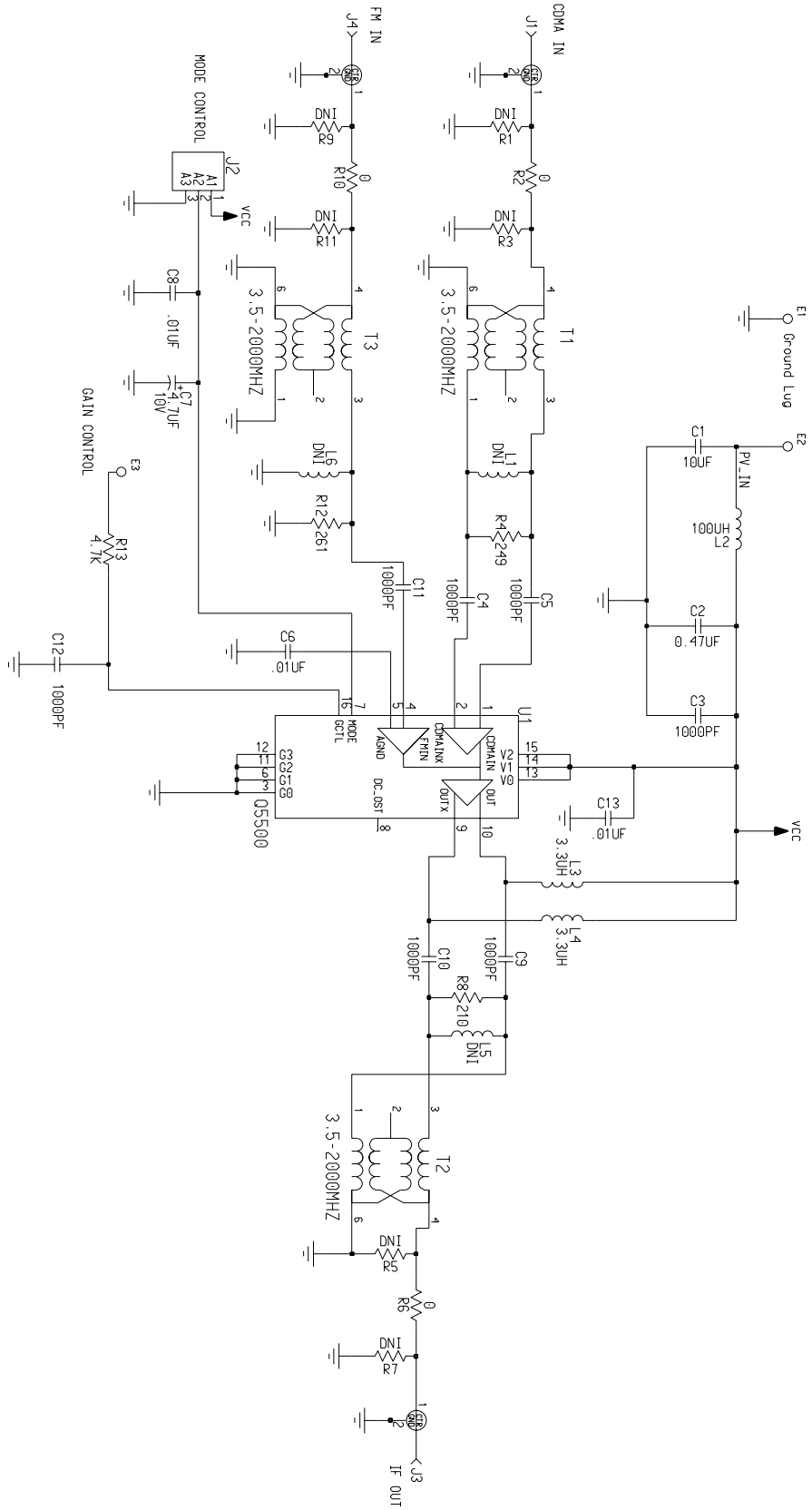
4.3 SPECIFIC FREQUENCY TUNING

The Q0500 and Q0505 Evaluation Boards are designed to provide maximum flexibility and optimal performance over the entire 10 MHz to 300 MHz bandwidth of the Q5500 and Q5505 amplifiers. Wideband performance is accomplished through the use of resistive impedance-matching elements, but is done so at the expense of power loss through the resistive elements. An alternative approach to impedance matching is to use an inductor (L1, L5; Q0500-L6) in parallel with the input/output impedance of the amplifier in place of the resistor (L1, L5; Q0500-R12). This approach offers improved power transfer by reducing I^2R losses due to the inductor's lower internal resistance. Using an impedance-matching inductor also serves to tune the circuit to a specific frequency based upon the inductive value chosen. The result is an impedance matched circuit which efficiently transfers power, but only at the tuned frequency. At all frequencies differing from the turned frequency, the transmitted or received signal will experience attenuation and loss of power.

5.0 APPENDIX

5.1 APPENDIX A SCHEMATICS

5.1.1 Q0500 RX AGC BOARD SCHEMATIC



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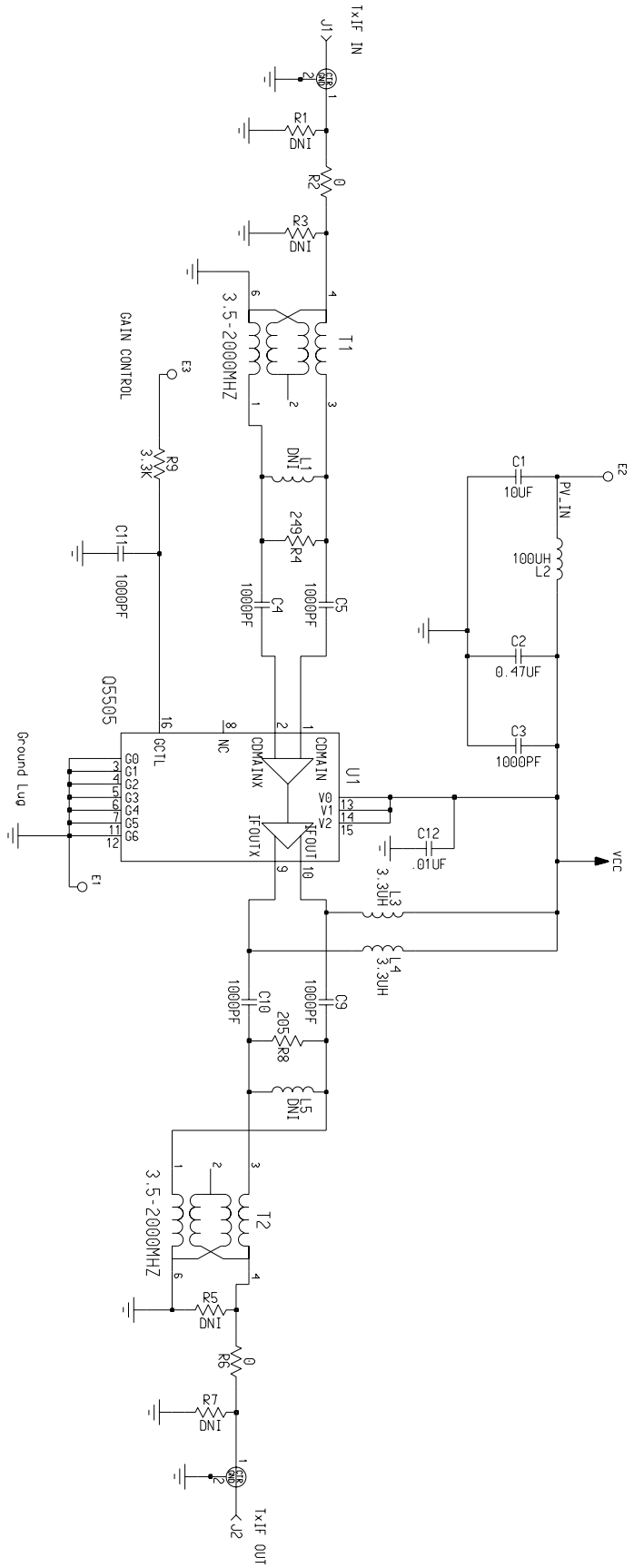
5.1.2 Q0505 TX AGC BOARD SCHEMATIC



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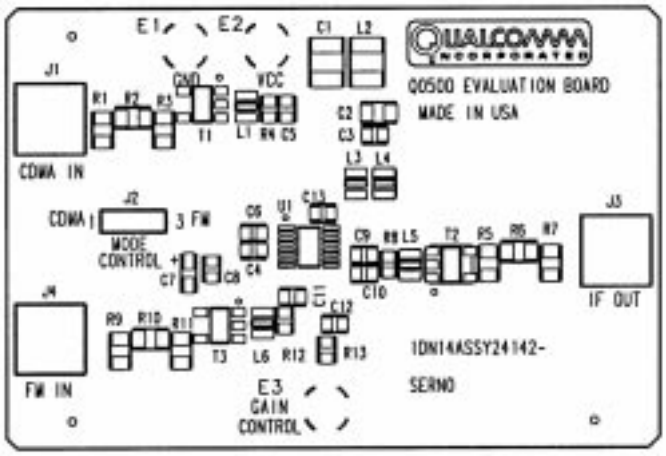
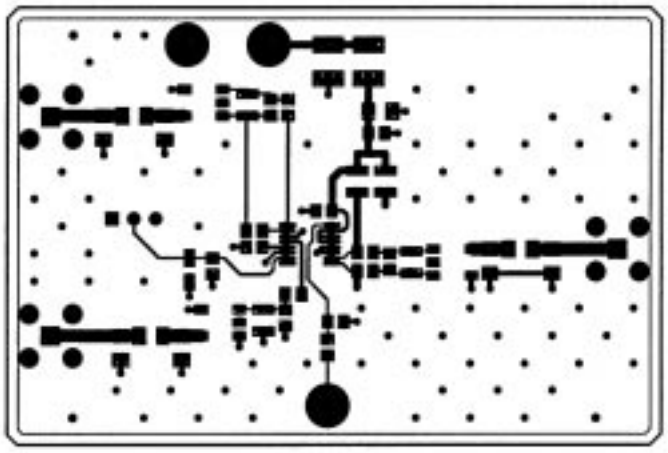
5.2 APPENDIX B LAYOUT DRAWINGS

5.2.1 Q0500 RX AGC BOARD LAYOUT DRAWINGS

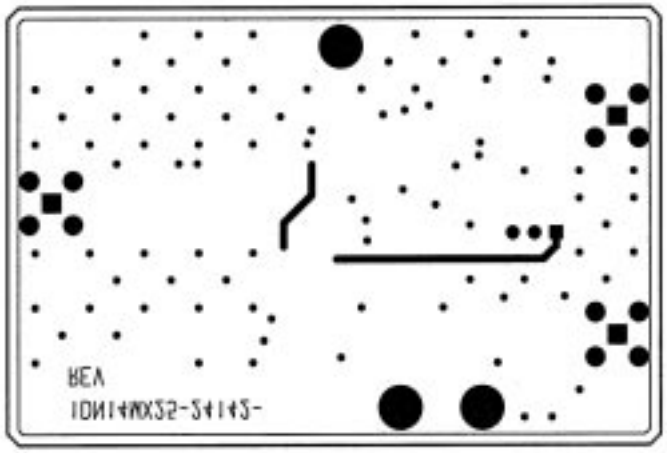
Q0500 Rx AGC Top Silk Layout



Q0500 Rx AGC Top Traces Layout



Q0500 Rx AGC Bottom Traces Layout



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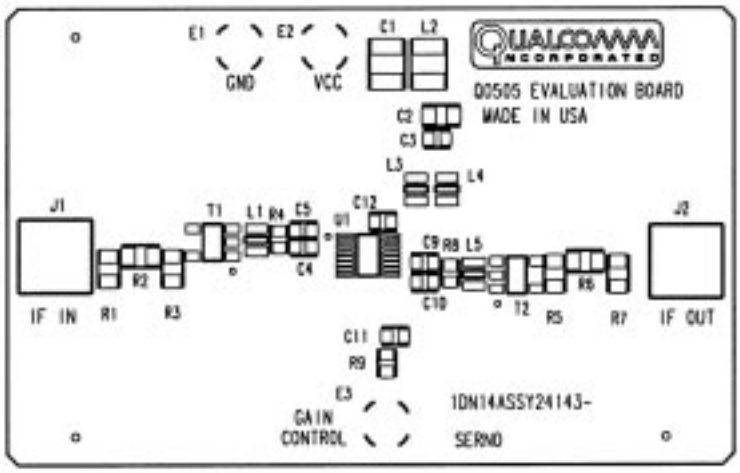
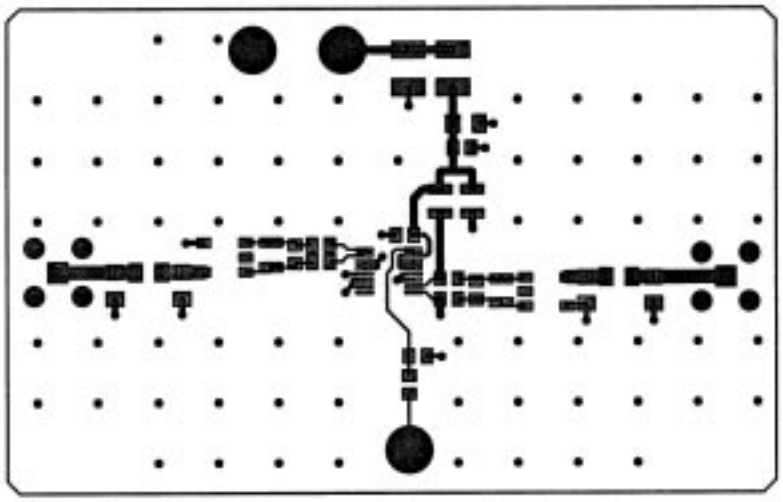
5.2.2 Q0505 TX AGC BOARD LAYOUT DRAWINGS

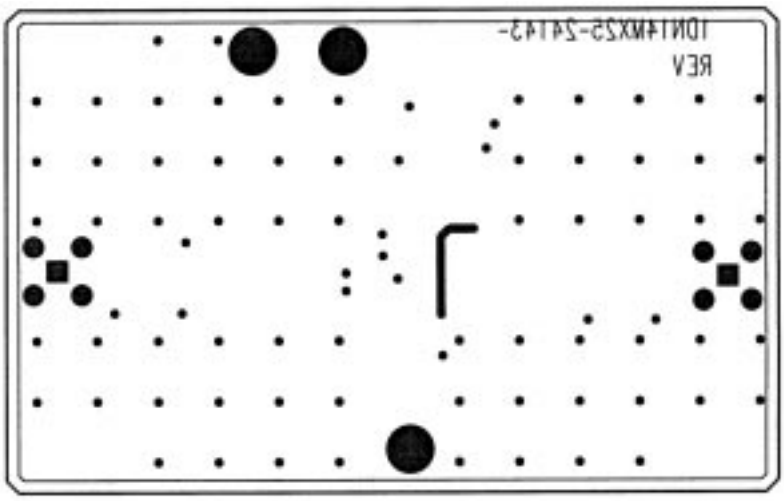
Q0505 Tx AGC Top Silk Layout



Q0505 Tx AGC Top Traces Layout



Q0505 Tx AGC Bottom Traces Layout



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5.3 APPENDIX C PARTS LISTS

5.3.1 Q0500 EVALUATION BOARD PARTS LIST

REFERENCE DESIGNATOR	QTY	MANUFACTURERS PART NUMBER	PART DESCRIPTION
	1	25-24142-1	PWB, Q0500 EVALUATION BOARD
U1	1	Q5500	IC, AMPLIFIER, RX AGC
E1 - E3	3	160-1558-02-01-00	TERMINAL, SOLDER TURRET SILVER .062" PCB
	1	MSB-2360-100-AU015-U-CTP	JUMPER, TERMINAL BI-PIN
J2	1	TSW-103-07-L-S	CONN, STRIP HEADER .025SQ 1X3 POS PCB .230 AU/SN
J1, J3, J4	3	85SMA50-0-44	CONN, SMA R/A PCB FEMALE RECEPTACLE
L3, L4	2	1008CS-332XKBC	INDUCTOR, CHIP 3.3UH 10%
L2	1	IMC-1812-100UH ± 10%	INDUCTOR, CHIP 100UH 10% Q=50 SRF=8.0MHz
T1 - T3	3	617DB-1010	TRANSFORMER, BALUN FREQ MIXER 3dB 3.5-2000MHz
R2, R6, R10	3	RM73Z2B000J	RES, CHIP THICK FILM ZERO 5% 1/8W (SIZE 1206)
R13	1	RM73B2A472J	RES, CHIP THICK FILM 4.7K 5% .1W ± 200PPM/C
R8	1	MCR10FX2100	RES, CHIP THICK FILM 210 1% .W ± 200PPM/C
R4	1	RK73H2A2490F	RES, CHIP THICK FILM 249 1% .W ± 200PPM/C
R12	1	MCR10FX2610	RES, CHIP THICK FILM 261 1% .W ± 200PPM/C
C3 - C5, C9 - C12	7	C0805C102K1RAC	CAP, CHIP CERAMIC 1000PF 10% X7R 50V
C6, C8, C13	3	C0805C103K5RAC	CAP, CHIP CERAMIC .01UF 10% X7R 50V
C2	1	THCS30E1H474ZT	CAP, CHIP CERAMIC 0.47UF +80/-20% Y5U 50V
C1	1	THCS50E1E106ZT	CAP, CHIP CERAMIC 10UF +80/-20% Y5U 25V
C7	1	T491A475M010AS	CAP, CHIP TANT 4.7UF 20% 10V

5.3.2 Q0505 EVALUATION BOARD PARTS LIST

REFERENCE DESIGNATOR	QTY	MANUFACTURERS PART NUMBER	PART DESCRIPTION
	1	25-24143-1	PWB, Q0505 EVALUATION BOARD
U1	1	Q5505	IC, AMPLIFIER, TX AGC
E1 - E3	3	160-1558-02-01-00	TERMINAL, SOLDER TURRET SILVER .062" PCB
J1 - J2	2	85SMA50-0-44	CONN, SMA R/A PCB FEMALE RECEPTACLE
L3 - L4	2	1008CS-332XKBC	INDUCTOR, CHIP 3.3UH 10%
L2	1	IMC-1812-100UH ± 10%	INDUCTOR, CHIP 100UH 10% Q=50 SRF=8.0MHz
T1, T2	2	617DB-1010	TRANSFORMER, BALUN FREQ MIXER 3dB 3.5-2000MHz
R2, R6	2	RM73Z2B000J	RES, CHIP THICK FILM ZERO 5% 1/8W (SIZE 1206)
R9	1	RM73B2A332J	RES, CHIP THICK FILM 3.3K 5% .1W ± 200PPM/C
R8	1	MCR10FX2050	RES, CHIP THICK FILM 205 1% .W ± 200PPM/C
R4	1	RK73H2A2490F	RES, CHIP THICK FILM 249 1% .W ± 200PPM/C
C3 - C5, C9 - C11	6	C0805C102K1RAC	CAP, CHIP CERAMIC 1000PF 10% X7R 50V
C12	1	C0805C103K5RAC	CAP, CHIP CERAMIC .01UF 10% X7R 50V
C2	1	THCS30E1H474ZT	CAP, CHIP CERAMIC 0.47UF +80/-20% Y5U 50V
C1	1	THCS50E1E106ZT	CAP, CHIP CERAMIC 10UF +80/-20% Y5U 25V

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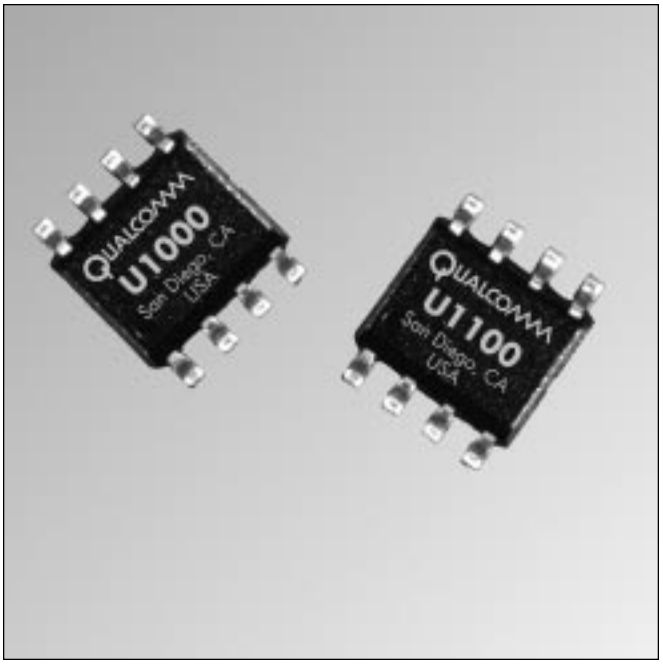
U1000

WIDEBAND UPCONVERTER

U1100

DUALBAND UPCONVERTER



U1000 / U1100 FEATURES

- Wideband RF Output Range covers Cellular and PCS Frequencies
- U1100 Includes Two Selectable RF Outputs for Dual-band PCS/Cellular FM Phone Applications
- Excellent Adjacent Channel Power Rejection Performance (High Linearity)
- Low Supply Voltage Requirements (2.7V - 3.78V)
- Low LO Power Requirement (-6 dBm min.)
- Excellent Noise Figure Performance
- All Input/Output Impedance Matching On-chip
- SOIC 8-lead Plastic Package
- Low Cost

APPLICATIONS

- CDMA/FM Cellular Systems
- CDMA US PCS Systems
- CDMA Korean PCS Systems
- Wireless Local Loop Systems
- TDMA Systems
- GSM/DCS Systems
- Spread Spectrum Cordless Phones

DESCRIPTION

The U1000 Wideband Upconverter and U1100 Dualband Upconverter are part of QUALCOMM's growing family of CDMA RFIC solutions designed specifically for the transmit section of both dual-mode CDMA/FM cellular and PCS handset applications. They are also ideal for use with other digital cellular systems. RF output performance has been specifically characterized over three primary frequency bands:

Cellular Frequency Band = 824 MHz to 849 MHz
US PCS Frequency Band = 1850 MHz to 1910 MHz
Korean PCS Frequency Band = 1750 MHz to 1780 MHz

Performance has also been characterized over the supply voltage range of 3.0 V ± 10% and 3.6 V ± 5% (2.7 V to 3.78 V). In addition, the U1100 Dualband Upconverter includes two selectable RF outputs to accomodate dual-band/dual-mode CDMA phone applications for operation between the PCS band and the Cellular FM band. Built to meet the demanding transmit specifications for CDMA phone requirements, the U1000 and U1100 achieve excellent Adjacent Channel Power Rejection (ACPR), an important indicator of linearity performance in spread spectrum systems. The differential IF input, matched to a nominal 265 Ω internally, reduces the effects of common-mode noise and allows a direct connection to differential IF AGC amplifiers or bandpass filters. The U1000 and U1100 include all Input/Output impedance matching on-chip and are packaged in an 8-lead SOIC plastic package.

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Figure 1. U1000 Wideband Upconverter Pinout Diagram

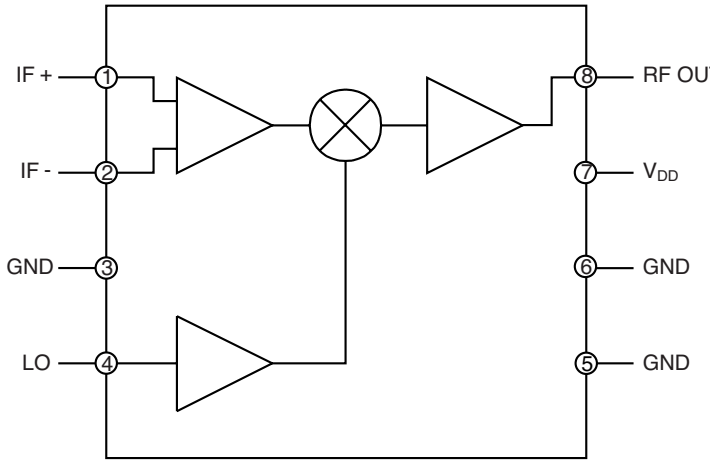

Table 1. U1000 Wideband Upconverter Pin Descriptions

SYMBOL	PINS	I / O TYPE	FUNCTION
IF +	1	IF Input	Non-inverting Differential IF Input
IF -	2	IF Input	Inverting Differential IF Input
GND	3, 5, 6	–	Ground
LO	4	LO Input	Local Oscillator Input
V_{DD}	7	Power	V_{DD} Power Supply
RF OUT	8	RF Output	RF Output

Table 2. U1000 Wideband Upconverter Operating Range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Temperature (Case)	T_C	-30	–	+80	°C	–
Operating Voltage (Relative to GND)	V_{DD}	2.7	–	3.78	V	–
RF Output Frequency Range	F_{RF}	824	–	1910	MHz	1
IF Input Frequency Range	F_{IF}	–	130.38	–	MHz	–
LO Input Frequency Range	F_{LO}	954	–	1780	MHz	1
LO Input Power Level	P_{LO}	-6	–	0	dBm	–

Note:

1. RF output performance has been characterized over three primary frequency bands:
   Cellular Frequency Band: 824 - 849 MHz
   US PCS Frequency Band: 1850 - 1910 MHz
   Korean PCS Frequency Band: 1750 - 1780 MHz

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Table 3. U1000 Wideband Upconverter Electrical Characteristics - Cellular Band (Typical Specifications given at V_{DD} = 3.0V, T = 25°C)

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Conversion Gain		–	0.6	–	dB	1, 2, 3
Gain Flatness		–	0.3	–	dB	4
Input 1 dB Compression Point (P_{1dB})		–	- 0.7	–	dBm	–
Noise Figure		–	11	–	dB	1
Adjacent Channel Power Rejection (ACPR)	Offset = ± 885 kHz	–	44	–	dBc	3, 7
	Offset = ± 1.98 MHz	–	63	–	dBc	3, 7
Isolation	IF to RF	–	49	–	dB	3
	IF to LO	–	64	–	dB	3
	RF to LO	–	43	–	dB	–
LO to RF Leakage		–	- 44	–	dBm	–
Image Rejection		–	0.26	–	dBc	–
Spurious Product Rejection	824 - 849 MHz	–	> 80	–	dBc	3, 9
	869 - 894 MHz	–	> 80	–	dBc	3, 9
	Elsewhere	–	> 40	–	dBc	3, 9
LO Harmonics of RF OUT (2LO, 3LO)		–	- 34	–	dBc	3, 9, 10
VSWR	RF Output	–	1.1 : 1	–	–	11
	IF Differential Input	–	1.5 : 1	–	–	12
	LO Input	–	1.2 : 1	–	–	11
Stability (spurious oscillations)		–	< - 78	–	dBm	13
Power Supply Current (I_{DD})		–	24	–	mA	3, 11

Table 4. U1000 Wideband Upconverter Electrical Characteristics - PCS Band (Typical Specifications given at V_{DD} = 3.0V, T = 25°C)

PARAMETER			MIN	TYP	MAX	UNITS	NOTES
Conversion Gain			–	- 0.4	–	dB	1, 2, 3
Gain Flatness			–	0.2	–	dB	5, 6
Input 1 dB Compression Point (P_{1dB})			–	- 0.2	–	dBm	–
Noise Figure			–	11.1	–	dB	1
Adjacent Channel Power Rejection (ACPR)		Offset = ± 1.25 MHz	–	47	–	dBc	3, 8
		Offset = ± 2.25 MHz	–	63	–	dBc	3, 8
Isolation		IF to RF	–	37	–	dB	3
		IF to LO	–	64	–	dB	3
		RF to LO	–	30	–	dB	–
LO to RF Leakage			–	- 30	–	dBm	–
Image Rejection			–	0.2	–	dBc	–
Spurious Product Rejection	1850 - 1910 MHz	1750 - 1780 MHz	–	> 80	–	dBc	3, 9
	1930 - 1990 MHz	1800 - 1830 MHz	–	> 80	–	dBc	3, 9
	Elsewhere US PCS	Elsewhere Korean PCS	–	> 40	–	dBc	3, 9
LO Harmonics of RF OUT (2LO, 3LO)			–	- 37	–	dBc	3, 9, 10
VSWR		RF Output	–	1.5 : 1	–	–	11
		IF Differential Input	–	1.5 : 1	–	–	12
		LO Input	–	1.5 : 1	–	–	11
Stability (spurious oscillations)			–	< - 78	–	dBm	13
Power Supply Current (I_{DD})			–	24	–	mA	3, 11

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THE UD1000-EB SINGLE-BAND CELLULAR AND THE UD1100-EB SINGLE-BAND PCS EVALUATION BOARDS

The UD1000-EB Evaluation Board is designed for evaluating the U1000 Wideband Upconverter as a cascaded transmit chain with a bandpass filter and Driver Amplifier specified over the cellular transmit frequency band. The UD1100-EB Evaluation Board is designed for evaluating the U1000 in the same type cascaded configuration specified over the PCS transmit frequency band. The bandpass filter and Driver Amplifier are included as typical building blocks of an RF Transmit Section in digital cellular phone archictecture. A typical transmitter chain topology is shown in Figure 2, along with the highlighted area representing the functionality of the UD1000-EB and UD1100-EB. Both evaluation boards allow separate testing and evaluation of the U1000 alone or included in the single-band cascaded configuration.

Figure 2. Typical Transmitter Chain Diagram

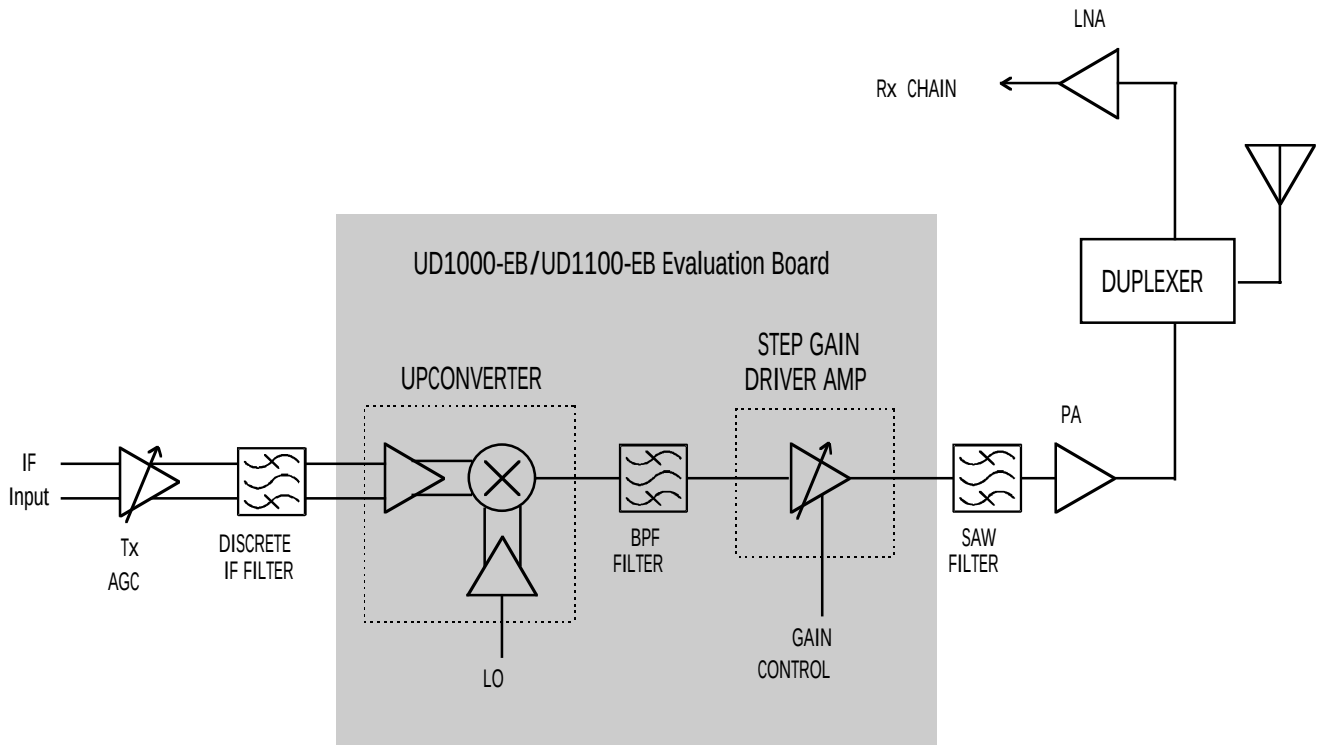

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Figure 3. U1100 Dualband Upconverter Pinout Diagram

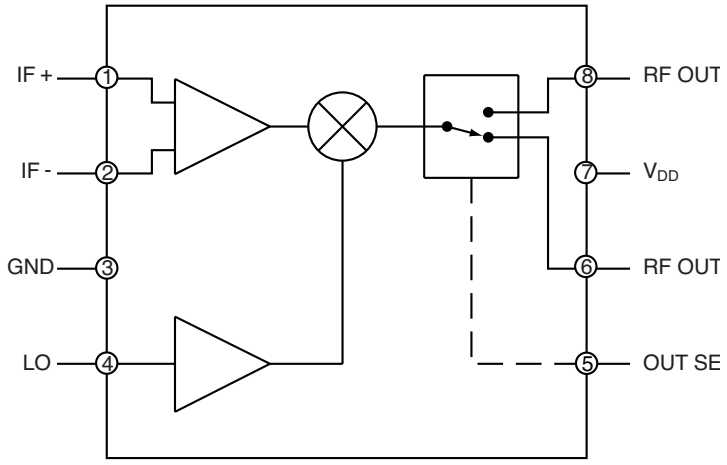

Table 5. U1100 Dualband Upconverter Pin Descriptions

SYMBOL	PINS	I / O TYPE	FUNCTION
IF +	1	IF Input	Non-inverting Differential IF Input
IF -	2	IF Input	Inverting Differential IF Input
GND	3	Ground	Ground
LO	4	LO Input	Local Oscillator Input
OUT SEL	5	Input	Output Select Switch. Low selects RF Output #2, High selects RF Output #1.
RF OUT1	6	RF Output	RF Output #1
V_{DD}	7	Power	V_{DD} Power Supply
RF OUT2	8	RF Output	RF Output #2

Table 6. U1100 Dualband Upconverter DC Electrical Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNITS
RF OUT2 Select, Low Input Voltage	V_{IL}	–	0.2	V
RF OUT1 Select, High Input Voltage	V_{IH}	2.9	–	V

Table 7. U1100 Dualband Upconverter Operating Range

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Operating Temperature (Case)	T_C	-30	–	+80	°C	–
Operating Voltage (Relative to GND)	V_{DD}	2.7	–	3.78	V	–
RF Output Frequency Range	F_{RF}	824	–	1910	MHz	1
IF Input Frequency Range	F_{IF}	–	130.38	–	MHz	–
LO Input Frequency Range	F_{LO}	954	–	1780	MHz	1
LO Input Power Level	P_{LO}	-6	–	0	dBm	–

Note:

1. RF output performance has been characterized over three primary frequency bands:
   Cellular Frequency Band: 824 - 849 MHz
   US PCS Frequency Band: 1850 - 1910 MHz
   Korean PCS Frequency Band: 1750 - 1780 MHz

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Table 8. U1100 Dualband Upconverter Electrical Characteristics - Cellular Band (Typical Specifications given at V_{DD} = 3.0V, T = 25°C)

PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Conversion Gain		–	- 0.6	–	dB	1, 2, 3
Gain Flatness		–	0.3	–	dB	4
Inactive Path Conversion Gain		–	- 34	–	dB	–
Input 1 dB Compression Point (P_{1dB})		–	- 2	–	dBm	–
Noise Figure		–	12	–	dB	1
Adjacent Channel Power Rejection (ACPR)	Offset = ± 885 kHz	–	43	–	dBc	3, 7
	Offset = ± 1.98 MHz	–	64	–	dBc	3, 7
Isolation	IF to RF	–	40	–	dB	3
	IF to LO	–	69	–	dB	3
	RF to LO	–	29	–	dB	–
LO to RF Leakage		–	- 30	–	dBm	–
Image Rejection		–	0.24	–	dBc	–
Spurious Product Rejection	824 - 849 MHz	–	> 80	–	dBc	3, 9
	869 - 894 MHz	–	> 80	–	dBc	3, 9
	Elsewhere	–	> 40	–	dBc	3, 9
LO Harmonics of RF OUT (2LO, 3LO)		–	- 37	–	dBc	3, 9, 10
VSWR	RF OUT1, RF OUT2	–	1.1 : 1	–	–	11
	IF Differential Input	–	1.3 : 1	–	–	12
	LO Input	–	1.25 : 1	–	–	11
Stability (spurious oscillations)		–	< - 70	–	dBm	13
Power Supply Current (I_{DD})		–	23	–	mA	3, 11

Table 9. U1100 Dualband Upconverter Electrical Characteristics - PCS Band (Typical Specifications given at V_{DD} = 3.0V, T = 25°C)

PARAMETER			MIN	TYP	MAX	UNITS	NOTES
Conversion Gain			–	- 1.4	–	dB	1, 2, 3
Gain Flatness			–	0.1	–	dB	5, 6
Inactive Path Conversion Gain			–	- 23	–	dB	–
Input 1 dB Compression Point (P_{1dB})			–	- 1.5	–	dBm	–
Noise Figure			–	12	–	dB	1
Adjacent Channel Power Rejection (ACPR)		Offset = ± 1.25 MHz	–	46	–	dBc	3, 8
		Offset = ± 2.25 MHz	–	65	–	dBc	3, 8
Isolation		IF to RF	–	34	–	dB	3
		IF to LO	–	63	–	dB	3
		RF to LO	–	20	–	dB	–
LO to RF Leakage			–	- 26	–	dBm	–
Image Rejection			–	- 0.1	–	dBc	–
Spurious Product Rejection	1850 - 1910 MHz	1750 - 1780 MHz	–	> 80	–	dBc	3, 9
	1930 - 1990 MHz	1800 - 1830 MHz	–	> 80	–	dBc	3, 9
	Elsewhere US PCS	Elsewhere Korean PCS	–	> 40	–	dBc	3, 9
LO Harmonics of RF OUT (2LO, 3LO)			–	- 30	–	dBc	3, 9, 10
VSWR		RF OUT1, RF OUT2	–	1.6 : 1	–	–	11
		IF Differential Input	–	1.3 : 1	–	–	12
		LO Input	–	1.6 : 1	–	–	11
Stability (spurious oscillations)			–	< - 70	–	dBm	13
Power Supply Current (I_{DD})			–	24	–	mA	3, 11

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Notes Pertaining to Tables 3, 4, 8 and 9

1. Z_S = 265 Ω, Z_L = 50 Ω.
2. Gain is specified as power gain.
3. IF input power, P_{IF} = - 10 dBm.
4. RF output frequency = 824 MHz to 849 MHz.
5. RF output frequency = 1850 MHz to 1910 MHz.
6. RF output frequency = 1750 MHz to 1780 MHz.
7. Adjacent Channel Power Rejection (ACPR) Test, Cellular Band. (See Figure 4)
   A. Measure the average power in the 1.23 MHz wide CDMA signal, and then determine the average power in a 30 kHz bandwidth, $P_{C\ 30\ kHz}$. For example, if the power in the CDMA signal is 0 dBm, $P_{C\ 30\ kHz}$ = - 16.13 dBm.
   B. Measure power at ± 885 kHz offset, $P_{\pm\ 885\ kHz}$ in a 30 kHz bandwidth.
   C. Measure power at ± 1.98 MHz offset, $P_{\pm 1.98\ MHz}$ in a 30 kHz bandwidth.
   D. $ACPR_{\pm\ 885\ kHz} = P_{C\ 30\ kHz} - P_{\pm\ 885\ kHz}$ dBc.
      $ACPR_{\pm\ 1.98\ MHz} = P_{C\ 30\ kHz} - P_{\pm 1.98\ MHz}$ dBc.
8. Adjacent Channel Power Rejection (ACPR) Test, PCS Band. (See Figure 5)
   A. Measure the average power in the 1.23 MHz wide CDMA signal, and then determine the average power in a 30 kHz bandwidth, $P_{C\ 30\ kHz}$. For example, if the power in the CDMA signal is 0 dBm, $P_{C\ 30\ kHz}$ = - 16.13 dBm.
   B. Measure power at ± 1.25 MHz offset, $P_{\pm\ 1.25\ MHz}$ in a 30 kHz bandwidth.
   C. Measure power at ± 2.25 MHz offset, $P_{\pm 2.25\ MHz}$ in a 30 kHz bandwidth.
   D. $ACPR_{\pm\ 1.25\ MHz} = P_{C\ 30\ kHz} - P_{\pm\ 1.25\ MHz}$ dBc.
      $ACPR_{\pm\ 2.25\ MHz} = P_{C\ 30\ kHz} - P_{\pm 2.25\ MHz}$ dBc.
9. Reference to RF OUT.
10. LO input power, P_{LO} = 0 dBm.
11. 50 Ω nominal, no external matching.
12. 265 Ω differential nominal.
13. Source and load VSWR 10:1, all phases.

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Figure 4. Adjacent Channel Power Rejection (ACPR) Test of the U1000 and U1100 in Cellular Band

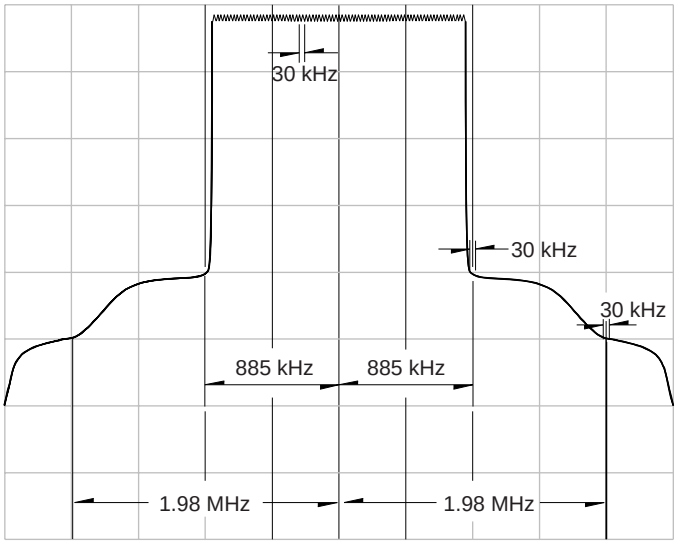
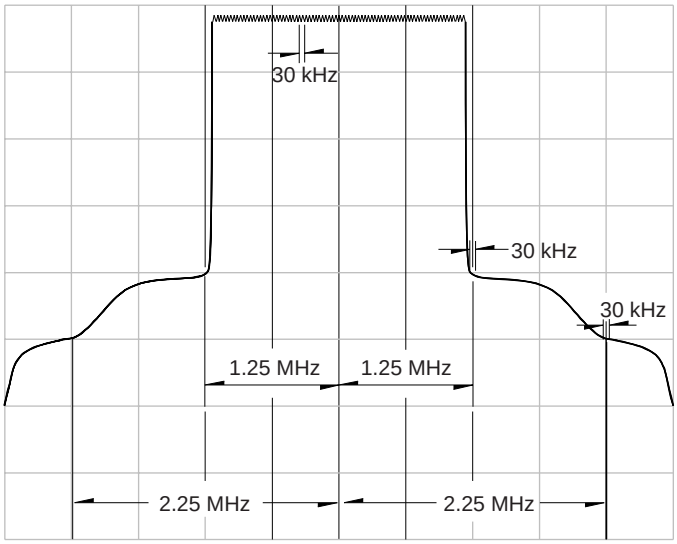


Figure 5. Adjacent Channel Power Rejection (ACPR) Test of the U1000 and U1100 in PCS Band



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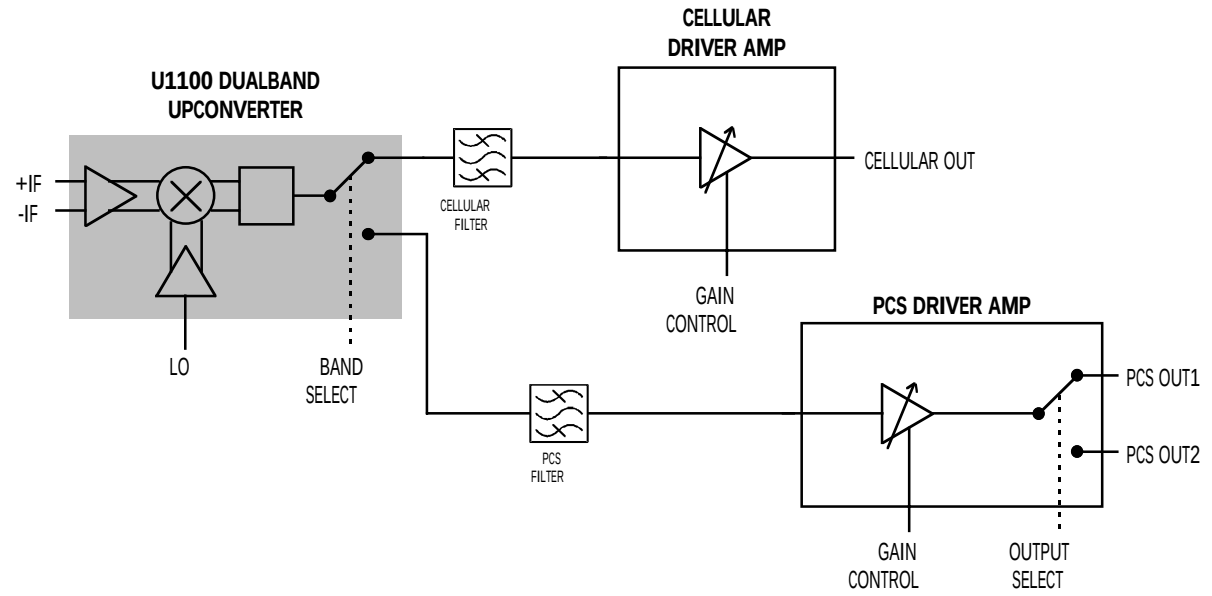
THE U1100-EB DUALBAND UPCONVERTER EVALUATION BOARD

The U1100-EB Evaluation Board is an easy-to-test printed circuit card assembly designed specifically to demonstrate the performance of the QUALCOMM U1100 Dualband Upconverter. A typical dual-band transmit section including bandpass filters and Driver Amplifiers for phone applications that operate between the PCS band and the Cellular FM band is shown in Figure 6. The highlighted area represents the functionality of the U1100-EB. RF output selection of the U1100 is simply changed by moving an on-board jumper. All inputs and outputs to the U1100-EB are single-ended and matched to 50 Ω.

Figure 6. Typical Dual-band Transmit Section



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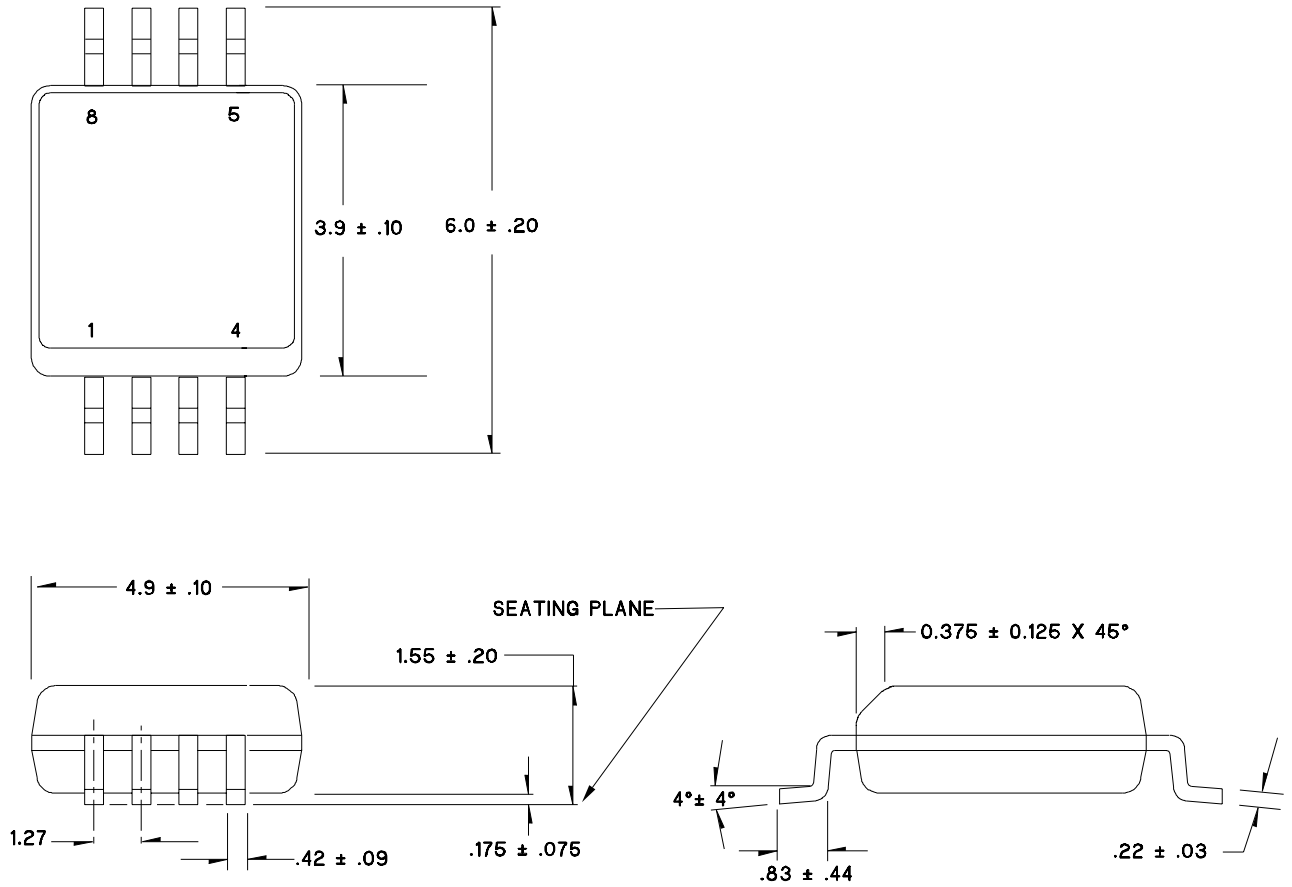
SOIC PACKAGING

Figure 7. U1000 and U1100 SOIC 8-Lead Package Outline



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UD1000-EB

WIDEBAND UPCONVERTER / CELLULAR DRIVER AMPLIFIER EVALUATION BOARD

USER'S GUIDE

CONTENTS

1.0 INTRODUCTION

The UD1000-EB was designed specifically to demonstrate the performance of QUALCOMM's U1000 Wideband Upconverter individually or in a cascaded RF chain including a cellular ceramic bandpass filter and a Cellular Driver Amplifier on the output of the U1000.

A block diagram of the UD1000-EB can be found in Figure 1. Minimal equipment is required to demonstrate the functionality of the evaluation board and to verify the high degree of performance of the U1000. Gain control of the Cellular Driver Amplifier is simply changed by moving an on-board jumper. All inputs and outputs to the UD1000-EB are single ended and matched to 50 Ω.

This User's Guide provides all the information required to operate the UD1000-EB Evaluation Board. Appendices are also provided which contains the UD1000-EB schematic, layout and a complete parts list. It is also recommended that designers read the "U1000 Wideband Upconverter/U1100 Dualband Upconverter Preliminary Data Sheet".

The UD1000-EB is meant to be a demonstration circuit and evaluation tool. QUALCOMM does not make any warranty as to the UD1000-EB suitability for a specific applications without further design modifications. However, we believe you will find the UD1000-EB a useful tool in evaluating and understanding QUALCOMM's U1000.

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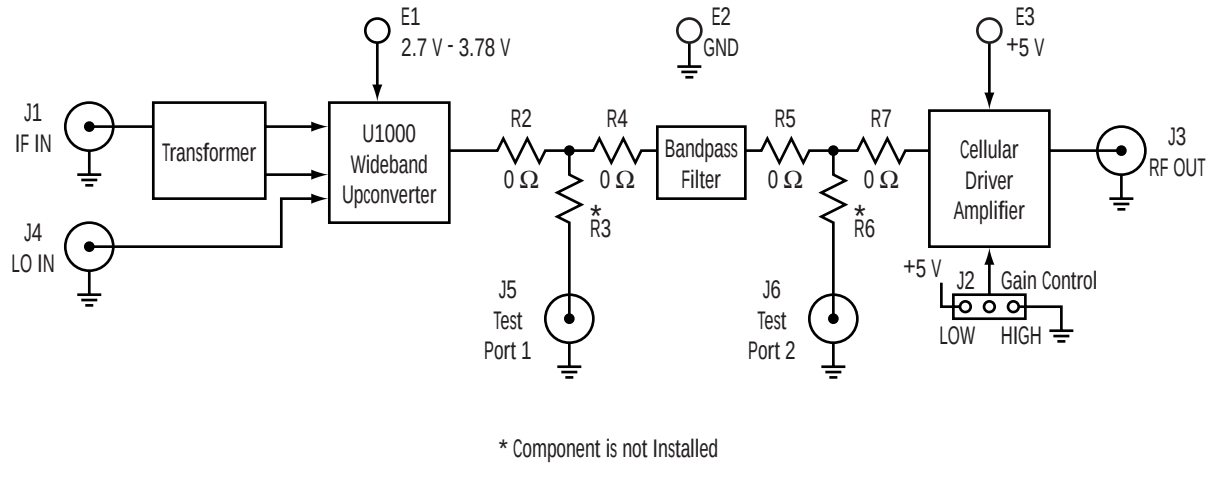
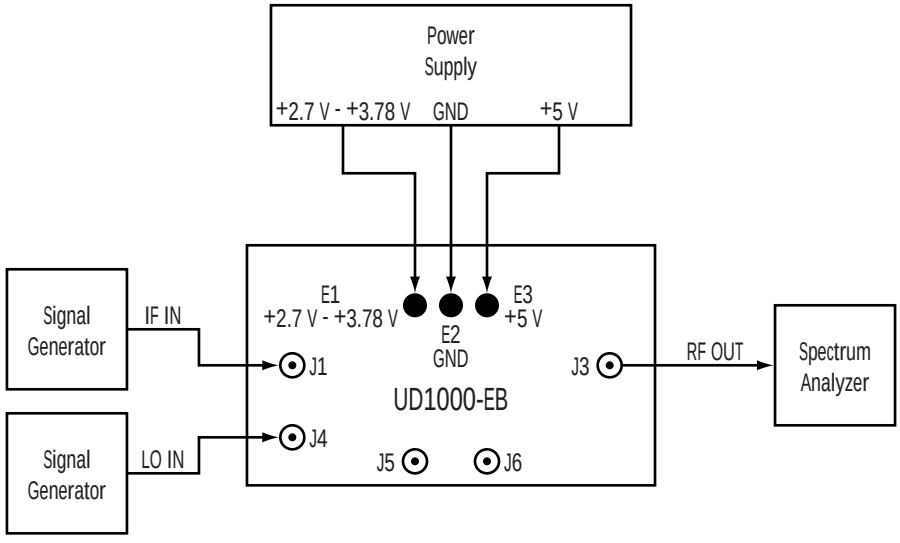
Figure 1. UD1000-EB Block Diagram



2.0 GETTING STARTED

Operation of the UD1000-EB is very simple. The board requires an LO and IF input via signal generators or other source to drive the U1000, while gain of the Cellular Driver Amplifier is controlled via a simple jumper. The output of the UD1000-EB is then measured by a spectrum analyzer. Test signals enter and exit the board via coax cables with SMA connectors. The UD1000-EB does require two different voltages be applied to the board. The U1000 requires 2.7 V to 3.78 V connected to E1 while the Cellular Driver Amplifier requires 5 volts applied to E3. The U1000 and Cellular Driver Amplifier share a common ground on the evaluation board. A functional setup block diagram of the UD1000-EB can be found in Figure 2.

Figure 2. UD1000-EB Board Setup



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2.1 REQUIRED EQUIPMENT

The UD1000-EB comes fully configured for operation with minimal assembly. The following list of standard test equipment is provided as a baseline. If specific equipment is not available, equipment with equivalent functionality may be substituted.

Spectrum Analyzer	HP8563E
Signal Generators (2)	HP8648C
Power Supply	Leader LPS-152
Coax Cables	
Power cables	

3.0 EVALUATION BOARD OPERATION

Figure 1 shows the UD1000-EB block diagram. The following paragraphs describe the function and operation of each of the circuit elements shown in the block diagram.

3.1 INPUTS

3.1.1 POWER SUPPLY REQUIREMENTS

The UD1000-EB requires two voltages for proper operation. The U1000 requires 2.7 V to 3.78 V at 35 mA connected to E1 while the Cellular Driver Amplifier requires 5 volts at 60 mA applied to E3. The U1000 and Cellular Driver Amplifier share a common ground, E2.

3.1.2 IF INPUT (J1)

The IF input to the U1000 is applied on connector J1, which is closely matched to 50 Ω. To minimize power loss to the U1000, a 4:1 impedance transformer was placed in between the 50 Ω IF input and the U1000. The balun transformer purpose is two fold. First, it transforms the 50 Ω input impedance to 200 Ω but also turns the single ended input into a differential input which is routed to the U1000. The nominal frequency input to the IF port is 130.38 MHz with a maximum power level of -5 dBm. There will be some IF power loss due to the impedance mismatch between the transformer and the U1000 IF input. The typical conversion loss of the U1000 is 0 dB.

3.1.3 LO INPUT (J4)

The LO input to the U1000 is applied on connector J4. This connector is matched to 50 Ω. The LO input is directly routed to the U1000 and will suffer minimal power loss. The nominal frequency input to the LO port is 954 to 979 MHz with a power level between -6 and 0 dBm.

3.1.4 CELLULAR DRIVER AMPLIFIER GAIN CONTROL (J2)

The Cellular Driver Amplifier Gain Mode is controlled through jumper J2. When pins 1 and 2 of jumper J2 are connected, the Cellular Driver Amplifier gain control pin is pulled to +5 volts. This will cause the Cellular Driver Amplifier to enter Low Gain Mode. When the Cellular Driver Amplifier enters Low Gain Mode, the nominal gain of the device is -2.2 dB. When pins 2 and 3 of jumper J2 are connected, the Cellular Driver Amplifier gain control pin is pulled to 0 volts. This will cause the Cellular Driver Amplifier to enter High Gain Mode. When the Cellular Driver Amplifier enters High Gain Mode, the nominal gain of the device is +23.5 dB.

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3.2 TEST PORTS

3.2.1 TEST PORT 1 (J5)

The functionality of Test Port 1 is two fold. First, it can be configured as the U1000 output or as a input to the ceramic bandpass filter. Refer to Figure 1. In order to configure Test Port 1 as the output of the U1000, 0 Ω resistors should be placed in R2 and R3, and resistor R4 should be removed. The resistor pads are configured to accept 0603 size resistors. In doing this, the RF output of the U1000 will not be routed to the ceramic filter or to the Cellular Driver Amplifier; therefore the RF Output of J3 will be invalid.

Secondly, Test Port 1 can be configured as a ceramic filter input. In order to configure the port as the ceramic filter input, insert 0 Ω resistors in R3 and R4, remove resistor R2. The resistor pads are configured to accept 0603 size resistors. In this configuration, a RF signal can be injected directly into to the ceramic bandpass filter without having to go through the U1000.

3.2.2 TEST PORT 2 (J6)

The functionality of Test Port 2 is also two fold. The port can be configured as the ceramic bandpass filter output or as an input to the Cellular Driver Amplifier. Refer to Figure 1. In order to configure Test Port 2 as the output of the ceramic filter, insert 0 Ω resistors in R5 and R6, and remove resistor R7. The resistor pads are configured to accept 0603 size resistors. In this configuration, the RF output of the ceramic filter can be examined without going through the Cellular Driver Amplifier.

Secondly, Test Port 2 can be configured as the input to the Cellular Driver Amplifier. In order to configure the port as the Cellular Driver Amplifier input, insert 0 Ω resistors in R6 and R7, and remove resistor R5. The resistor pads are configured to accept 0603 size resistors. In this configuration, the RF signal is directly input to the Cellular Driver Amplifier. The nominal frequency input of the Cellular Driver Amplifier is 824 to 849 MHz.

3.3 RF OUTPUT (J3)

The output of the Cellular Driver Amplifier is routed directly to connector J3. The output is matched to 50 Ω, so impedance matching to a spectrum analyzer or power meter is not required. The output power of the Cellular Driver Amplifier will be dependent upon the input power to the device and the gain mode setting. The typical output P1dB of the Cellular Driver Amplifier is +15 dBm.

4.0 EVALUATION CONSIDERATIONS

In order to fully understand the performance of the U1000 and the Cellular Driver Amplifier when the devices are cascaded as a transmit chain, the characteristics of the ceramic bandpass filter must be known. Table 1 outlines the specifications of the ceramic bandpass filter on the UD1000-EB.

Table 1. Ceramic Bandpass Filter Characteristics

Nominal Impedance	50 Ω
Center Frequency (f_0)	836.5 MHz
Pass Band Range	$f_0 \pm 12.5$ MHz
Insertion Loss	2.8 dB MAX
Attenuation	20 dB MIN at $f_0 \pm 77.5$ MHz
Ripple in Bandwidth	1.0 dB MAX

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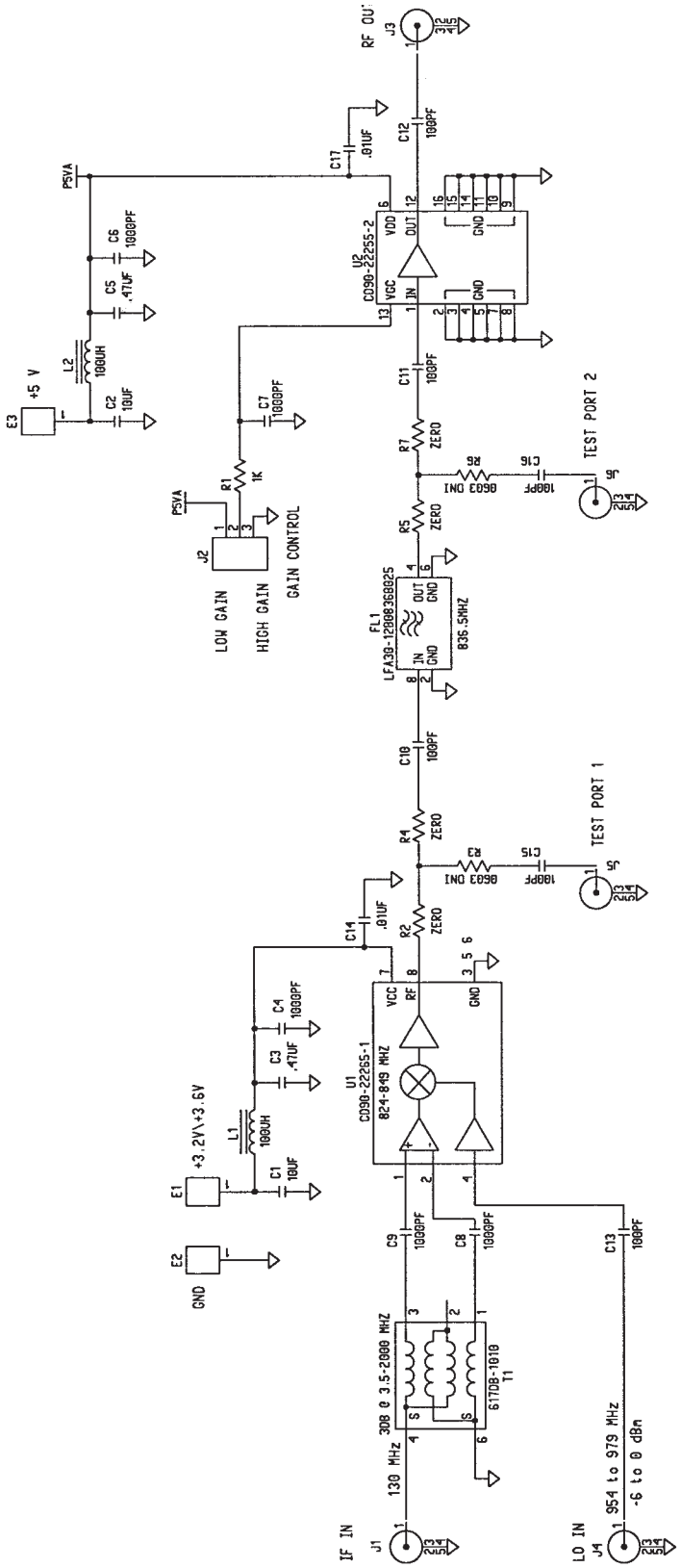
5.0 APPENDIX

5.1 APPENDIX A UD1000-EB SCHEMATICS



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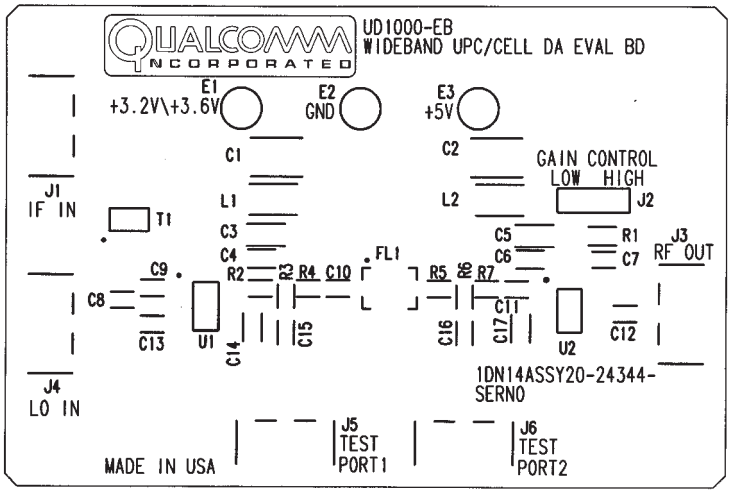
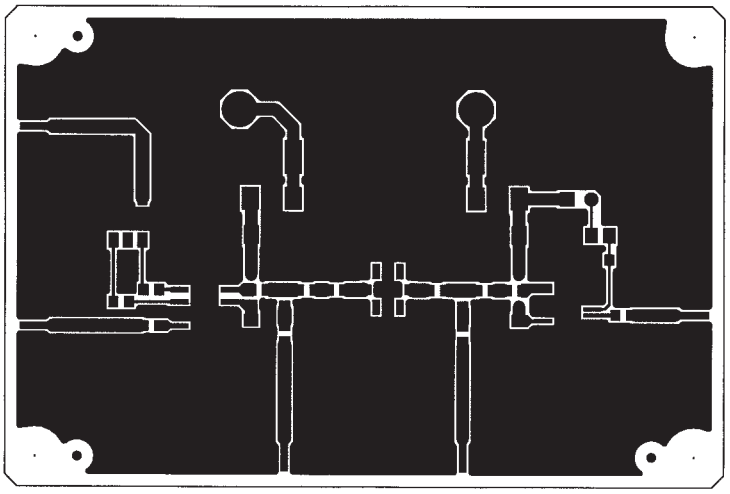
5.2 APPENDIX B UD1000-EB LAYOUT DRAWINGS

UD1000-EB Top Silk Layout



UD1000-EB Top Traces Layout



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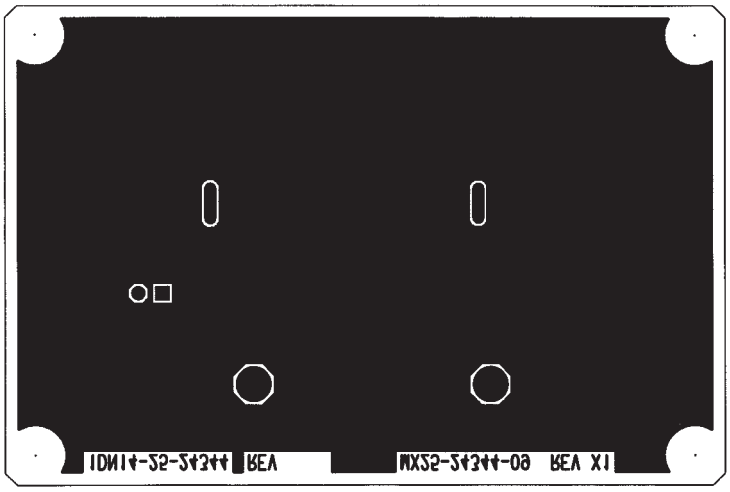

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5.3 APPENDIX C UD1000-EB PARTS LIST

REFERENCE DESIGNATOR	QTY	MANUFACTURERS PART NUMBER	PART DESCRIPTION
	1	25-24344-1	PWB,UD1000-EB, WIDEBAND UPC/CELL DA
R1	1	MCR10F1001	RES, CHIP THICK FILM 1.0K 1% .1W
R2, R4, R5, R7	4	MCR03JZHMJW000E	RES, CHIP THICK FILM ZERO 5% .063W
C4, C6	2	C0805C102K1RAC	CAP, CHIP CERAMIC 1000PF 10% X7R
C14, C17	2	C0805C103K5RAC	CAP, CHIP CERAMIC .01UF 10% X7R
C13, C10, C11, C15, C16	6	C0603C101J5GAC	CAP, CHIP CERAMIC 100PF 5% COG/NP0
C8, C9	3	C0603C102K5RAC	CAP, CHIP CERAMIC 1000PF 10% X7R
C3, C5	2	THCS30E1H474ZT	CAP, CHIP CERAMIC 0.47UF +80/-20%
C1, C2	2	THCS50E1E106ZT	CAP, CHIP CERAMIC 10UF +80/-20%
L1, L2	2	IMC-1812 100UH 10%	INDUCTOR, CHIP 100UH 10% Q=50
T1	1	617DB-1010	TRANSFORMER, BALUN 4:1 IMPEDANCE
FL1	1	LFA30-12B0836B025	FILTER, BANDPASS CERAMIC
E1, E2, E3	3	160-1558-02-01-00	TERMINAL, SOLDER TURRET SILVER .062
J2	1	TSW-103-07-L-S	CONN, STRIP HEADER .025SQ 1X3 POS
J1, J3 - J6	5	142-0701-881	CONN, SMA JACK RCPT END LAUNCH
U2	1	CD-90-22285-3	IC, DRIVER AMP, HIGH FREQUENCY, STEP
U1	1	U1000	WIDEBAND UPCONVERTER IC

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UD1100-EB

WIDEBAND UPCONVERTER / PCS DRIVER AMPLIFIER EVALUATION BOARD

USER'S GUIDE

CONTENTS

1.0 INTRODUCTION

The UD1100-EB was designed specifically to demonstrate the performance of QUALCOMM's U1000 Wideband Upconverter individually or in a cascaded RF transmit chain including a PCS SAW bandpass filter and a PCS Driver Amplifier on the output of the U1000. A block diagram of the UD1100-EB can be found in Figure 1. Minimal equipment is required to demonstrate the functionality of the evaluation board and to verify the high degree of performance of the U1100. Gain control of the PCS Driver Amplifier and RF Output Select is simply changed by moving on-board jumpers. All inputs and outputs to the UD1100-EB are single ended and matched to 50 Ω.

This User's Guide provides all the information required to operate the UD1100-EB Evaluation Board. Appendices are also provided which contains the UD1100-EB schematic, layout and a complete parts list. It is also recommended that designers read the "U1000 Wideband Upconverter/U1100 Dualband Upconverter Preliminary Data Sheet".

The UD1100-EB is meant to be a demonstration circuit and evaluation tool. QUALCOMM does not make any warranty as to the UD1100-EB suitability for a specific applications without further design modifications. However, we believe you will find the UD1100-EB a useful tool in evaluating and understanding QUALCOMM's U1000.

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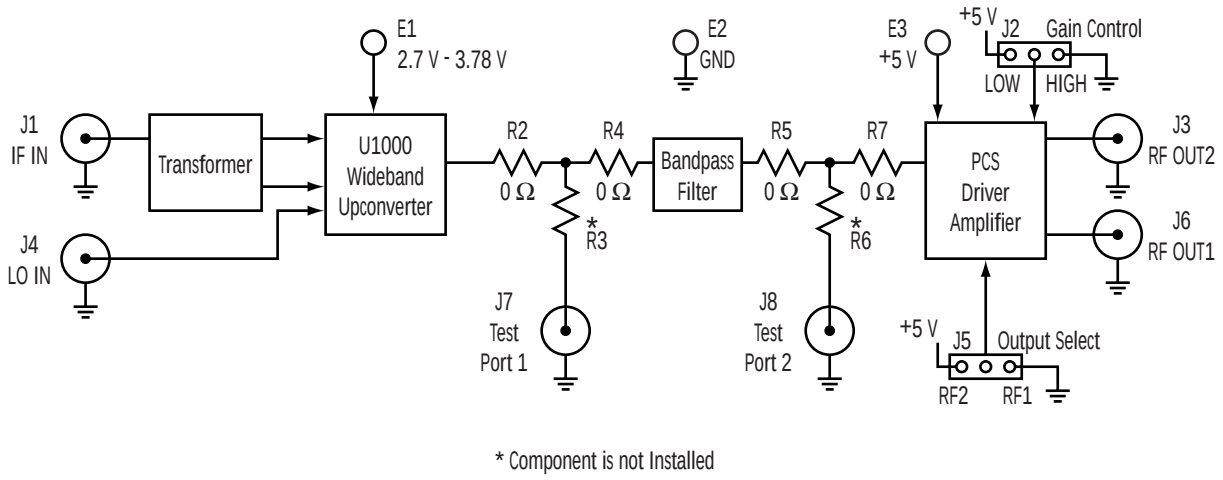
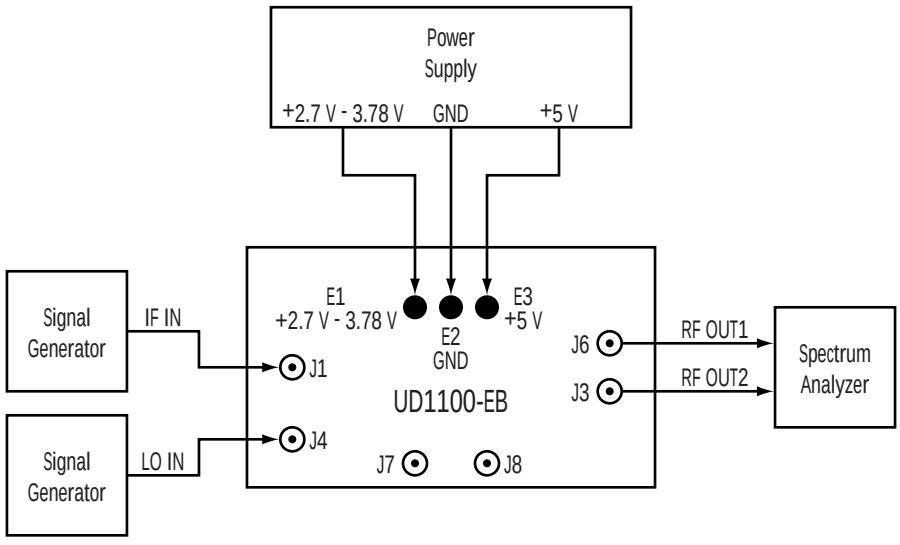
Figure 1. UD1100-EB Block Diagram



2.0 GETTING STARTED

Operation of the UD1100-EB is very simple. The board requires an LO and IF input via signal generators or other source to drive the U1000 while gain and RF output select of the PCS Driver Amplifier is controlled via simple jumpers. The output of the UD1100-EB is then measured by a spectrum analyzer. Test signals enter and exit the board via coax cables with SMA connectors. The UD1100-EB does require two different voltages be applied to the board. The U1000 requires 2.7 V to 3.78 V connected to E1 while the PCS Driver Amplifier requires 5 volts applied to E3. The U1000 and PCS Driver Amplifier share a common ground on the evaluation board. A functional setup block diagram of the UD1100-EB can be found in Figure 2.

Figure 2. UD1100-EB Board Setup



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2.1 REQUIRED EQUIPMENT

The UD1100-EB comes fully configured for operation with minimal assembly. The following list of standard test equipment is provided as a baseline. If specific equipment is not available, equipment with equivalent functionality may be substituted.

Spectrum Analyzer	HP8563E
Signal Generators (2)	HP8648C
Power Supply	Leader LPS-152
Coax Cables	
Power cables	

3.0 EVALUATION BOARD OPERATION

Figure 1 shows the UD1100-EB block diagram. The following paragraphs describe the function and operation of each of the circuit elements shown in the block diagram.

3.1 INPUTS

3.1.1 POWER SUPPLY REQUIREMENTS

The UD1100-EB requires two voltages for proper operation. The U1000 requires either 2.7 V to 3.78 V at 35 mA connected to E1, while the PCS Driver Amplifier requires 5 volts at 60 mA applied to E3. The U1000 and PCS Driver Amplifier share a common ground, E2.

3.1.2 IF INPUT (J1)

The IF input to the U1000 is applied on connector J1, which is closely matched to 50 Ω. To minimize power loss to the U1000, a 4:1 impedance transformer was placed in between the 50 Ω IF Input and the U1000. The balun transformer purpose is two fold. First, it transforms the 50 Ω input impedance to 200 Ω but also turns the single ended input into a differential input which is then routed to the U1000. The nominal frequency input to the IF port is 130.38 MHz with a maximum power level of -5 dBm. There will be some IF power loss due to the impedance mismatch between the transformer and the U1000 IF input. The typical conversion loss of the U1000 is 0 dB.

3.1.3 LO INPUT (J4)

The LO input to the U1000 is applied on connector J4. This connector is matched to 50 Ω. The LO input is directly routed to the U1000 and will suffer minimal power loss. The nominal frequency input to the LO port is 1720 to 1780 MHz with a power level between -6 and 0 dBm.

3.1.4 PCS DRIVER AMPLIFIER GAIN CONTROL (J2)

The PCS Driver Amplifier Gain Mode is controlled through jumper J2. When pins 1 and 2 of jumper J2 are connected, the PCS Driver Amplifier gain control pin is pulled to +5 volts. This will cause the PCS Driver Amplifier to enter Low Gain Mode. When the PCS Driver Amplifier enters Low Gain Mode, the nominal gain of the device is +8 dB. When pins 2 and 3 of jumper J2 are connected, the PCS Driver Amplifier gain control pin is pulled to 0 volts. This will cause the PCS Driver Amplifier to enter High Gain Mode. When the PCS Driver Amplifier enters High Gain Mode, the nominal gain of the device is +28 dB.

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3.1.5 PCS DRIVER AMPLIFIER OUTPUT SELECT (J5)

The PCS Driver Amplifier has two RF outputs which are selectable by jumper J5. When pins 2 and 3 of jumper J5 are connected, the PCS Driver Amplifier Output Select pin is pulled to ground. This causes the RF output of the PCS Driver Amplifier to be routed to the RF1 Output J6. When pins 1 and 2 of jumper J5 are connected. the PCS Driver Amplifier Output Select pin is pulled high. This causes the RF output of the PCS Driver Amplifier to be routed to the RF2 Output, J3.

3.2 TEST PORTS

3.2.1 TEST PORT 1 (J5)

The functionality of Test Port 1 is two fold. First, it can be configured as the U1000 output or as a input to the SAW bandpass filter. Refer to Figure 1. In order to configure Test Port 1 as the output of the U1000, 0 Ω resistors should be placed in R2 and R3, and resistor R4 should be removed. The resistor pads are configured to accept 0603 size resistors In doing this, the RF output of the U1000 will not be routed to the saw filter or to the PCS Driver Amplifier, therefore the RF Outputs of J3 and J6 will be invalid.

Secondly, Test Port 1 can be configured as a SAW filter input. In order to configure the port as the saw filter input, insert 0 Ω resistors in R3 and R4, and remove resistor R2. The resistor pads are configured to accept 0603 size resistors. In this configuration, a RF signal can be injected directly into to the saw bandpass filter without having to go through the U1000.

3.2.2 TEST PORT 2 (J6)

The functionality of Test Port 2 is also two fold. The port can be configured as the saw bandpass filter output or as an input to the PCS Driver Amplifier. Refer to Figure 1. In order to configure Test Port 2 as the output of the saw filter, insert 0 Ω resistors in R5 and R6, and remove resistor R7. The resistor pads are configured to accept 0603 size resistors. In this configuration, the RF output of the ceramic filter can be examined without going through the PCS Driver Amplifier.

Secondly, Test Port 2 can be configured as the input to the PCS Driver Amplifier. In order to configure the port as the PCS Driver Amplifier input, insert 0 Ω resistors in R6 and R7, and remove resistor R5. The resistor pads are configured to accept 0603 size resistors. In this configuration, the RF signal is directly input to the PCS Driver Amplifier. The nominal frequency input of the PCS Driver Amplifier is 1850 to 1910 MHz.

3.3 RF OUTPUT (J3)

The output of the PCS Driver Amplifier is routed directly to connector J3 or J6 depending on the Output Select jumper. The output is matched to 50 Ω, so impedance matching to a spectrum analyzer or power meter is not required. The output power of the PCS Driver Amplifier will be dependent upon the input power to the device and the gain mode setting. The typical output P1dB of the PCS Driver Amplifier is +15 dBm.

4.0 EVALUATION CONSIDERATION

In order to fully understand the performance of the U1000 and Cellular Driver Amplifier when the devices are cascaded as a transmit chain, the characteristics of the PCS SAW bandpass filter must be known. Table 1 outlines the specifications of the PCS SAW bandpass filter on the UD1100-EB.

Table 1. PCS SAW Bandpass Filter Characteristics

Nominal Impedance	50 Ω
Center Frequency (f_0)	1880 MHz
Pass Band Range	$f_0 \pm 30$ MHz
Insertion Loss	2.0 dB MAX
Attenuation	20 dB MIN at $f_0 \pm 100$ MHz

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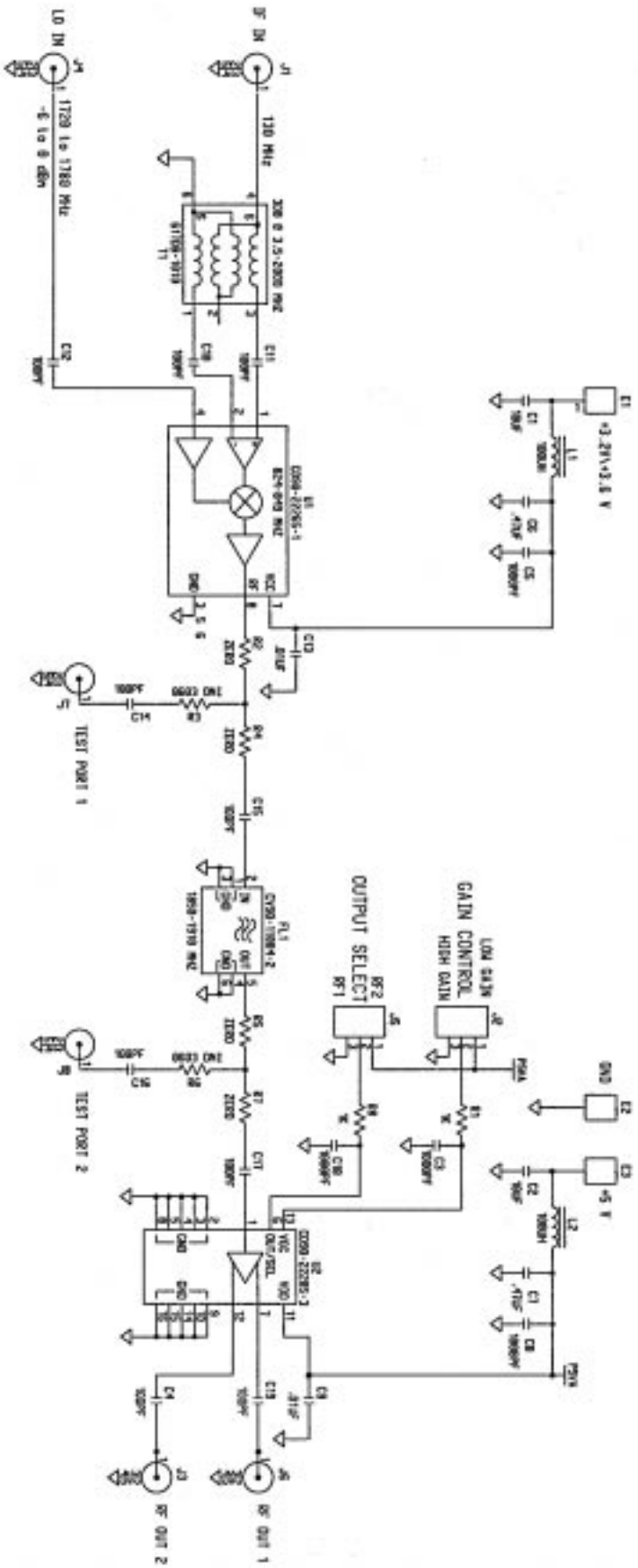
5.0 APPENDIX

5.1 APPENDIX A UD1100-EB SCHEMATICS



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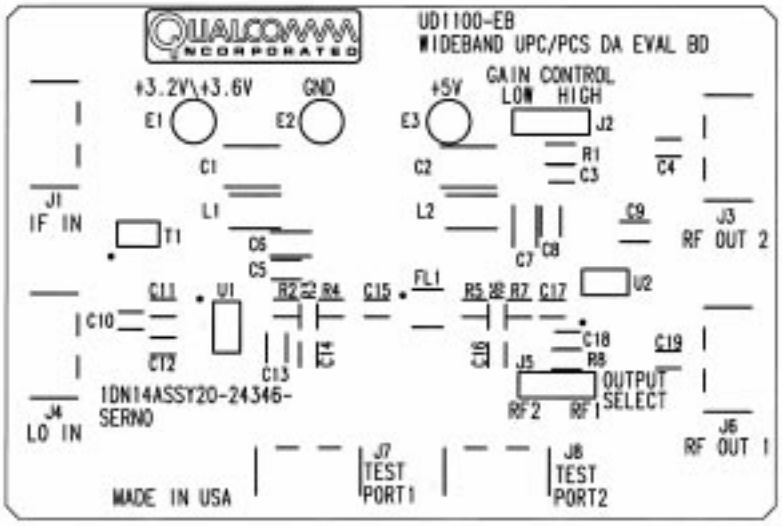
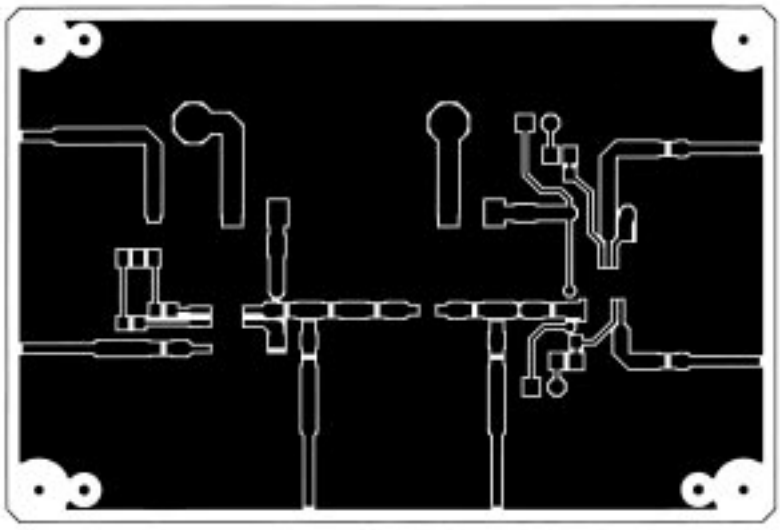
5.2 APPENDIX B UD1100-EB LAYOUT DRAWINGS

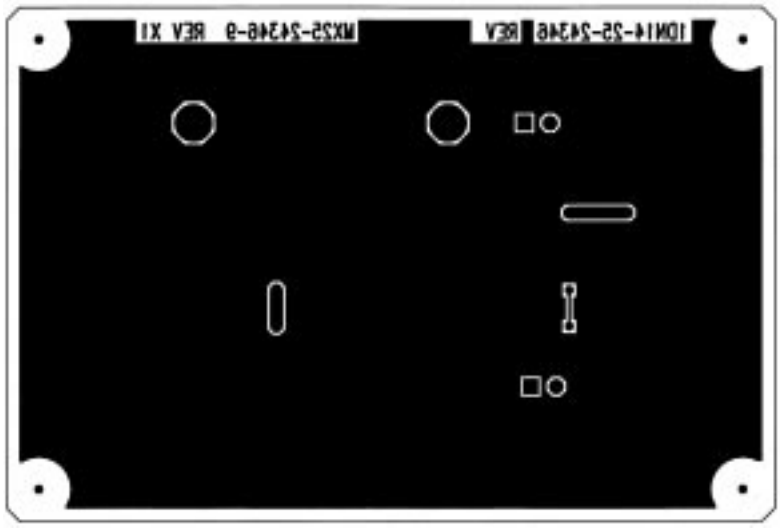
UD1100-EB Top Silk Layout



UD1100-EB Top Traces Layout



UD1100-EB Bottom Traces Layout



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5.3 APPENDIX C UD1100-EB PARTS LIST

REFERENCE DESIGNATOR	QTY	MANUFACTURERS PART NUMBER	PART DESCRIPTION
	1	24-24346-1	PWB,UD1100-EB, WIDEBAND UPC/PCS DA
R1, R8	2	MCR10F1001	RES, CHIP THICK FILM 1.0K 1% .1W
R2, R4, R5, R7	4	MCR03JZHMJW000E	RES, CHIP THICK FILM ZERO 5% .063W
C5, C8	2	C0805C102K1RAC	CAP, CHIP CERAMIC 1000PF 10% X7R
C9, C13	2	C0805C103K5RAC	CAP, CHIP CERAMIC .01UF 10% X7R
C4, C10-C12, C14-C17, C19	9	C0603C101J5GAC	CAP, CHIP CERAMIC 100PF 5% COG/NP0
C6, C7	2	THCS30E1H474ZT	CAP, CHIP CERAMIC 0.47UF +80/-20%
C1, C2	2	THCS50E1E106ZT	CAP, CHIP CERAMIC 10UF +80/-20%
L1, L2	2	IMC-1812 100UH 10%	INDUCTOR, CHIP 100UH 10% Q=50
T1	1	617DB-1010	TRANSFORMER, BALUN FREQ MIXER
E1-E3	3	160-1558-02-01-00	TERMINAL, SOLDER TURRET SILVER .062
J2, J5	2	TSW-103-07-L-S	CONN, STRIP HEADER .025SQ 1X3 POS
J1, J3, J4, J6-J8	6	142-0701-881	CONN.SMA JACK RCPT END LAUNCH
U1	1	U1000	WIDEBAND UPCONVERTER
U2	1	CD-90-22285-3	PCS DRIVER AMPLIFIER
FL1	1	CV90-11884-2	FILTER, PCS TX, SAW 1850-1910 MHZ

U1100-EB

DUALBAND UPCONVERTER EVALUATION BOARD

USER'S GUIDE

CONTENTS

1.0 INTRODUCTION

The U1100-EB Dualband Upconverter (UPC) Evaluation Board was designed specifically to demonstrate the performance of QUALCOMM's U1100 Dualband UPC. A block diagram of the U1100-EB can be found in Figure 1. Minimal equipment is required to demonstrate the functionality of the evaluation board and to verify the high degree of performance of the U1100. The RF outputs of the U1100-EB is selected by simply moving an on-board jumper. All inputs and outputs to the U1100-EB are single ended and matched to 50 Ω.

This User's Guide provides all the information required to operate the U1100-EB Evaluation Board. Appendices are also provided which contains the U1100-EB schematic, layout and a complete parts list. It is also recommended that designers read the "U1000 Wideband Upconverter U1100/Dualband Upconverter Preliminary Data Sheet".

The U1100-EB is meant to be a demonstration circuit and evaluation tool. QUALCOMM does not make any warranty as to the U1100-EB suitability for a specific applications without further design modifications. However, we believe you will find the U1100-EB a useful tool in evaluating and understanding QUALCOMM's U1100.

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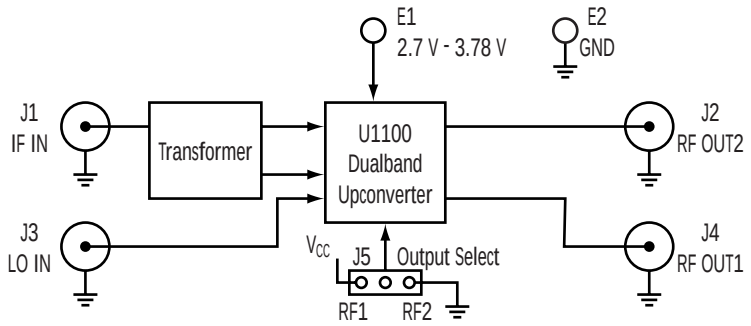
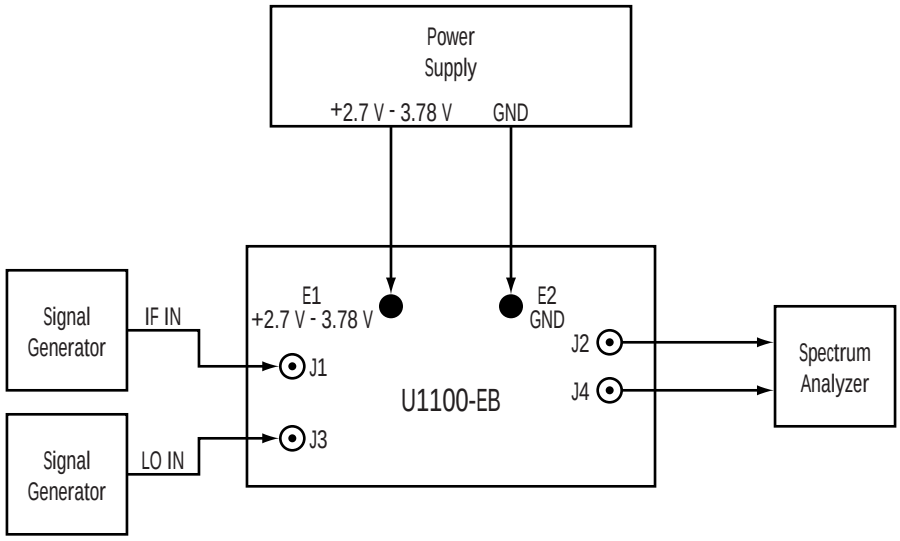
Figure 1. U1100-EB Block Diagram



2.0 GETTING STARTED

Operation of the U1100-EB is very simple. The board requires an LO and IF input via signal generators or other source to drive the U1100, while the RF output select is controlled via a simple jumper. The output of the U1100-EB is then measured by a spectrum analyzer. Test signals enter and exit the board via coax cables with SMA connectors. The U1100-EB requires only a single voltage, 2.7 V to 3.78 V, connected to E1 referenced to the Ground pin E2. A functional setup block diagram of the U1100-EB can be found in Figure 2.

Figure 2. U1100-EB Board Setup



2.1 REQUIRED EQUIPMENT

The U1100-EB comes fully configured for operation with minimal assembly. The following list of standard test equipment is provided as a baseline. If specific equipment is not available, equipment with equivalent functionality may be substituted.

Spectrum Analyzer	HP8563E
Signal Generators (2)	HP8648C
Power Supply	Leader LPS-152
Coax Cables	
Power cables	

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3.0 EVALUATION BOARD OPERATION

Figure 1 shows the U1100-EB block diagram. The following paragraphs describe the function and operation of each of the circuit elements shown in the block diagram.

3.1 INPUTS

3.1.1 POWER SUPPLY REQUIREMENTS

The U1100-EB requires a single voltage for proper operation. The U1100 requires from 2.7 V to 3.78 V, at a maximum of 35 mA connected to E1 referenced to the Ground pin E2.

3.1.2 IF INPUT (J1)

The IF input to the U1100-EB is applied on connector J1. This input is closely matched to 50 Ω. To minimize power loss to the U1100, a 4:1 impedance transformer was placed in between the 50 Ω IF Input and the U1100. The balun transformer purpose is two fold. First, it transforms the 50 Ω input impedance to 200 Ω but also turns the single ended input into a differential input which is routed to the U1100. The nominal frequency input to the IF port is 130.38 MHz with a maximum. The typical input P1db of the U1100 is -2.0 dBm in the cellular band and -1.5 dBm in the PCS band. There will be some IF power loss due to the impedance mismatch between the transformer and the U1100 IF input.

3.1.3 LO INPUT (J3)

The LO input to the U1100 is applied on connector J3. This connector is matched to 50 Ω. The LO input is directly routed to the U1100 and will suffer minimal power loss. The nominal frequency input to the LO port is 954 to 1780 MHz with a power level between -6 and 0 dBm.

3.1.4 RF OUTPUT SELECT CONTROL (J5)

The U1100 RF Output Select is controlled through jumper J5. When pins 1 and 2 of jumper J5 are connected, the U1100 select control pin is pulled to +5 volts. This will cause the U1100 to route the RF Output to RF OUT1, connector J4. When the RF output is routed to J4, the RF output of J2, RF OUT2, is invalid. When pins 2 and 3 of jumper J5 are connected, the U1100 select control pin is pulled low. This will cause the U1100 to route the RF output to RF OUT2, connector J2. When the RF output is routed to J2, the RF output of J4, RF OUT1, is invalid.

3.2 OUTPUTS

3.2.1 RF OUT1 (J4)

The output of the U1100 is either routed directly to connector J2 or J4 depending upon the location of the RF Select jumper J5. When jumper J5 is connected to pins 1 and 2, the RF Output of the U1100 will be routed to RF OUT1, J4. This output is matched to 50 Ω so impedance matching to a spectrum analyzer or power meter is not required. The typical conversion gain of the U1100 is -0.7 dB.

3.2.2 RF OUT2 (J2)

The output of the U1100 is either routed directly to connector J2 or J4 depending upon the location of the RF Select jumper J5. When jumper J5 is connected to pins 2 and 3, the RF Output of the U1100 will be routed to RF OUT2, J2. This output is matched to 50 Ω so impedance matching to a spectrum analyzer or power meter is not required. The typical conversion gain of the U1100 is -0.7 dB.

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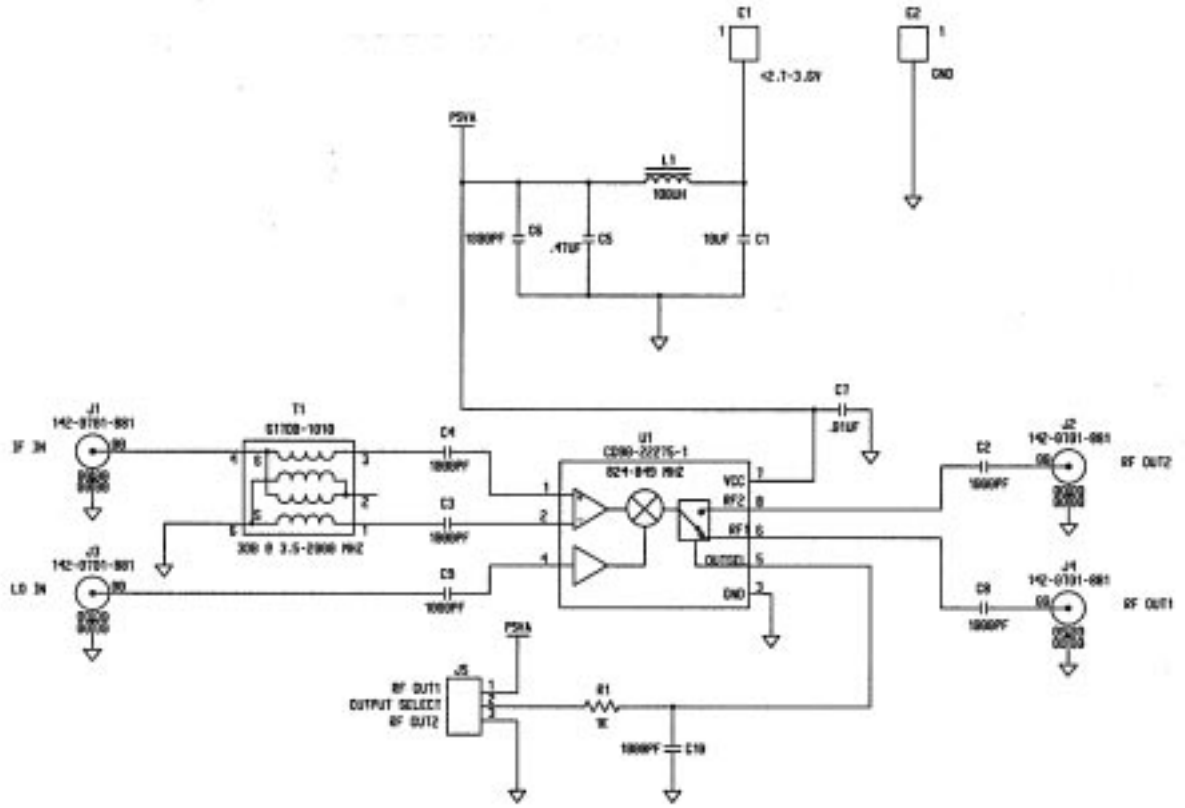
4.0 APPENDIX

4.1 APPENDIX A U1100-EB SCHEMATICS



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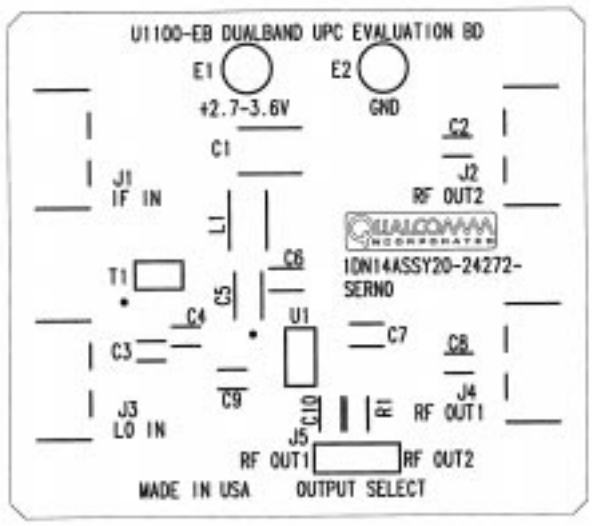
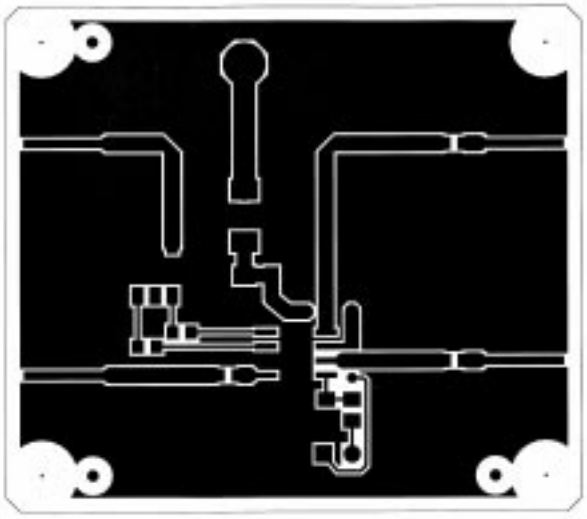
4.2 APPENDIX B U1100-EB LAYOUT DRAWINGS

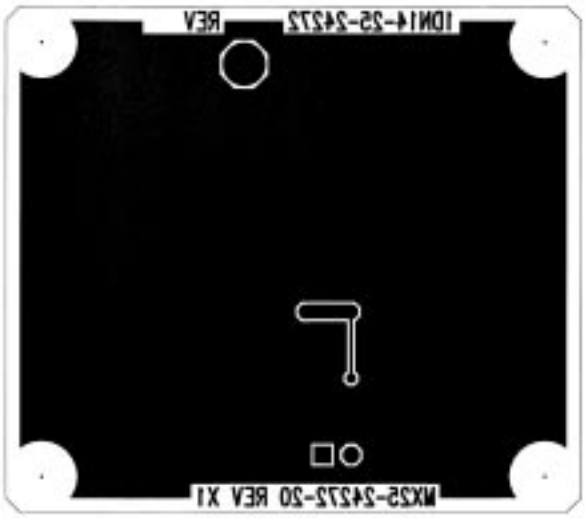
U1100-EB Top Silk Layout



U1100-EB Top Traces Layout



U1100-EB Bottom Traces Layout



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4.3 APPENDIX C U1100-EB PARTS LIST

REFERENCE DESIGNATOR	QTY	MANUFACTURERS PART NUMBER	PART DESCRIPTION
	1	24-24272-1	PWB,U1100-EB, DUALBAND UPC EVALUATION BOARD
R1	1	MCR10F1001	RES, CHIP THICK FILM 1.0K 1% .1W
C6, C10	2	C0805C102K1RAC	CAP, CHIP CERAMIC 1000PF 10% X7R
C7	1	C0805C103K5RAC	CAP, CHIP CERAMIC .01UF 10% X7R
C2-C4, C8, C9	5	C0603C101J5GAC	CAP, CHIP CERAMIC 100PF 5% COG/NP0
C5	1	THCS30E1H474ZT	CAP, CHIP CERAMIC 0.47UF +80/-20%
C1	1	THCS50E1E106ZT	CAP, CHIP CERAMIC 10UF +80/-20%
L1	1	IMC-1812 100UH 10%	INDUCTOR, CHIP 100UH 10% Q=50
T1	1	617DB-1010	TRANSFORMER, BALUN FREQ MIXER
E1, E2	2	160-1558-02-01-00	TERMINAL, SOLDER TURRET SILVER .062
J5	1	TSW-103-07-L-S	CONN, STRIP HEADER .025SQ 1X3 POS
J1-J4	4	142-0701-881	CONN.SMA JACK RCPT END LAUNCH
U1	1	U1100	DUALBAND UPCONVERTER