PLESSEY
Semiconductors

SP9131

520 MHz DUAL TYPE D MASTER SLAVE FLIP-FLOP

The SP9131 is a dual master slave type D flip-flop which is pin-for-pin compatible with the rECL10131, but with improved dynamic performance and increased power dissipation.

R-S TRUTH TABLE

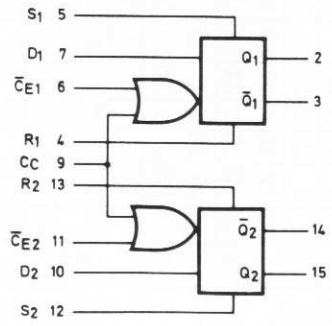
R	S	Q_n+1
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

CLOCKED TRUTH TABLE

C	D	Q_n+1
L	ø	Q_n
H	L	L
H	H	H

ø = Don't Care
$C = \overline{C_E} + C_C$.
A clock H is a clock transition from a low to a high state.

$P_D = 364\,mW$
$f_{Tog} = 520\,MHz$ (typ)



VCC1 = Pin 1
VCC2 = Pin 16
VEE = Pin 8

Fig. 1 Logic diagram

ELECTRICAL CHARACTERISTICS

Each circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and a transverse air flow greater than 500 linear FPM is maintained. Outputs are terminated through a 50-ohm resistor to −2.0Volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

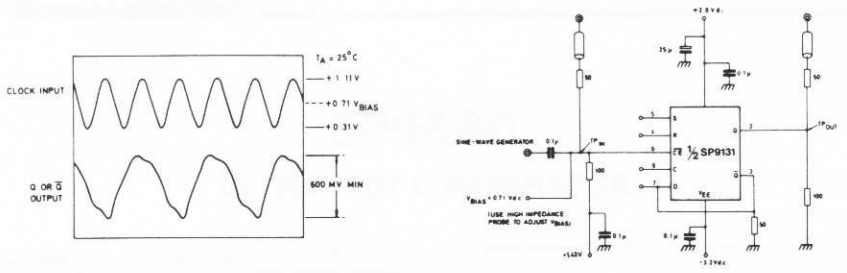
Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
−30°	−0.89	−1.89	−1.205	−1.500	−5.2
+25°	−0.81	−1.85	−1.105	−1.475	−5.2
+85°	−0.70	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	SP9131 Test Limits −30 C Min	−30 C Max	+25 C Min	+25 C Typ	+25 C Max	+85 C Min	+85 C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(Vcc) Gnd
Power Supply Current	I_E	8	—	—	—	70	87	—	—	mAdc	—	—	—	—	8	1,16
Input Current	I_{inH}	4	—	—	—	—	600	—	—	µAdc	4	—	—	—	8	1,16
		5	—	—	—	—	600	—	—		5	—	—	—		
		6	—	—	—	—	300	—	—		6	—	—	—		
		7	—	—	—	—	300	—	—		7	—	—	—		
		9	—	—	—	—	420	—	—		9	—	—	—		
Input Leakage Current	I_{inL}	4,5,*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1,16
		6,7,9*	—	—	0.5	—	—	—	—	µAdc	—	—	—	—	8	1,16
Logic "1" Output Voltage	V_{OH}	2	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	5	—	—	—	8	1,16
		2*	-1.06	-0.89	-0.96	—	-0.81	-0.89	-0.70	Vdc	7	—	—	—	8	1,16
Logic "0" Output Voltage	V_{OL}	3	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	5	—	—	—	8	1,16
		3*	-1.89	-1.675	-1.85	—	-1.65	-1.825	-1.615	Vdc	7	—	—	—	8	1,16
Logic "1" Threshold Voltage	V_{OHA}	2	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	5	—	8	1,16
		2*	-1.08	—	-0.98	—	—	-0.91	—	Vdc	—	—	7	9	8	1,16
Logic "0" Threshold Voltage	V_{OLA}	3	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	5	—	8	1,16
		3*	—	-1.655	—	—	-1.63	—	-1.595	Vdc	—	—	7	9	8	1,16
Switching Times											+1.11 Vdc		Pulse In	Pulse Out	+3.2Vdc	+2.0Vdc
Clock Input Propagation Delay	t_{9-2-}	2	—	—		1.0	—	—	—	ns	—	—	9	2	8	1,16
	t_{9-2-}	2	—	—				—	—		7	—	9	2		
	t_{16-2-}	2	—	—				—	—		7	—	6	2		
	t_{16-2-}	2	—	—				—	—		—	—	6	2		
Rise Time (20 to 80%)	t_{2-}	2	—	—		1.0		—	—		7	—	9	2		
Fall Time (20 to 80%)	t_{2-}	2	—	—				—	—		—	—	9	2		
Set Input Propagation Delay	t_{5-2-}	2	—	—		1.0		—	—	ns	—	—	5	2	8	1,16
	t_{12-15-}	15	—	—				—	—		6	—	12	15		
	t_{5-3-}	3	—	—				—	—		—	—	5	3		
	t_{12-14-}	14	—	—				—	—		9	—	12	14		
Reset Input Propagation Delay	t_{4-2-}	2	—	—		1.0		—	—	ns	—	—	4	2	8	1,16
	t_{13-15-}	15	—	—				—	—		6	—	13	15		
	t_{4-3-}	3	—	—				—	—		—	—	4	3		
	t_{13-14-}	14	—	—				—	—		9	—	13	14		
Setup Time	t_{setup}	7	—	—		—	1.0	—	—	ns	—	—	6.7	2	8	1,16
Hold Time	t_{hold}	7	—	—		—	0.2	—	—	ns	—	—	6.7	2	8	1,16
Toggle Frequency (Max)	f_{TOG}	2	—	—	5.0		—	—	—	MHz	—	—	6 *	2	8	1,16

*Individually test each input; apply $V_{IL\ min}$ to pin under test.

* Output level to be measured after a clock pulse has been applied to the C_E input (pin 6) $V_{IH\ max}$ / $V_{IL\ min}$

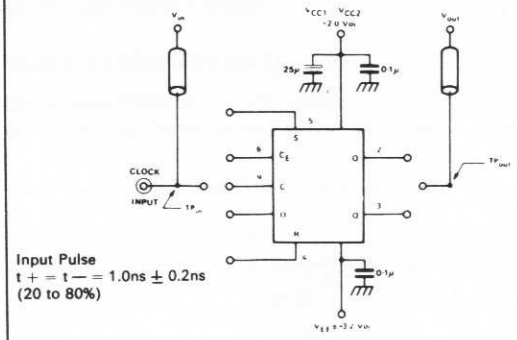
This is advance information and specifications are subject to change without notice.



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

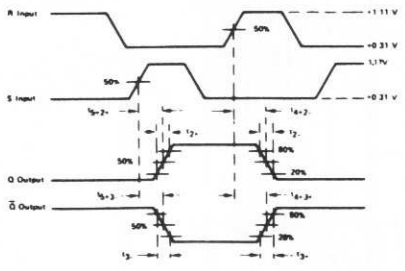
Fig. 2 Toggle frequency test circuit

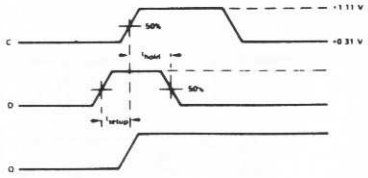


Input Pulse
t + = t — = 1.0ns ± 0.2ns
(20 to 80%)

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.





NOTE:
t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).
t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

Fig. 3 Switching time test circuit and waveforms at +25°C

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