A High Performance Magnetron Radar Transmitter Design Study

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Abbreviations

CFM	Cubic Foot per Minute
COHO	COHerent Oscillator
CSA	Cross Sectional Area
CMRR	Common Mode Rejection Ratio
DC	Direct Current
EPROM	Erasable Programmable Read Only Memory
FSD	Full Scale Deflection
GHz	Giga Hertz
HT	High Tension
HV	High Voltage
Hz	Hertz
I/F	Improvement Factor
kV	Kilo-Volt
LSB	Lowest Significant Bit
MHz	Mega Hertz
MOSFET	Metal Oxide Silicon Field Effect Transistor
MSB	Most Significant Bit
MTI	Moving Target Indication
MW	Mega Watt
OP AMP	Operational Amplifier
PBA	Printed Board Assembly
PEC	Printed Electric Circuit
PIV	Peak Inverse Voltage

PRI	Pulse Repetition Interval
PRF	Pulse Repetition Frequency
PSRR	Power Supply Rejection Ratio
PW	Pulse Width
RMS	Root Mean Square
SMPS	Switch Mode Power Supply
STALO	STAble Local Oscillator
+ve	Positive
-ve	Negative

Preface

I Introduction

Increasing volume of air traffic and the market demand for a low cost, high reliability air traffic control radar, has led to the development of a high performance Primary Surveillance Radar, known as SURVEYOR.

The SURVEYOR Primary Surveillance Radar is used to detect and monitor aircraft movements within a radius of 100 nautical miles of an airport to enable safe management of air traffic.

The SURVEYOR has two radar transmitter-receiver systems operating on different frequencies in the range 2.7 GHz to 2.9 GHz (tunable), in parallel to provide high radar availability and enhanced detection. One of the radar systems working alone provides full performance as published even in the worst weather conditions.

The radar system is simple in architecture (see Figure 1), having a Transmitter, a rotating antenna, a Receiver and a Moving Target Indication Digital Signal Processor. The MTI DSP enables the radar to extract and display only aircraft that are moving and reject all returned signal echoes from static land features and certain weather conditions (eg: rain, fog, snow, clouds etc) known as Clutter.

The stability of the transmitted pulse in frequency, amplitude and time jitter has considerable effect on the radar's ability to extract aircraft (targets) and reject Clutter. Improvements to transmitter stability are the subject of this paper.

The new radar offers comparable performance and better value for money than more complex radars using driven linear beam tube or solid state transmitters.

Appendix 1: The published specification sheets.

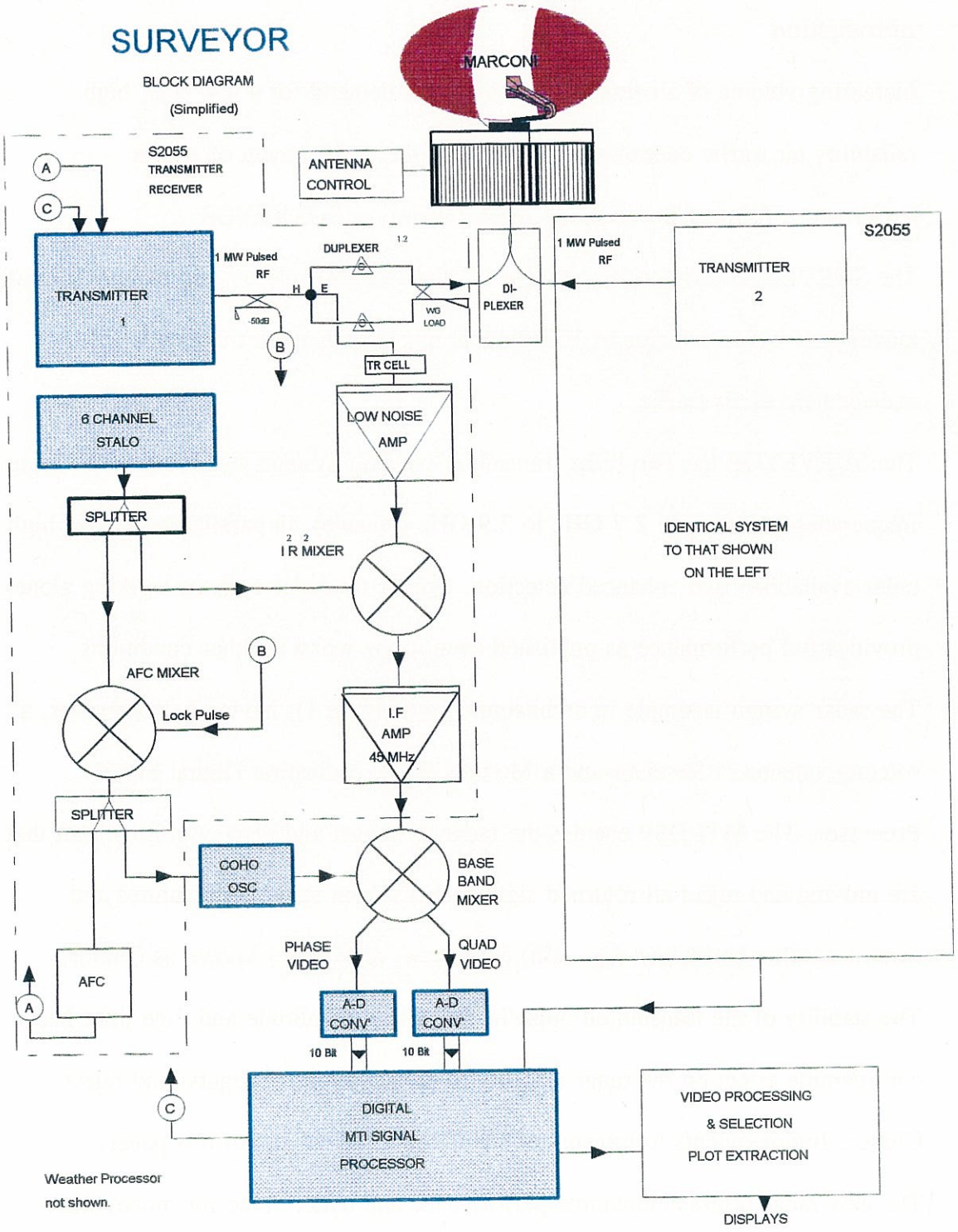

SURVEYOR
BLOCK DIAGRAM
(Simplified)
MARCONI
S2055
TRANSMITTER
RECEIVER
ANTENNA
CONTROL
A
C
TRANSMITTER
1
1 MW Pulsed
RF
DUPLEXER
1.2
H
E
50dB
WG
LOAD
DI-
PLEXER
B
TR CELL
LOW NOISE
AMP
6 CHANNEL
STALO
SPLITTER
2 2
I R MIXER
AFC MIXER
Lock Pulse
I.F
AMP
45 MHz
SPLITTER
COHO
OSC
BASE
BAND
MIXER
PHASE
VIDEO
QUAD
VIDEO
AFC
A-D
CONV'
A-D
CONV'
10 Bit
10 Bit
DIGITAL
MTI SIGNAL
PROCESSOR
VIDEO PROCESSING
& SELECTION
PLOT EXTRACTION
DISPLAYS
Weather Processor
not shown.
S2055
1 MW Pulsed
RF
TRANSMITTER
2
IDENTICAL SYSTEM
TO THAT SHOWN
ON THE LEFT

Figure 1

S2055 Transmitter

The superior performance of the Surveyor radar system is achieved by the incorporation of a very high stability compact Solid State Modulator/Coaxial Magnetron transmitter.

A block diagram of the transmitter is shown in Figure 2.

The transmitter has been designed to operate up to 3 magnetrons (switched), any magnetron type, on any frequency required, to provide flexibility for future systems.

The Surveyor application of the transmitter incorporates a single 1 MW peak power coaxial magnetron, matched to a solid state modulator, optimised to achieve the high stability required by modern MTI Radar Systems.

The compact nature of the transmitter is shown in Figure 3, the units being fitted into the lower half of a standard 19" cabinet. The Charging Unit, Modulator and Magnetron Heater Power Supplies are located in the lower half of an adjacent 19" cabinet on the left.

Design Aim

II The aim was to achieve an Overall System MTI Improvement Factor of 50dB minimum. To do this it was necessary to tailor the design of certain units within the S2055 transmitter which have significant influence over the stability of the transmitted RF pulse.

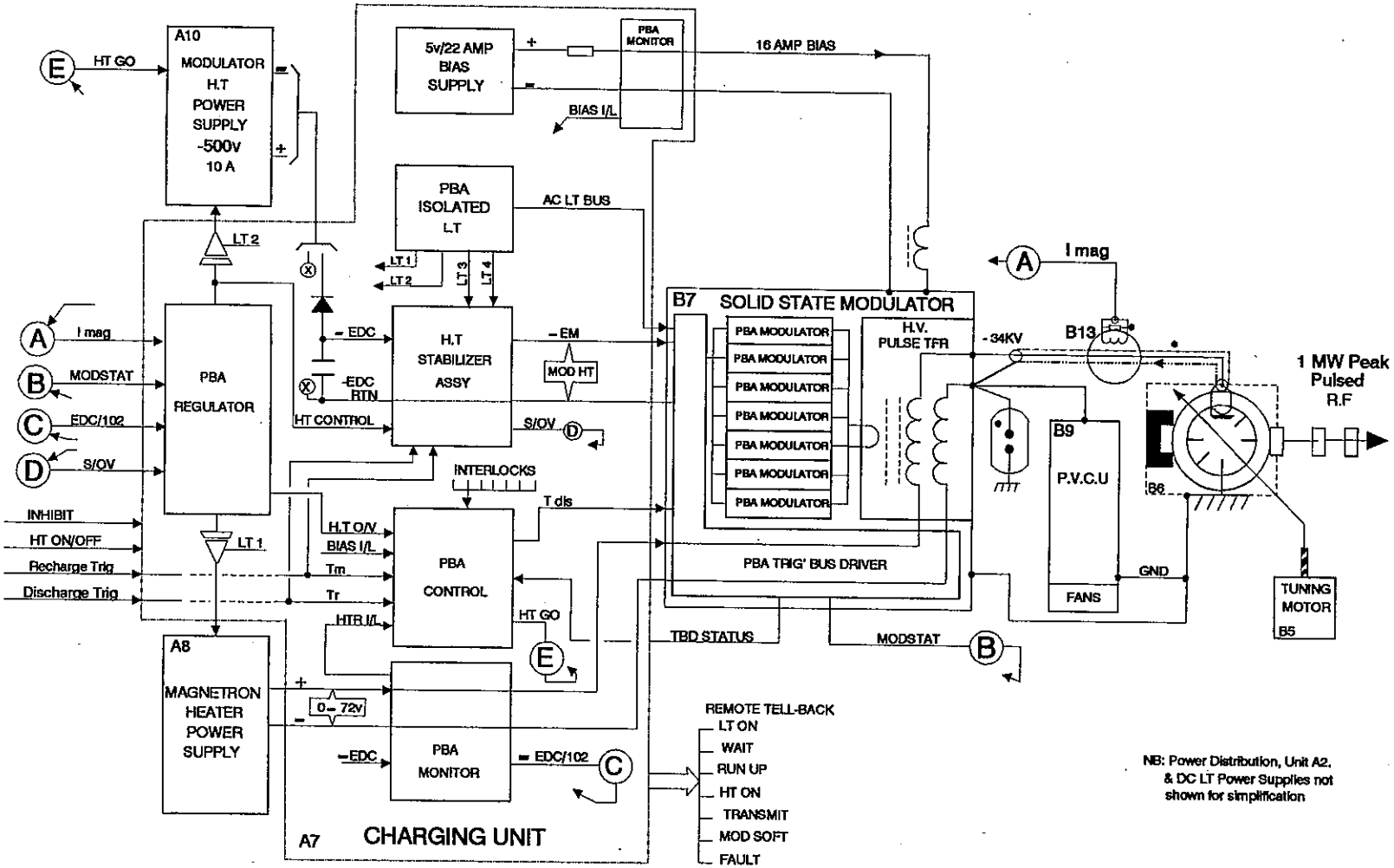
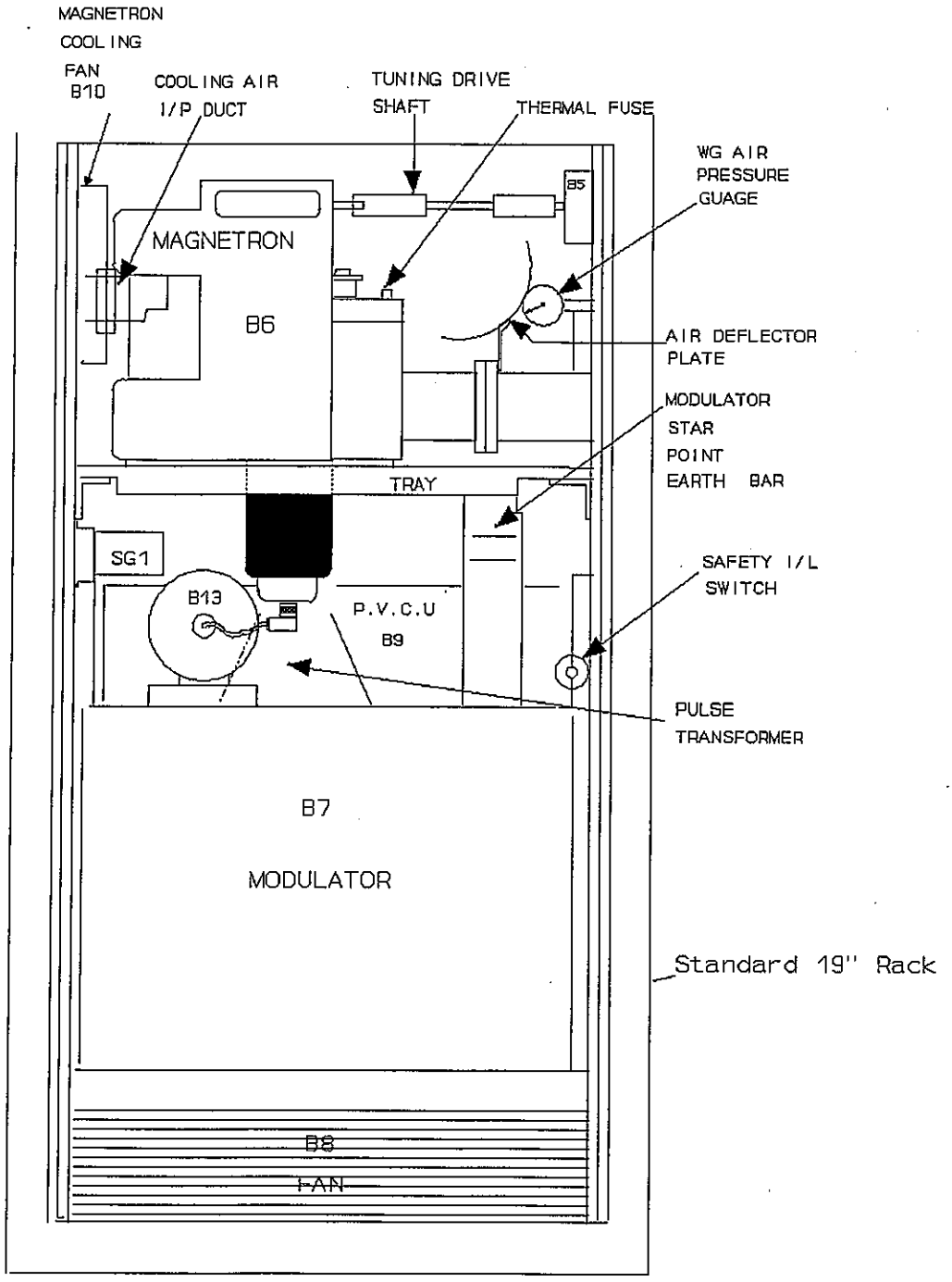


Fig 2: S2055 TRANSMITTER Block Diagram



MODULATOR COMPARTMENT

(Front View)

Figure 3

III Background

The Surveyor radar has been formed using existing designed units with the exception of certain units within the transmitter.

The contributions limiting the overall improvement factor (I/F) of the system transmitter are those due to Jitter on the front edge and Frequency Stability of the transmitted RF pulse.

Units that have enabled the Surveyors Overall MTI I/F of 50 dB to be achieved are the subject of this paper.

Chapter 1 **Magnetron Cathode Heater Controller.**

A circuit that automatically controls the heating of the magnetron cathode, to achieve maximum valve life and low front edge jitter of the RF pulse.

Chapter 2 **Modulator HT Stabilizer.**

A unit that controls the charging of the modulator energy storage capacitors, stabilizing the voltage (nominally -350v) to within 10mV (typ) over any group of 4 PRI intervals, independent of supply variations due to PRI stagger.

Modulator HT voltage stabilization is the prime requisite inxchieving high frequency stability from magnetron transmitters.

Chapter 3 **Pulse Voltage Control Unit.**

A unit that shapes the front edge profile of the -34kV pulse applied to the magnetron cathode, in order to achieve efficient start up of oscillation for lowest jitter on the front edge of the transmitted RF pulse.

CHAPTER 1

Magnetron Cathode Heater Controller

Design Study

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CHAPTER 1

Magnetron Cathode Heater Controller (MCHC)

Design Study

1.1 Introduction

Long life and high stability (low jitter) operation of any magnetron relies on operating the cathode at an optimum temperature.

A manufacturer of valves has reported that the most common reason for premature valve failure is due to operation with incorrect heater voltage, which suggested that a new approach to magnetron heater control was required.

1.2 Design Aim

The design aim was to produce a magnetron heater control circuit that measures the mean power into the magnetron cathode and controls the heater voltage proportionally as required to ensure that the cathode temperature is optimised for long valve life and low jitter on the front edge of the transmitted RF pulse.

1.3 Background

Prior to the S2055 MG5403 magnetron pulsing at some duty, the cathode is pre heated with the heater voltage set to 70v @ 2.7 Amps. The tungsten matrix (sponge reservoir) cathode is loaded with barium aluminate (see Figure 1.1) which when heated forms an electron cloud layer hovering above the cathode surface. The life of the magnetron is determined by the operating time that it takes to deplete the cathode of barium aluminate, such that electron emission is reduced. Reduced emission starves the rotating space charge of electrons which causes excessive moding(oscillation build-up at non π mode frequencies during start-up) and results in poor jitter performance.

When a magnetron is pulsed, the cathode heater voltage must be reduced to ensure that the cathode is not over heated due to back-bombardment of electrons. Electron emission due to the application of heater voltage is referred to as Primary Emission. When the magnetron is operated at a duty of 0.001344 nearly all of the emission is Secondary Emission due to back-bombardment of the cathode surface. When the magnetron is pulsed and the rotating circumferential space charge is formed in the space between the cathode and anode vanes, interaction occurs between the outer layers of electrons and the oscillating electric fields on the vane edges. Electrons approaching vanes which are more +ve are attracted to the vanes to form the anode current. Electrons approaching vanes which are more -ve decelerate and are pushed back towards the cathode with added energy from the slow wave structure.

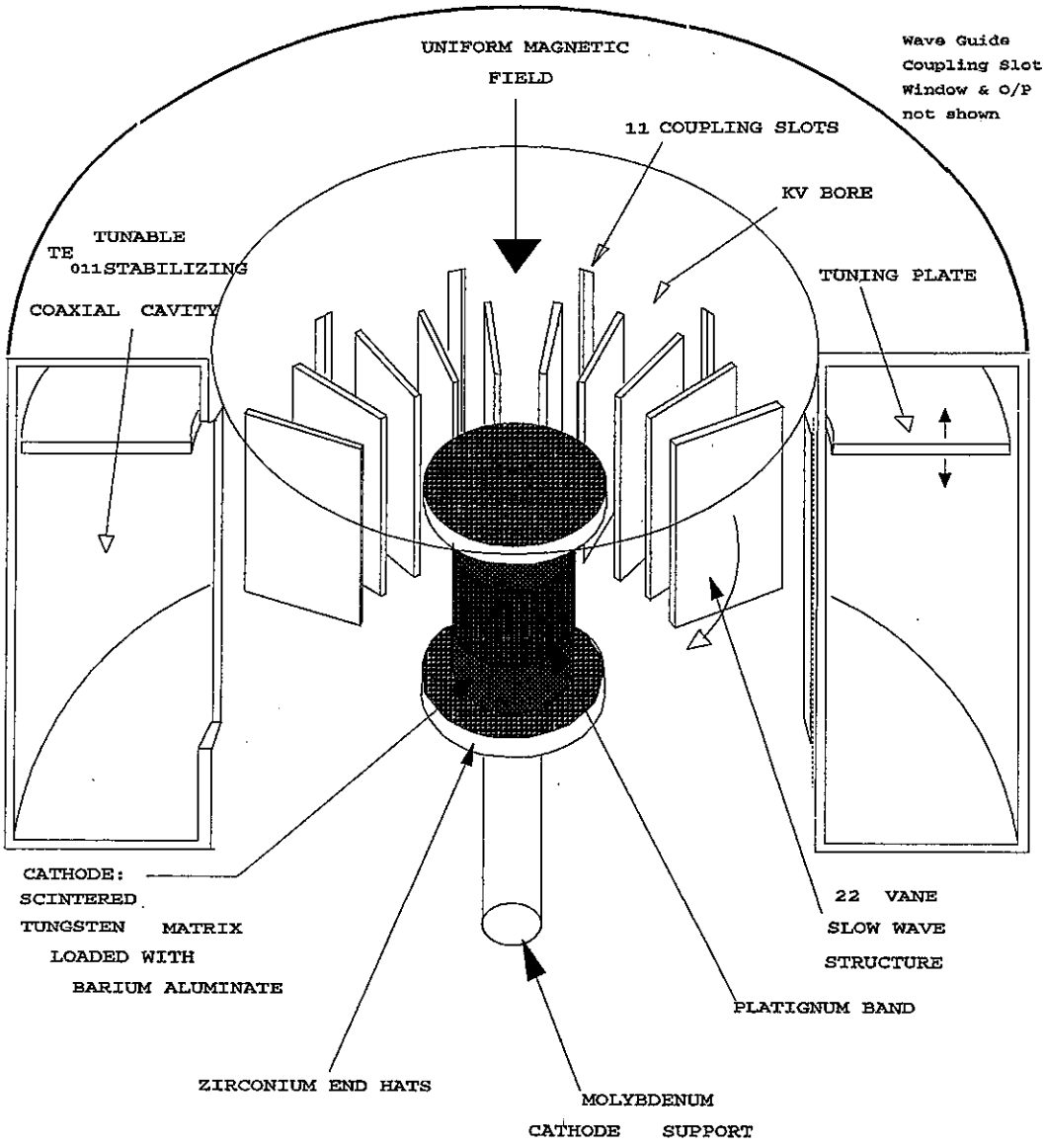

UNIFORM MAGNETIC
FIELD
Wave Guide
Coupling Slot
Window & O/P
not shown
11 COUPLING SLOTS
KV BORE
TUNABLE
TE
011STABILIZING
COAXIAL CAVITY
TUNING PLATE
CATHODE:
SCINTERED
TUNGSTEN MATRIX
LOADED WITH
BARIUM ALUMINATE
22 VANE
SLOW WAVE
STRUCTURE
PLATIGNUM BAND
ZIRCONIUM END HATS
MOLYBDENUM
CATHODE SUPPORT

Figure 1.1

Any kinetic energy that the electrons have is given up as heat as they hit the cathode surface. A platinum band is fitted around the middle area of the cathode surface to receive the bombarding electrons, and is the main source of electrons. Electrons bombarding areas of the cathode not protected by the platinum band can cause cathode material to evaporate and coat other adjacent surfaces.

Any other surface, eg, End Hats , when coated in cathode material become primary emitters producing electrons which is un-desirable. The End Hats are disks at either end of the cathode, and are used to focus the space charge such that it is directed at the central region of the anode vanes, thus reducing leakage current to other parts of the anode cylinder. The End Hats are made from Zirconium, which raises the work function of the barium coating and thus reduces the emissivity.

The heater controller must proportionally reduce the externally applied heater power as the mean input power to the cathode increases following a defined law.

In the S2055 transmitter the MG5403 operating at a duty of 0.001344 requires a heater voltage that varies typically between 10 and 0v depending on the efficiency of the magnetron. The mean input power at the cathode is adjusted as required to produce 1 MW peak RF o/p power.

The efficiency (typically between 48% and 65%) also varies with frequency across the band 2.7 GHz to 2.9 GHz.

The electron emission from the cathode surface is proportional to (Cathode Surface Temperature)^4 therefore cathode heater voltage control must be accurate.

1.4 The Requirement

The requirement for the design:-

a, To automatically control the magnetron heater power supply for a 1, 2 or 3 magnetron system, selectable via a 3 input and return control signal.

Note: The MCHC was designed not only to meet the S2055 requirements but also possible future systems having up to 3 magnetrons driven from the same modulator.

b, To control the selected magnetron heater voltage to achieve low jitter on the front edge of the transmitted RF pulse for any duty and mean power at which the valve is operated at all times.

c, To provide easy selection and re-programming of 9 'heater voltage turndown laws' for each of the 3 magnetron options.

1.5 Selection of Hardware

The requirement as described above suggests that a combined analogue and digital solution (including software) was necessary. The need to have many easily selectable 'heater voltage turndown laws' indicated that a EPROM was required, with a digital means of selection preferably without the complexity of a micro-processor.

One possible solution would have been to use an 'off the shelf', low end of the range embedded micro-controller, however the simplest design solution has the highest reliability and lowest component count.

To enable easy adjustment or creation of a new law, a software utility program was required, to generate the data for the 'look-up' tables for the magnetrons and organise the data into the correct format for programming the EPROM.

In order to assess the mean input power to the magnetron cathode, a means of monitoring the magnetron cathode peak current was required. The magnetron peak current sample would then have to be integrated and digitized, indicating a need for an Analogue to Digital converter. A Digital to Analogue converter would also be required to convert the digital heater voltage control data from the EPROM into a 0 to 5 v control voltage to drive the Switch Mode Power Supply used to provide the magnetron heater voltage.

The functions required are shown in Figure 1.2.

The most important operating parameter of a magnetron that should be monitored and regulated is the peak cathode current, it determines the peak RF power output and the frequency stability. The peak cathode current is set and regulated by controlling the modulator primary HT, this is performed by the HT Regulator circuit on the PBA Regulator.

The Solid State Modulator used in the new transmitter provides a current pulse sample, which has been used in previous radar transmitters for HT regulation and heater control. However, as the sample is monitored at the earthy end of the HV Pulse Transformer secondary bi-filar windings the current waveform produced comprises not only the magnetron cathode current pulse but also the current taken by the Pulse Voltage Control Unit and the magnetizing current of the HV Pulse Transformer. The distortion caused by the PVCU is such that the current pulse sample provided is un-suitable for use by the PBA Regulator for cathode peak current regulation or heater control.

It was decided not to use the existing current monitor, and to design a new magnetron cathode current monitor which would provide a true sample waveform.

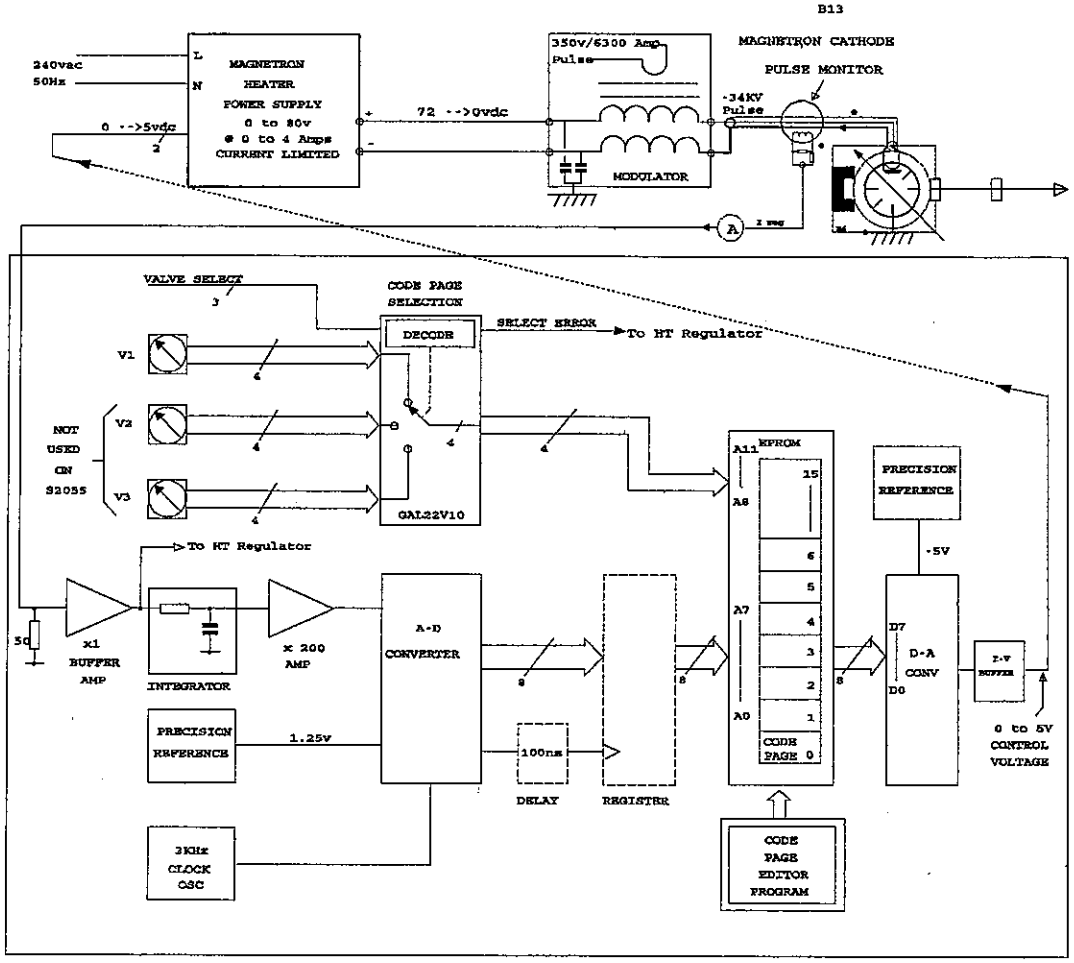


Figure 1.2

Magnetron Cathode Heater Controller, Functional Diagram

1.6 **Magnetron Cathode Current Pulse Monitor** (B13)

The PBA Regulator MCHC and HT control circuits require a 10 Amp/volt scaled cathode current pulse sample delivered via a 50 ohm coaxial cable.

Monitoring the cathode current pulse at the cathode/heater coaxial input to the magnetron required a toroidal pulse transformer insulated and shielded to withstand the -34 KV cathode pulse. The primary of the monitoring pulse transformer is formed by the short coaxial cable (RG 223/U) inter-connection between the output terminals of the HV Pulse Transformer and the cathode/heater input to the magnetron. The outer (double) shield of the coaxial cable carries the 52 Amp (typ) cathode current pulse, and the return for the cathode heater is via the centre conductor. The magnetic flux due to the heater current cancels in the primary coaxial cable.

B13 is located as shown in Figure 1.3:

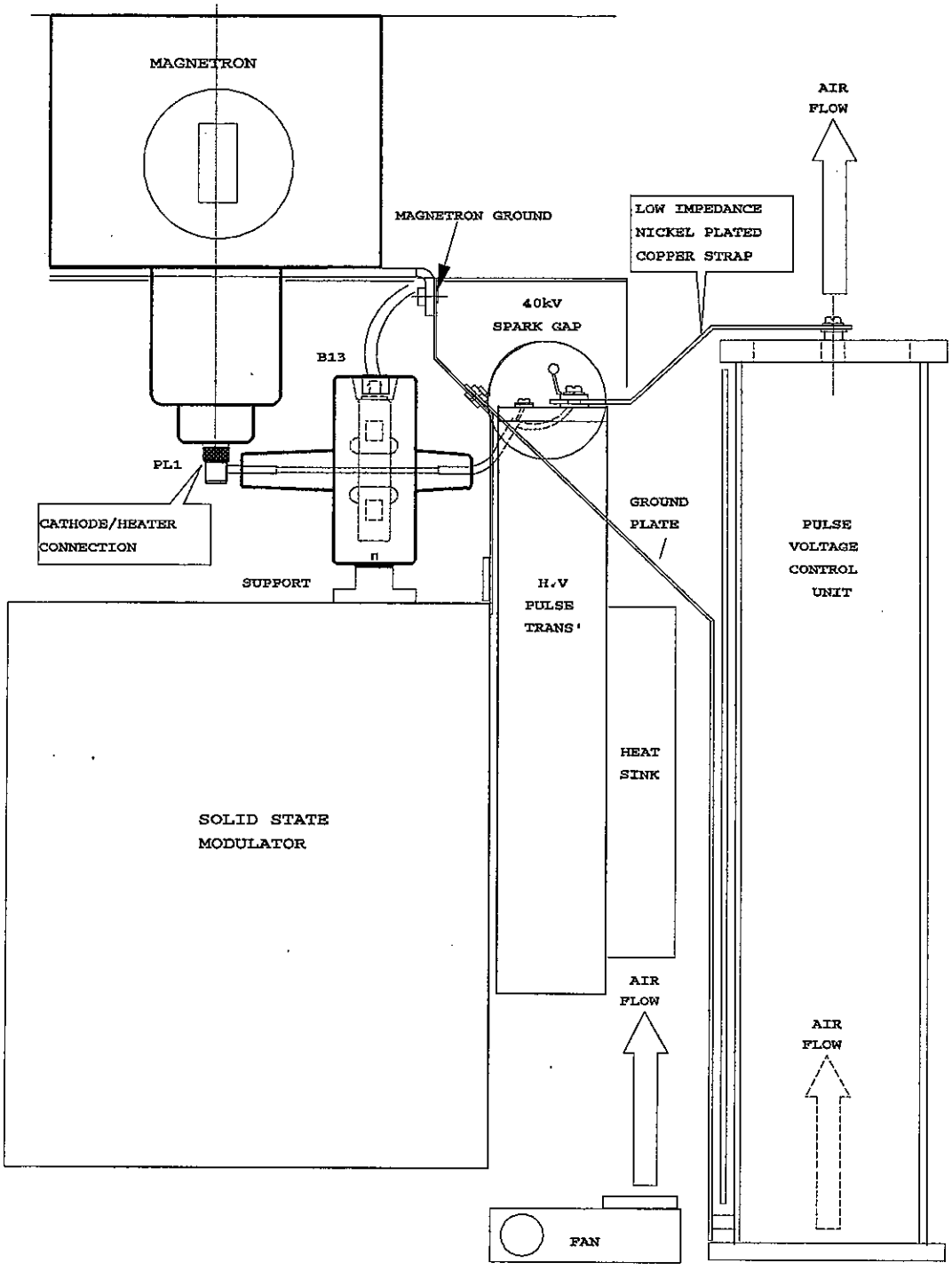


Figure 1.3

Modulator Compartment (Side View)

1.7 Insulation and Shielding to prevent Corona

The core, secondary winding and associated components (at earth potential) have to be insulated and screened from the central primary coax outer conductor which is pulsed at -34KV. The electrostatic screen as shown in Figure 1.4, is designed to control the voltage gradient (Electric Field Strength "E"in Volts/metre) between the outer conductor surface of the primary coax and the earthy core and secondary components. E can be very much greater in potential than the applied 34KV due to increased electric flux density "D" in the regions of sharp edges, radii and contours of the components. The total dielectric strength in volts of the insulating medium must always exceed the maximum electric field strength E.

Corona is caused by the acceleration of electrons or ions by intense electric fields. The accelerated electrons collide with other atoms to release more electrons, releasing heat and light. Corona if observed appears as a faint blue glow. The corona activity causes the chemical conversion of the insulation material into carbon, silicon slime and other substances. The substances produced greatly reduce the dielectric strength of the insulation and total break down occurs eventually. Corona activity if allowed to occur on any leads or components connected to the magnetron cathode has an adverse effect on jitter performance.

Corona in the insulating medium is minimised by:

a, Avoiding sharp edges or points and having a shield with carefully contoured surfaces to control the electric gradient or field strength E, such that break down of the insulation does not occur. Both metallic surfaces must be considered.

b, To have an insulating medium (dielectric) of one type with constant relative permittivity ϵ_r.

The electric field strength E is increased at the boundaries between dis-similar dielectrics. For example: if air bubbles are trapped in the epoxy resin. Vacuum moulding techniques are essential in the potting processes, to remove all air bubbles and ensure that the potting material fills all crevices in the component.

The monitoring transformer is produced in two phases. The first phase is to mould the core assembly (Figure 1.5). The core assembly incorporates the wound core, 3 resistors, 2 zeners and a BNC connector. The core assembly is a toroidal shape with a 26 mm diameter hole through the centre. The electrostatic shield is shown and produced by coating the moulded core assembly with silver all over. A break in the shield is then cut as shown in order to prevent current from flowing around the electrostatic shield (shorted turn effect). The BNC plug that mates with the socket on the core box has a independent safety earth wire that is connected to the modulator earth.

The second phase of manufacture is that the core assembly is supported centrally inside a split mould with the prepared coaxial cable running through the centre (Figure 1.6). The outer insulation of the coaxial cable is removed as shown in the central region so that the only dielectric material between the electrostatic shield and the outer silver plated conductor of the coaxial primary is the resin. The mould is then filled with resin under vacuum.

1.8 Thickness of Resin, between Primary and Electrostatic Shield

The Monitoring Transformer will have -34KV Pulsed (3μS max PW) applied to its central primary conductor.

The thickness of the resin required in the central region between the outer conductor of the primary and the surface of the electrostatic shield is determined by considering the worse case Electric Field Strength "E" and the Dielectric Strength of the resin used (10 MV/m).

The greatest electric field strength is in the middle region where there are effectively two concentric cylinders, the inner cylinder being the outer conductor of the coax and the outer cylinder being the inner surface of the electrostatic shield.

The resin dielectric used has a relative permittivity k = 3·84.

The primary electric constant $\epsilon_0 = 8{\cdot}854 \cdot 10^{-12}$. Farads/meter

The absolute permittivity of the dielectric material:

$$\epsilon_a = \epsilon_0 \cdot k \text{ F/m} \qquad (1.8.1)$$

$$\epsilon_a = 8{\cdot}854 \cdot 10^{-12} \cdot 3{\cdot}84 = \underline{3{\cdot}4.10^{-11}} \text{ F/m.} \qquad (1.8.2)$$

From first principles:-

To determine the worse case electric field strength E:

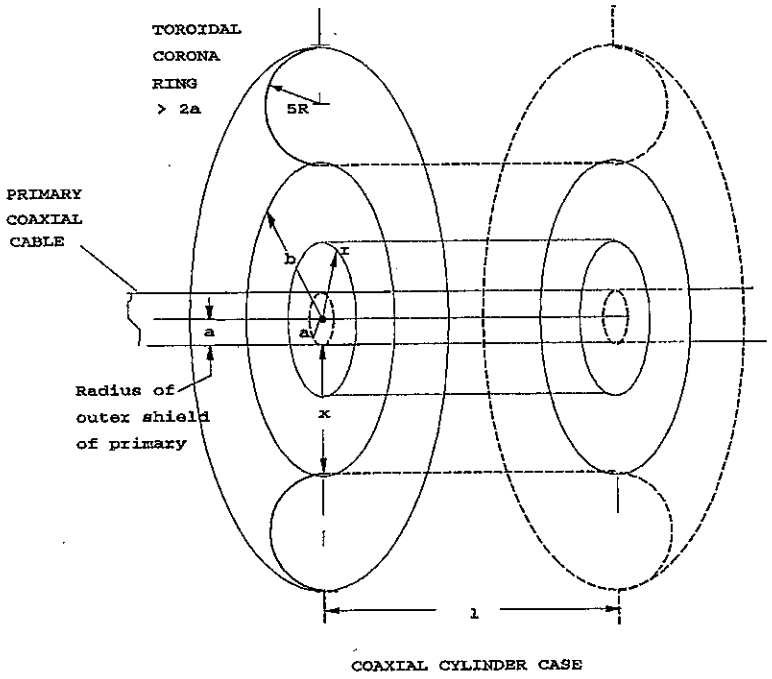


Figure 1.4

When the primary coaxial cable is pulsed to -34KV during operation, a -ve charge of "q" Coulombs is set up on the outer surface of the inner cylinder. This in turn produces an electric force field E between the inner cylinder and the inside surface of the outer cylinder (electrostatic shield at earth potential). The lines of electric flux Ψ produced by E are perpendicular to the cylinder surfaces, passing through the insulating dielectric resin, pointing in towards the inner cylinder.

The electric flux density:

$D = \Psi/\text{Area in Coulombs/meter}^2$ (1.8.3)

Also, as Electric Flux Ψ is quantified in Coulombs/meter (q'/m)

$D = q'/(2.\pi r.l)$ C/m^2 (1.8.4)

Where q' is the charge in coulombs on a 1 meter length.

Where $2\pi rl$ is the surface area of an imaginary cylinder of radius r, through which the flux passes, between the limits a and b, such a surface is called a "Gaussian" surface.

The flux density is maximum when "r" is close to the radius "a".

The flux density D is also related to the absolute permittivity of the resin ϵ_a and the electric field strength E:

$$D = \epsilon_a E \text{ Coulombs/m}^2 \qquad (1.8.5)$$

Therefore, substituting $\epsilon_a E$ for D in (1.8.4):

$$\epsilon_a E = q'/2\pi r \text{ Coulombs/m}^2 \qquad (1.8.6)$$

$$E = q'/2\pi\epsilon_a r \text{ volts/m} \qquad (1.8.7)$$

$$q' = E.2\pi\epsilon_a r \text{ Coulombs} \qquad (1.8.8)$$

The total potential difference between radius a and b:

$$V = \int_a^b E\, dr. \text{ volts} \qquad (1.8.9)$$

Substituting (1.8.7) $(q'/2\pi\epsilon_a r)$ for E in (1.8.9)

$$V = \int_a^b (q'/2\pi\epsilon_a r)\, dr \text{ volts} \qquad (1.8.10)$$

$$\therefore V = (q'/2\pi\epsilon_a) \int_a^b dr/r. \text{ volts} \qquad (1.8.11)$$

$$\therefore V = (q'/2\pi\epsilon_a).\ln (b/a). \text{ volts} \qquad (1.8.12)$$

A relationship for the capacitance/meter for the coaxial cylinder case may be derived using the fact that C = Q/V, leading to $C = (2\pi\epsilon_a)/\ln(b/a)$ F/meter.

To derive an expression to include V, E & (b/a), substitute (1.8.8) $(E.2\pi\epsilon_a r)$ for q' in (1.8.12):

$$V = (E.2\pi\epsilon_a r/2\pi\epsilon_a).\ln (b/a) \quad = E.r.\ln(b/a) \text{ volts} \qquad (1.8.14)$$

Electric Field Strength $E = V/[r.\ln(b/a)]$ V/m. (1.8.15)

In order to determine a minimum value for the thickness of resin ("x" in Figure 1.4), expression 1.8.15 is re-arranged to find x, where b is replaced by "a+x":-

$$E = \frac{V}{r.\ln(a+x)/a} \quad (1.8.16)$$

$$E.r.\ln(a+x)/a = V \quad (1.8.17)$$

$$\ln(a+x)/a = V/E.r \quad (1.8.18)$$

$$(a+x)/a = e^{V/E.r} \quad (1.8.19)$$

$$a+x = a.e^{V/E.r} \quad (1.8.20)$$

$$x = a.e^{V/E.r} - a \quad (1.8.21)$$

$$x = a(e^{V/E.r} - 1) \quad (1.8.22)$$

Find x_{min}, when E is made equal to the dielectric strength of the resin (10MV/m) and 34KV is applied:-

$$x_{min} = 2{\cdot}25.10^{-3}(e^{34KV/10MV/m.2.25mm)} - 1) \quad (1.8.23)$$

$x_{min} = \underline{7{\cdot}946}$ mm. The resin could break down at this thickness (1.8.24)

It was decided to increase the resin thickness x to 10·75mm, making the b radius = 13mm, which increases the life of the insulation and reduces E:-

$$E = 34.10^3/ (2{\cdot}25.10^{-3}.\ln(13.10^{-3}/2{\cdot}25.10^{-3}) \quad (1.8.25)$$

$$E = \underline{8{\cdot}615.10^6} \text{ V/m.} \quad (1.8.26)$$

The new maximum DC voltage, using (1.8.14):-

$$V_{max} = E.r.\ln(b/a) = 10.10^6.2{\cdot}25.10^{-3}.\ln(13/2{\cdot}25) = \underline{39{\cdot}465} \text{ KV.} \quad (1.8.27)$$

A drawing of the resin moulded core assembly, showing the electrostatic shield is shown in Figure 1.5:

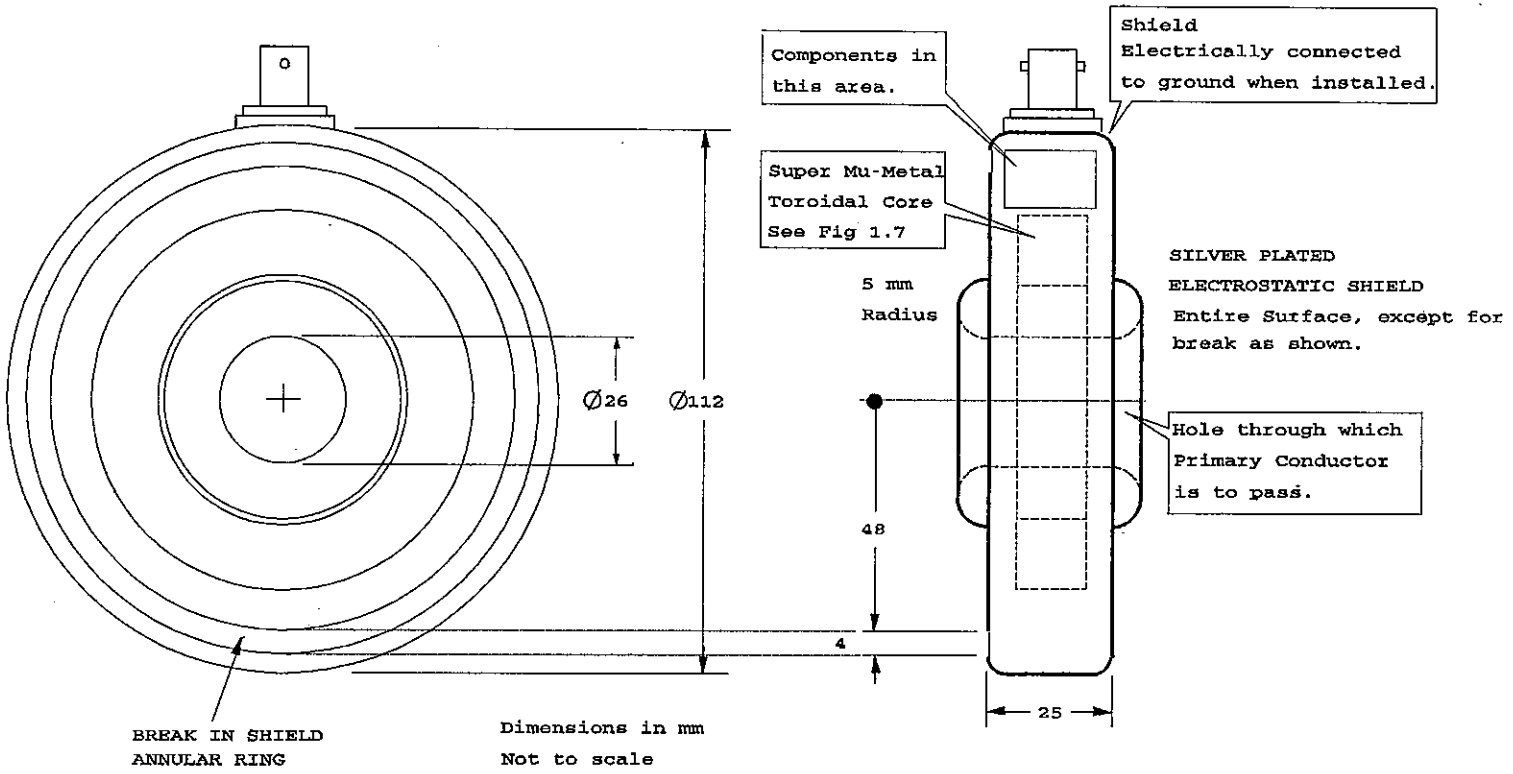


Figure 1.5 : RESIN MOULDED CORE ASSEMBLY

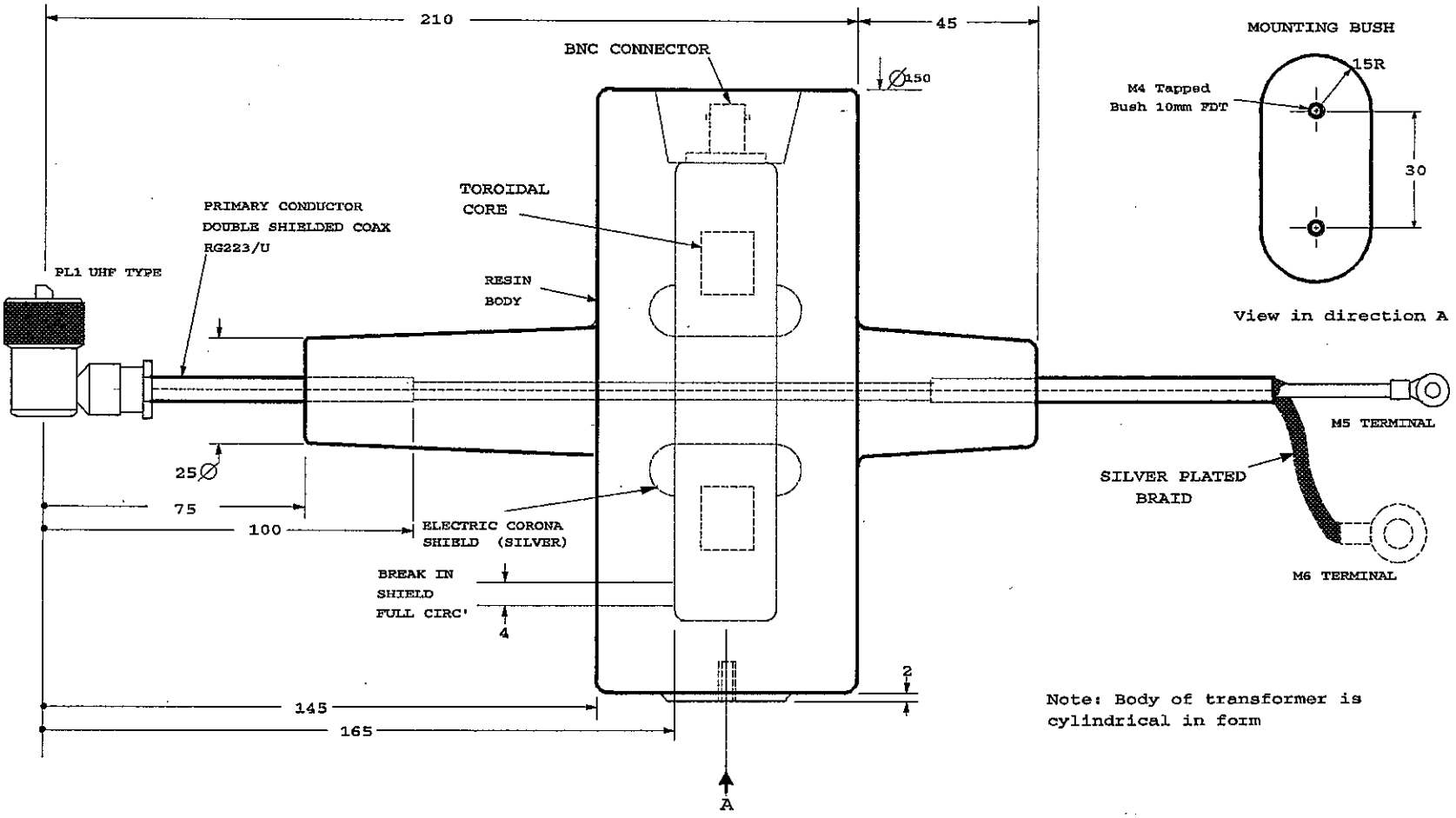


Figure 1.6: MONITORING TRANSFORMER

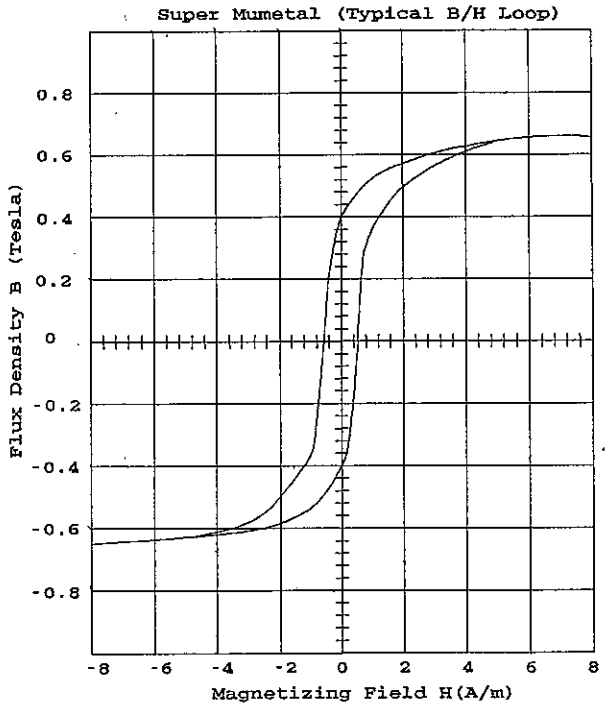
1.9 Core Selection

To produce an accurate representation of the magnetron cathode current pulse, a large super-mumetal tape wound toroidal core was chosen for the following reasons:

a, Toroidal, to achieve negligible leakage inductance and good high frequency response.

b, Large toroidal core; O/D = 79·25 mm, 48·5 mm I/D, was required to allow space for insulation and shielding from the primary coaxial cable (pulsed at -34KV). Also minimises exciting current and yields a more accurate current transformation.

c, Super-mumetal 0·05 mm tape wound, to achieve extremely high permeability (B/H) which gives high magnetizing inductance and low exciting current, giving good low frequency response. The B/H loop performance graph for the core selected is shown in **Figure 1.7:**



Change in Flux Density δB for a 100 Amp Pulse at 3μS PW

From first principles, Induced Emf = $-N.\delta\Phi/\delta t$

From Faradays Law of Electromagnetic Induction:-

$Emf.\delta t = N.\delta\Phi$ Where N is N° Turns (1.9.1)

and as $\Phi = B.A$ Where B is Flux Density (Tesla) (1.9.2)

and A is csa of core (m^2)

$Emf.\delta t = N.A.\delta B$ (1.9.3)

$\delta B = (Emf.\delta t)/N.A$ (1.9.4)

Toroidal core csa = $13{\cdot}64.10^{-3}$m x $15{\cdot}37.10^{-3}$m = $\underline{2{\cdot}0965.10^{-4}}$ m^2

Number of Turns

For an Emf= 20v(for 100 Amp pulse in primary) and a core csa of $2{\cdot}0965.10^{-4}$ m^2

N^0 of turns = 100 and a maximum pulse width of 3μS:-

$\delta B = (20.3.10^{-6})/(100.2{\cdot}0965.10^{-4}) = \underline{2{\cdot}862.10^{-3}}$ Tesla. (1.9.5)

It was decided to settle for 100 turns for convenience, as described in para 1.11.

1.10 Secondary Winding & Components

The current monitoring transformer B13 has been designed to drive a scale sample pulse (1 volt/10 Amp) into a 50 ohm coaxial cable (2m long) to obtain minimum pulse distortion. This was achieved by making the source impedance of B13 o/p 50 ohms and terminating the coaxial cable in 50 ohms on the PBA Regulator.

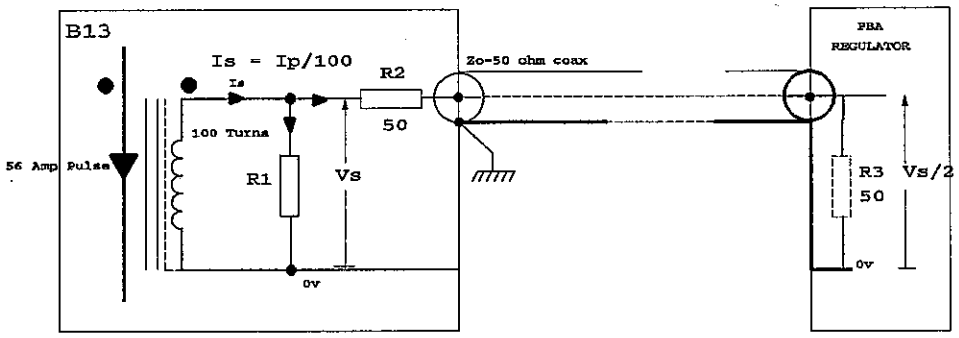


Figure 1.8

1.11 The magnetron is operated with a typical cathode current pulse of 52 Amps peak. The Ipk meter on the transmitter front panel has a FSD of 100 Amps.

For a 52 Amp pulse in the primary, a 5.2 volt pulse is required to be produced across R3/50 ohms on the PBA Regulator. Because of the potential divider R2 & R3, a Vs=10.4v pulse is required to be produced across R1.

The amplitude of the pulse Vs depends on the equivalent resistance (Req) of R1 in parallel with the series R2(50 ohm) and R3(50 ohm) and Is.

Using 100 turns for the secondary winding, equally spaced and tightly wound on the toroidal core, minimises flux leakage, gives good high frequency response and provides an accurate current ratio.

Assuming a perfect transformer with no losses from:-

$$Ip \times Np = Is \times Ns \quad \text{and} \quad Is = \frac{Vs}{R\ eq} \tag{1.11.1}$$

$$Ip \times Np\ (1turn) = \frac{Ns \times Vs}{R\ eq} \tag{1.11.2}$$

$$R\ eq: = \frac{Ns \times Vs}{Ip} \tag{1.11.3}$$

Where Ns = No of Secondary Turns

Ip = Primary Pulse Current

Vs = Secondary Pulse Voltage

$$R\ eq: = \frac{100 \times 10.4}{52} = 20\ ohms \tag{1.11.4}$$

For a primary current of 52 Amps (pulsed),the secondary current:

$$Is = \frac{Ip \times 1}{Ns} = \frac{52}{100} = 0{\cdot}52\ Amps \tag{1.11.5}$$

$$Vs = 0.52 \times 20 = 10.4\ v.$$

The value of R1 required:-

$$R\ eq = \frac{R1 \times (R2+R3)}{R1 + (R2+R3)} \tag{1.11.6}$$

$$R1 = 2000/80 = 25\ ohms \tag{1.11.7}$$

The resistors chosen for R2 and R3 are 50 ohm/ 0·1% / 0·5 Watt RC65 series, for accuracy reasons and for convenience R1 is formed by 2 x 50 ohm resistors in parallel, to give the required 25 ohms.

Two diodes have also been added, D1 and D2(BZT03-C15)zeners, to clamp and provide a bypass path for the core reset current at the end of the pulse. Vs rapidly swings negative when the excitation due to the primary current pulse ceases.

1.12 Wire Gauge (secondary)

Inaccuracy due to secondary winding pulse resistance was reduced by selecting the largest diameter wire that could be evenly wound on the selected core without overlaps (to reduce leakage inductance):

Inside diameter of core: d = 48·514 mm

Inside circumference = π.d = 152·4 mm

Space available/turn = 152·4/100 = 1·52 mm.

An insulated copper winding wire from a range to BS4516:Part 1(Grade 2) was chosen, having a maximum outside diameter of 1·423 mm (+ insulation).

DC resistance 0·01249Ω/m, conductor diameter = 1·32 mm, csa = 1·3685 mm^2.

Core cross section dimensions = 13·64 mm x 15·37 mm.

From the core dimensions the length of the secondary winding wire was assessed to be 60mm/turn x 100 = 6 m.

The DC resistance is: R_{DC} = 0·01249Ω/m x 6m = 0·075 Ω. Negligible compared to Req = 20Ω.

However, the effective pulse resistance is higher:

Calculation of effective pulse resistance due to "skin effect" is complex, so it was decided to follow the recommendations and formula specified in a reference book[4]:

$$R_{eff} = 1{\cdot}58.10^{-7}.(1/\sqrt{\tau}).\ (\text{length of conductor})/(\text{conductor diameter}).$$

Where τ = pulse width (Surveyor is 1·6μs PW).

$$R_{eff} = 1{\cdot}58.10^{-7}.(1/\sqrt{1{\cdot}6.10^{-6}})\ .\ (6000/1.32) = 0{\cdot}568\ \Omega.$$

The pulse resistance is greater than the DC resistance, not negligible however acceptable for the design. Had a smaller diameter wire been selected, the R_{eff} would be greater and thus lead to errors. **Litze wire would reduce the loss.**

1.13 Direction of Secondary Winding

With reference to Figure 1.9: The primary current pulse through the centre of the toroidal core will produce an associated magnetic field flux in the direction shown, in accordance with 'Maxwell's Cork Screw Rule'. The core selected has a very high permeability so most of the flux will be concentrated in the core. The flux will be increasing following the front edge of the pulse. It is required to produce a + ve pulse across the 20 Ω equivalent load resistance, therefore the direction of the winding (100 turns) is decided by LENZ's LAW, in that the induced current in the secondary winding must produce a flux direction to oppose the exciting flux direction in the core. Thus to satisfy the above law, the winding must be as shown in the diagram.

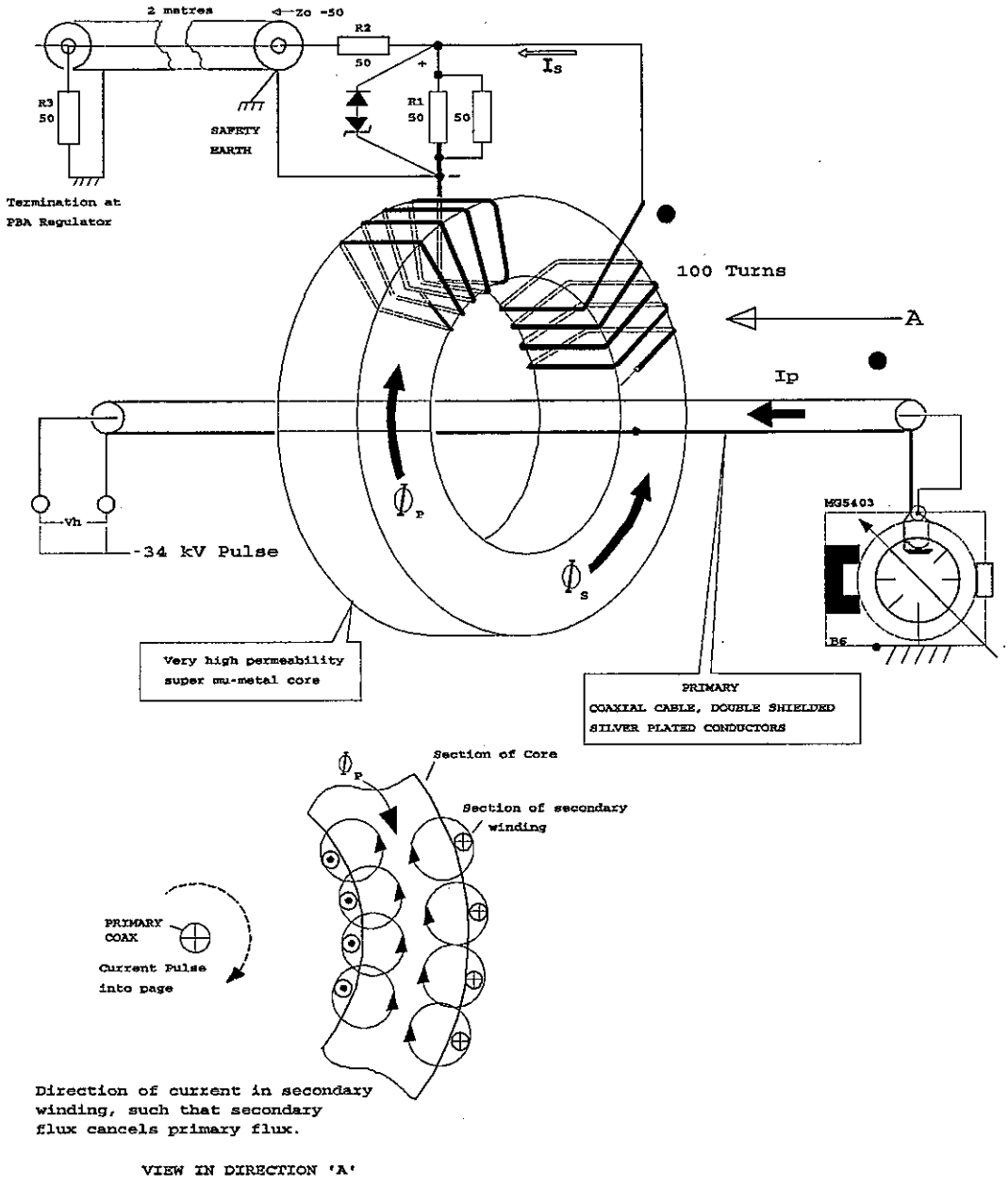


Figure 1.9 : Direction of Secondary Winding

1.14 Magnetron Cathode Heater Controller

The current pulse sample from the Monitoring Transformer B13 is used by the following circuits on the PBA Regulator board:

a, Modulator HT Regulator circuit.

b, The Magnetron Cathode Heater Controller.

c, 50 Ω line driver (pulse monitor buffer).

The pulse is received onto the board by a unity gain voltage follower, input terminated in 50 Ω. This is to ensure that the coaxial line is properly terminated, that the scaling factor of the monitoring is not affected and that there is sufficient pulse current drive.

An AD841J Op-Amp was chosen for the following reasons:-

a, Wide unity gain bandwidth product(40MHz).

b, Fast settling (110 ns to 0·01%).

c, Fast Slew rate (300V/μsec).

d, > 50mA output drive capability.

e, Very low input bias current (3·5μA typical)

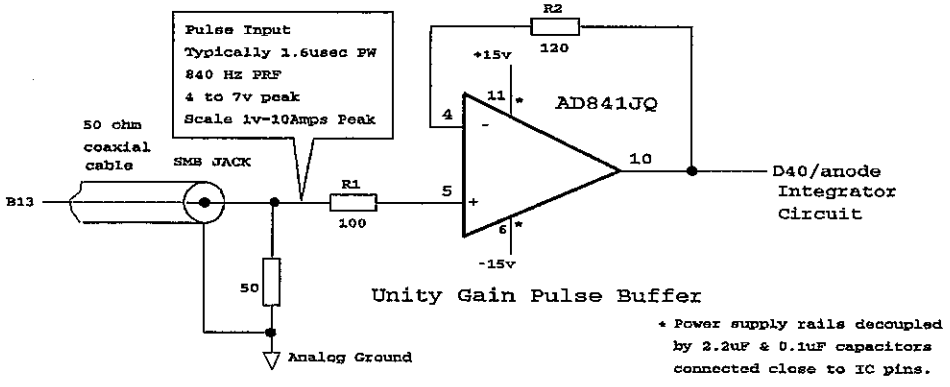


Figure 1.10

The 50Ω coaxial cable from B13 is terminated in a 50Ω resistor. R1 is fitted to provide input protection against transient voltages that exceed the +/-6v maximum differential limit specification of the AD581. R2(120Ω) is fitted to match the -ve input, to reduce errors due to input bias currents. R2 value is set to approximate the equivalent total source resistance of the pulse on the +ve input. The gain error of the voltage follower is equal to 1/Open Loop Gain ie: 1/45000 or to the common mode rejection whichever is less.

1.15 Integrator

To derive a voltage proportional to the mean input power at the magnetron cathode, the scale magnetron cathode current pulse is integrated. A diode, resistor/capacitor integrator was selected for simplicity and low cost:-

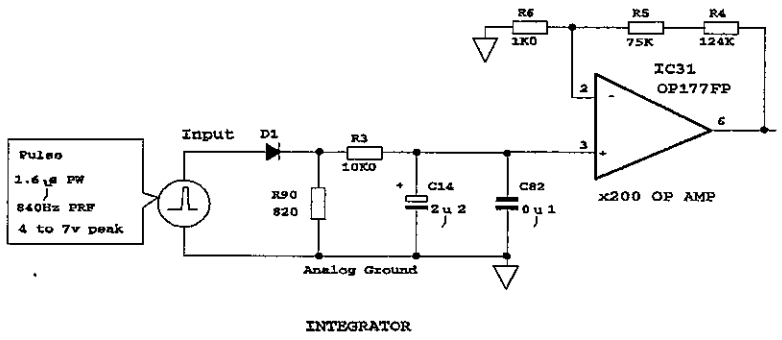


Figure 1.11

The typical dc level across the integrating capacitor, for a 6v (60 Amp) pulse sample is:-

Pulse Duty = Radar PRF x Cathode Current PW (1.15.1)

Pulse Duty = 840 x 1·6. 10^{-6} = 1·344.10^{-3} (1.15.2)

Therefore the integrated output (io) DC level = (6 - 0·6*) x 1·344.10^{-3}

= 7·26 mV approximately. * approximate volt drop across diode. (1.15.3)

The pulse input is passed via D40 and developed across the load R90(820Ω).

Initially capacitors C14//C82 will charge to a voltage v_c via R3(10kΩ) during the 1·6μs pulse duration from 0v:-

$v_c = v_p (1 - e^{-t/C \times R})$ therefore v_{c1} after the 1st pulse:- (1.15.4)

$v_{c1} = 5{\cdot}4 (1 - e^{-1.6us/2.3uF \times 10K}) = \underline{0{\cdot}376}$mV (1.15.5)

Then after the pulse, v_c will discharge via R3 & R90 by a small amount during the period between the end of the 1st pulse and the start of the 2nd pulse:-

For a PRF = 840 Hz

Discharge duration $t = 1/840 - 1{\cdot}6.10^{-6} = \underline{1{\cdot}189}$ ms (1.15.6)

new $v_{c1'}$ after discharge $= v_{c1}(e^{-t/C \times R})$ (1.15.7)

$v_{c1'} = 0{\cdot}376.10^{-3}(e^{-1.189ms/2.23uF \times 10.82K}) = \underline{0{\cdot}358}$ mV (1.15.8)

The 2nd pulse will then charge C14//C82 again via R3/10K to increase the last $v_{c1'}$ level by 0·376mV. Thus the new level $v_{c2} = 0{\cdot}376 + v_{c1'} = \underline{0{\cdot}734}$ mV (1.15.9)

After the 2nd pulse, v_{c2} will again discharge via R3 & R90:-

$v_{c2'} = v_{c2}(e^{-t/C \times R})$ (1.15.10)

$v_{c2'} = v_{c2}(e^{-1.189ms/2.23uF \times 10.82K}) = \underline{0{\cdot}699}$ mV (1.15.11)

And v_{c3} after the 3rd pulse will be $0.376 + v_{c2'} = \underline{1{\cdot}075}$ mV and so on...

Using PSPICE[5] the full charging sequence and final integrated level may be shown. The results of the PSPICE run are included in Appendix 4.

The voltage on C14/C82 will charge up in a 'stair case' manner up to the mean voltage.

The integrator circuit shown in Figure 1.11 only gives accurate integration if the o/p voltage is considerably lower than the i/p voltage, which in this case it is. The very low operating levels of between 0 to 12·5mV need to be amplified to a level suitable for input to an Analog-Digital converter.

1.16 Amplifier, x200 (See Circuit Diagram Figure 1.13/1 & 2)

The output from the integrator is amplified by a precision non-inverting OP AMP stage IC31 having a gain of 200 to increase the voltage range to between 0 to 2·5 volts.

A high precision, low offset drift OP AMP, OP177 was chosen.

Features: Ultra low off-set voltage 20μV (-55degC--125degC). Off-set voltage drift 0·1μV/degC. Open loop gain of 12V/μV maintained over full +/-10v output. CMRR of 130dB min. PSRR of 120dB min. The OP177 is an industry standard for very high precision amplification and is low cost.

The gain is set by resistors R4, R5 & R6. To achieve accuracy and stability of gain, 0·1% 15ppm/degC RC55 type resistors where used.

The Vo/Vin gain = (R4+R5+R6)/R6

Gain = (124K+75K+1K)/1K = 200

Due to the low voltage levels used in the integrator/IC31 amplifier circuit, considerable care was taken with respect to component layout. Each component in the entire circuit was placed to achieve minimum copper track lengths between component pins. With any design, each component has a logical obvious place on a PEC with respect to associated components (Figure 1.12). Careful placement and selection of power supply decoupling capacitors, and use of multilayer PEC with power & ground planes,minimises transients ensuring satisfactory circuit operation.

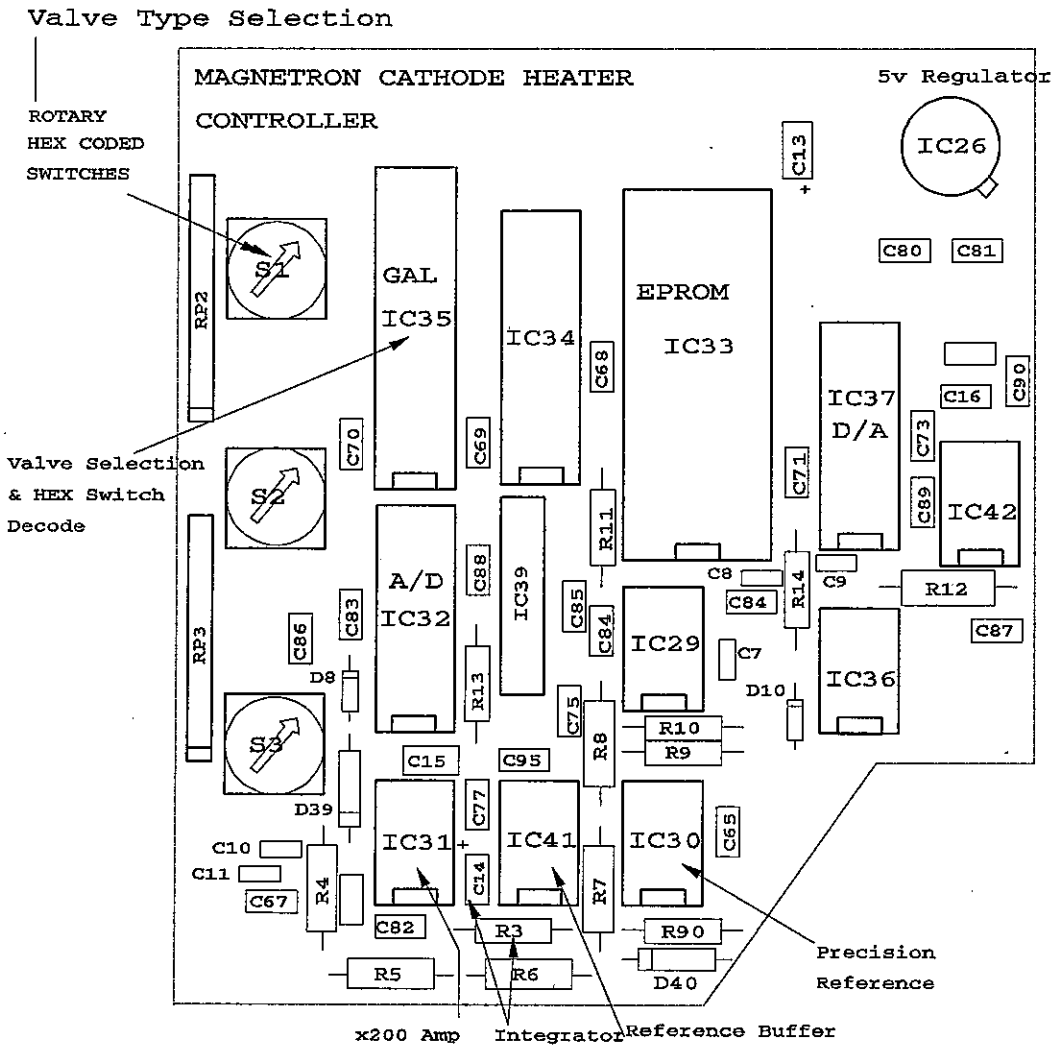
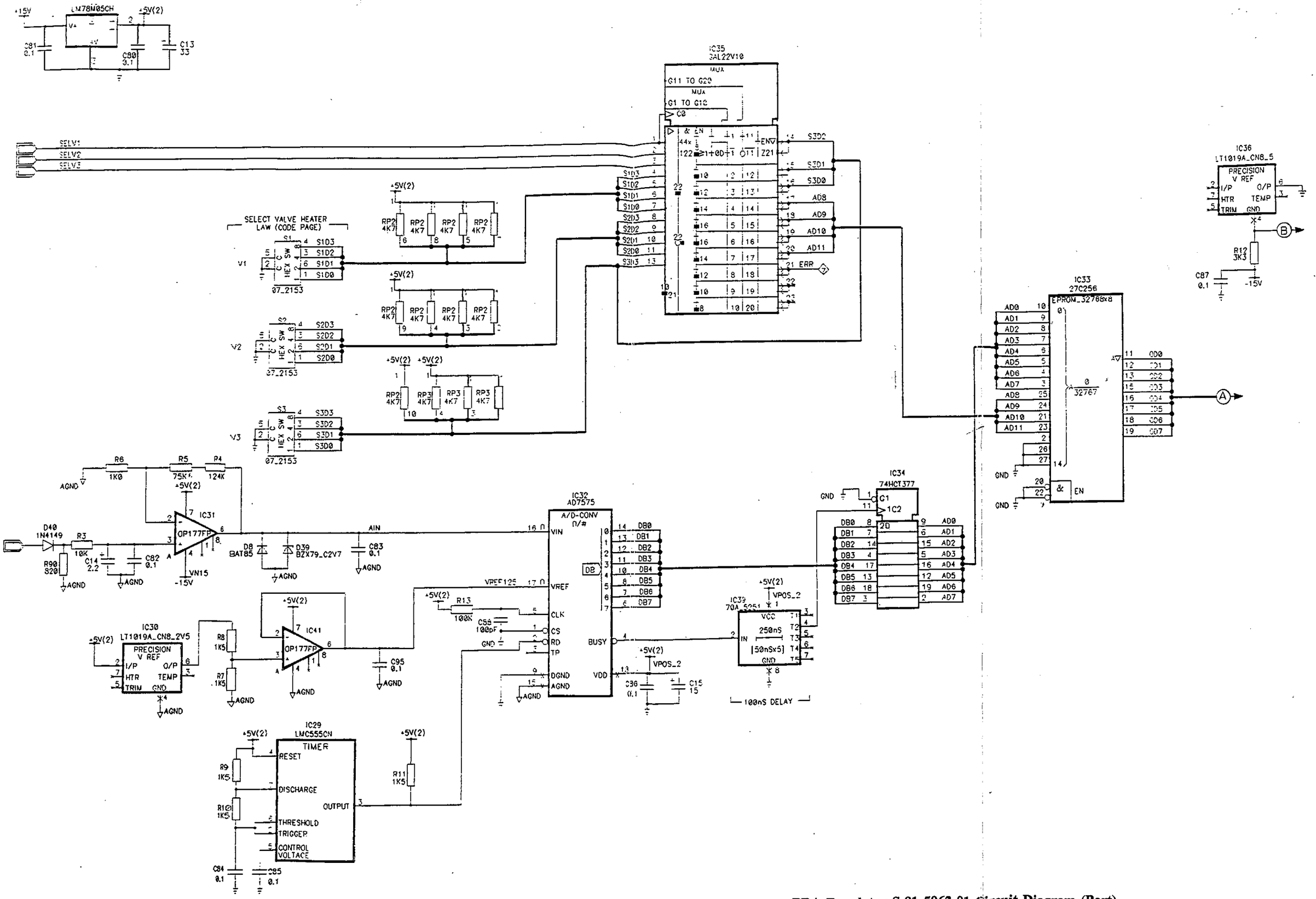
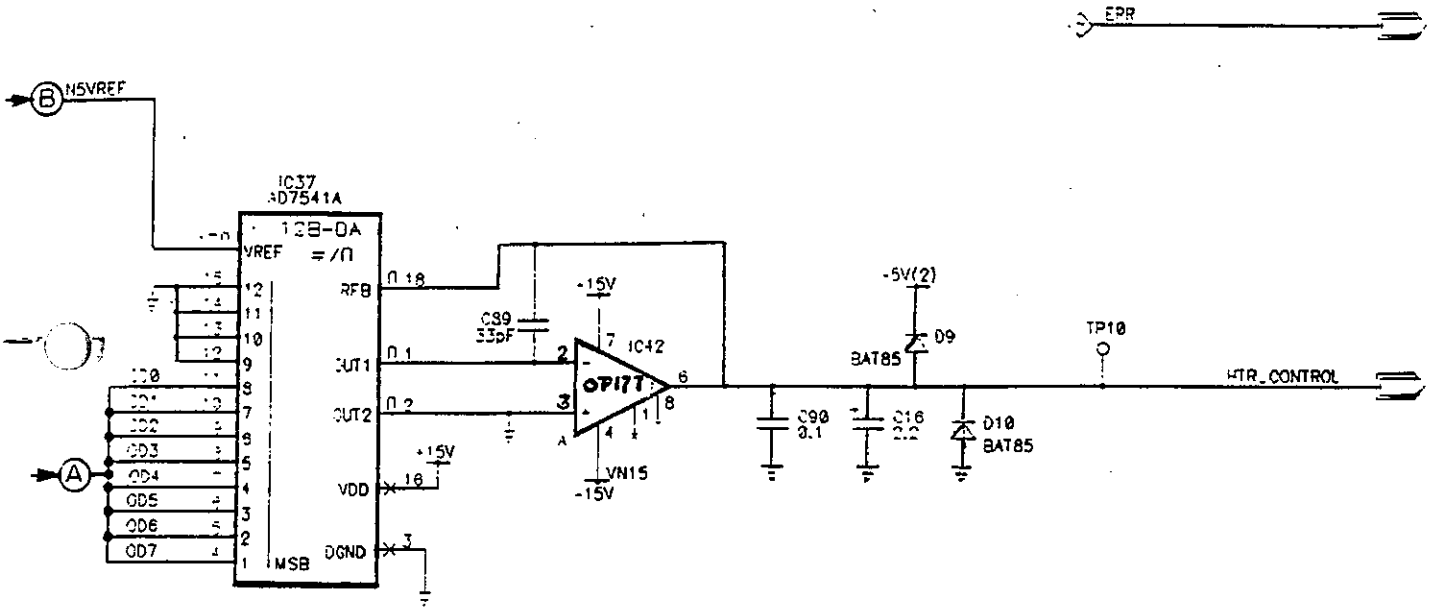


Figure 1.12: Component Layout

Prototype PBA Regulator



PBA Regulator S-81-5062-01 Circuit Diagram (Part)
Magnetron Cathode Heater Controller
Figure 1.18.1



PBA Regulator S-81-5062-01 Circuit Diagram (Part)
Magnetron Cathode Heater Controller
Figure 1.13.2

1.17 Analogue-Digital Converter

An analog to digital converter was required to digitize the integrated level o/p from IC31, which is proportional to mean power into the magnetron cathode.

The slow changing integrated level to be sampled determined that a low cost audio frequency class analogue-digital converter be selected.

An AD7575 successive approximation A-D converter was chosen[6] (cost £7).

The A-D performs a conversion in typically 5μs and is able to digitize signal frequencies up to 50KHz. As the analogue input is an integrated level of 0 to 2.5v , derived from pulses at a PRF of 840Hz, it was decided to configure the device for unipolar operation and sample the analogue input at 3KHz (> than 2 x 840Hz ripple frequency) so that digitization follows the mean level including the ripple component.

Variation of analogue input from 0v to 2·5v, causes the data output of the A-D converter to increases in value from 0 to 255 (ie: 00000000 to 11111111). The 1 LSB resolution of the A-D input is 2·5/256 = 9·765625 mV.

and the 1 LSB resolution of the 'io' level before IC31 (x200) is 12·5/256 = 48·828μV. FSD range of io is 12·5 mV.

The integrated output "io" level range was set at 12·5mV max based heater voltage turndown law requirements for all the magnetrons used in another system (not S2055).

The FSD range input of the A-D converter is set to 2·5v by the 1·25v reference voltage input on pin 17. The reference is derived from a LT1019A 2·5v precision reference IC, output divided by two via R8 & R7 and then buffered by a voltage follower IC41/OP177.

Precise conversion time was not required, so the internal clock oscillator was used, the frequency set to approximately 4MHz by R13/100K & C88/100pF as recommended in the device data sheet. Conversion is done in 10 internal clock cycles. During the conversion the BUSY signal o/p is low, when conversion is complete the BUSY o/p reverts to HIGH. At a maximum time of 80ns after the rising edge of busy, the data o/p from the A-D changes from old data to new data. The low active BUSY signal is delayed by 100ns(IC39), and the delayed rising edge used to clock the data into a register(IC34). The digital delay IC39 is adjustable up to 250ns in 50ns taps and is set to ensure that on the rising edge of delayed BUSY, the o/p data from the A-D is NEW DATA and is settled. In retrospect, the circuit would probably work just as well if old data was sampled. The o/p data of IC34, AD0(lsb) to AD7(msb) forms the lower 8 bits of the address input to the EPROM IC33.

The 8 bit system chosen provides an o/p 1 LSB resolution of 5/256 = 19·53 mV. The 0 to 5 volt o/p HTR PSU control voltage controls a 0 to 80 volt power supply and therefore the control scale factor is 80/5=16 o/p volts per control volt. Therefore the 1 LSB resolution in heater voltage is 16 x 19·53 mV = 0·3125v. The heater voltage may be set to within 0·3125v which was considered more than adequate by the designers of the magnetron.

1.18 Code Page Addressing

To provide Heater Voltage turndown profiles of up to 15 magnetrons (9 in use to date), the EPROM IC33 was mapped into 16 Code Pages; blocks of 256 addresses.

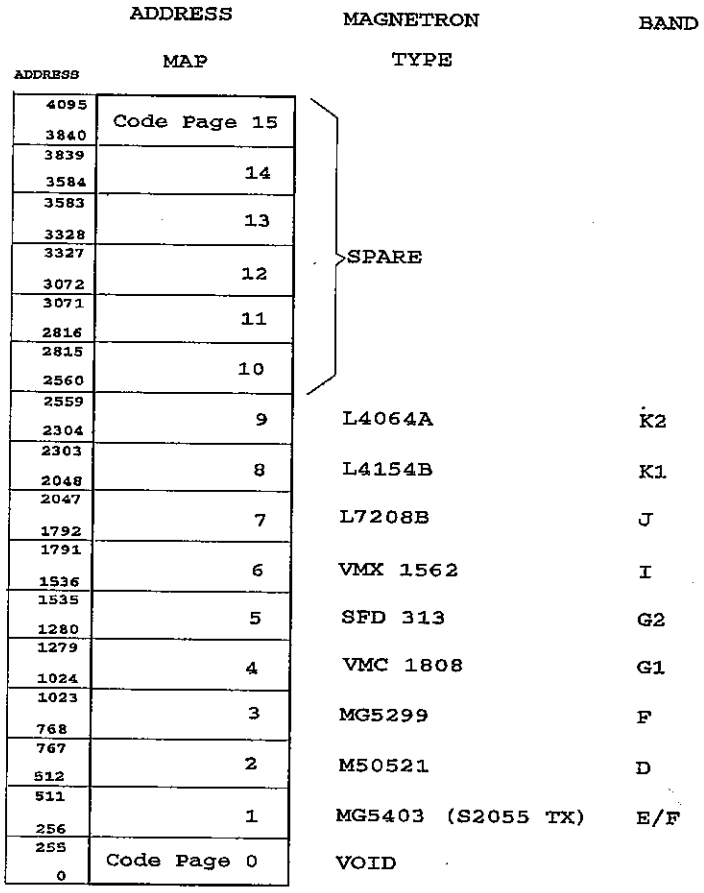


Figure 1.14

Code Pages 0 to 15 are selected by using the 4 most significant bit inputs (AD8 to AD11 to the EPROM. Code Page 0 is reserved, programmed with all zero's, and is selected should an invalid selection be attempted. Code Page 1 is selected by having AD11--AD8 = 0001, which adds 256 onto the value of data into AD7--AD0.

1.19 Code Page Selection

In order to have a selection of three magnetrons, with any of up to 15 magnetron types for each selection, it was decided to use three HEX rotary switches S1 (V1), S2 (V2) & S3 (V3) to select the required magnetron type.

The HEX switches produce a 4 Bit **low active** binary coded output,

ie, Code Page 1 = 1110(lsb), therefore requiring pull up resistors on each output.

The magnetron select inputs SELV1, SELV2 & SELV3 are **low active**, however are not binary coded, and are used to select one of the HEX switches.

To achieve this, a 4 bit 3 way multiplexer was designed into a programmable GAL22V10 device. The GAL device produces the **high active** (selected) 4 bit code page address and incorrect selection monitoring to provide an error (err) output. The err output is used to inhibit transmission if selection is invalid.

The source file for IC35 was compiled using ABEL V4 software, and is included in Appendix 5.5.

The **"inputs** & **"outputs** sections allocates names to the IC pin numbers. It is important that the architecture of the programmable device selected is checked when selecting inputs and outputs, and also to ensure that the IC has the necessary functions.

The low active select inputs SELV1, SELV2 & SELV3 are input on pins 1,2 & 3 respectively. The inputs from the HEX switches are labelled (A3--A0), (B3--B0) & (D3--D0). The letter C is reserved in ABEL.

"equations section.

The high active 4 bit o/p that will be the code page address is declared as (Q3--Q0). The GAL pins which are to be used as outputs have to be "output enabled". This is accomplished by the statements: [Q0] .oe=TRUE etc.

A 3 way, 4 bit multiplexer with logic inversion is achieved by using 4 sets of combinatorial statements.

In the ABEL language the following symbols are used to denote logical functions:

& AND

OR

! (signal name) LOW or Not Valid if signal is high active.
absence of "!" before a signal name indicates that the signal is high.

= Signal name to the left of "=" is true if expression on the right of "=" is valid.

:= Same as = , however becomes true on the next clock input, which would be input on pin 1 of the device if used.

; terminates a statement or set of statements.

```
Example:    Q0    = !A0 & !SELV1 & SELV2 & SELV3
                  # !B0 & SELV1 & !SELV2 & SELV3
                  # !D0 & SELV1 & SELV2 & !SELV3;
```

In the above statement, Q0 will be the inverse of A0 "OR" B0 "OR" D0, depending on the status of the select inputs SELV1, SELV2 and SELV3.

For example: Q0 will be the inverse of A0 if SELV1 is LOW AND SELV2 AND SELV3 are high.

The other 3 bits Q1, Q2, and Q3 are produced in the same way.

The valve select inputs are checked for being a valid combination by the statement set:

```
!ERR  =!SELV1 & SELV2 & SELV3
      # SELV1 & !SELV2 & SELV3
      # SELV1 & SELV2 & !SELV3;
```

test_vector section

Sets of test vectors are written to check output states with variation of input states. See Appendix 5 listings.

1.20 Whilst the design of the electronic hardware was straight forward, there remained the problem of generating the 256 element data profiles relating to the heater voltage turndown laws for each valve. Manually calculating 256 sets of data for each of the 15 Code Pages (profiles) would be very tedious.

To provide a fast means of editing and programming the profile data, a computer program was written (in "C" compiled into IBM 80x86 code). The program is menu driven and allows anyone to easily edit the profile defining data for each magnetron code page. The input data is in the form of 10 pairs of data describing a profile, the computer program calculates the heater voltage control data in-between and including the 10 pairs of input data to give 256 elements of data.

The output from the program is an RTT HEX ASCII formatted file compiled in a form ready to down-load into a device programmer and register with the company firmware registration department.

1.21 The heater profiles are prepared in the form of sets of data, derived from the valve manufacturers data sheets and knowledge of:

a,The output voltage/control voltage ratio of the heater power supply (A8) to be used. An 80v/6 Amp SMPS having a 0 to 5v control voltage was used.

b,The scaling factor ratio of the cathode current monitoring transformer (B13).

c,The voltage drops through the bi-filar secondary windings of the HV pulse transformer. The voltage drop when the power supply is set to 72v is 2v giving the required 70v at the magnetron.

d, The manufacturers recommended heater turn down law.

e, The cathode (PW x PRF) duty.

The sets of data defining the profiles, are entered into the computer program as initialised variables 'vcmn' & 'iomn.' where 'm' is the code page N° and n is used to identify each pair of vc io values:

MG5403 (S2055) Code Page 1 example:

Mag'Heater PSU Voltage	Control Voltage(vc)		Integrated Output(io)	
72.00v	vc11	4.500v	io11	0.000mv
64.00v	vc12	4.000v	io12	0.700mv
56.40v	vc13	3.525v	io13	1.500mv
48.64v	vc14	3.040v	io14	2.250mv
40.80v	vc15	2.550v	io15	3.000mv
33.12v	vc16	2.070v	io16	3.750mv
25.60v	vc17	1.600v	io17	4.500mv
17.60v	vc18	1.100v	io18	5.250mv
9.92v	vc19	0.620v	io19	6.000mv
2.00v	vc110	0.125v	io110	6.750mv

Each valve is assigned a similar set of data, vc2n io2n...etc.

The heater turn-down law for the set of data above is shown on a graph in Figure 1.15.

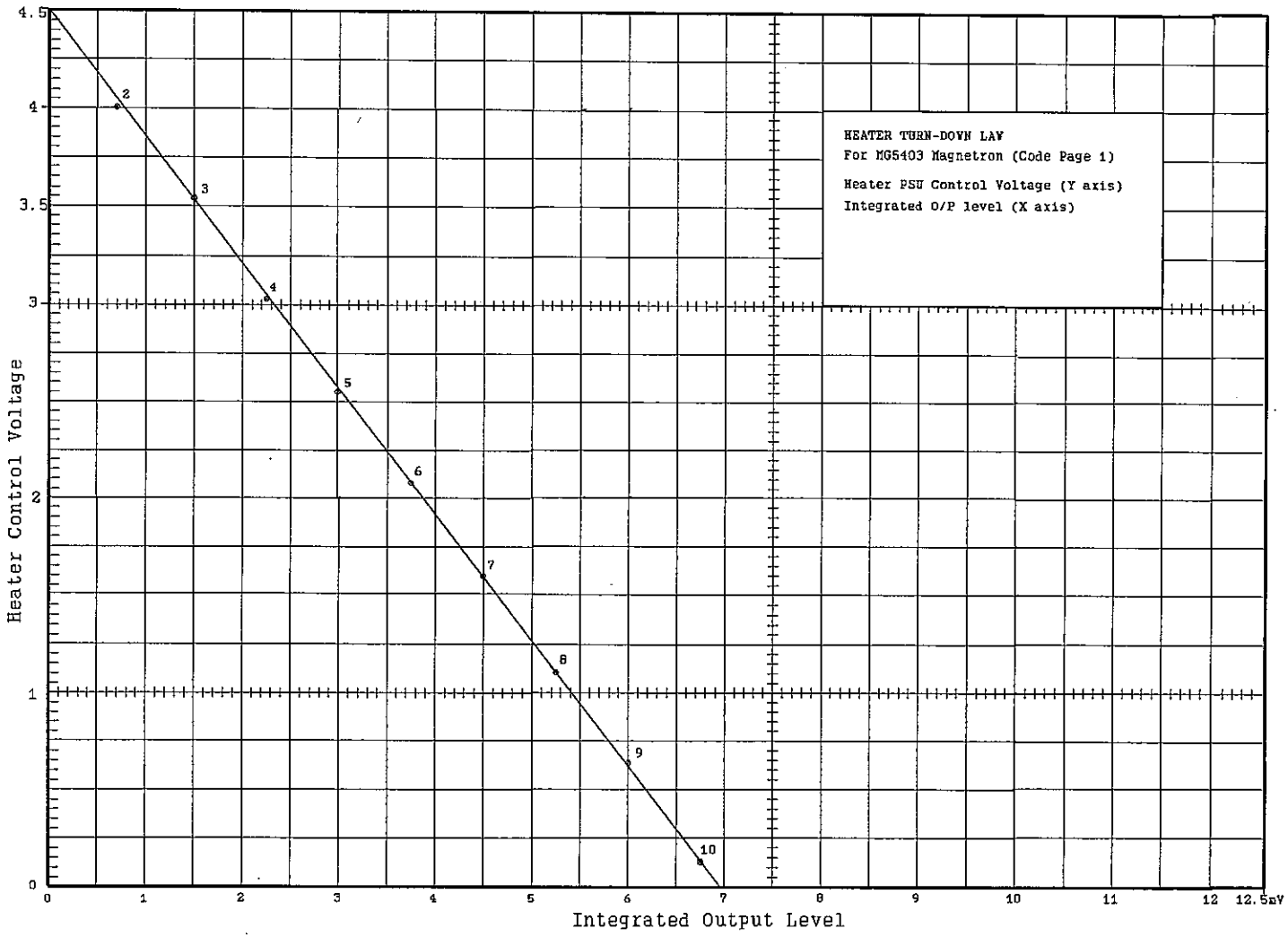

HEATER TURN-DOWN LAW
For MG5403 Magnetron (Code Page 1)
Heater PSU Control Voltage (Y axis)
Integrated O/P level (X axis)
Heater Control Voltage
Integrated Output Level
4.5
4
3.5
3
2
1
0
0
1
2
3
4
5
6
7
8
9
10
11
12
12.5mV
2
3
4
5
6
7
8
9
10

Figure 1.15

The data set and associated heater turn-down law graph shown above are optimised for the MG5403 magnetron in the S2055 transmitter. The performance of the magnetron in the S2055 is different from that obtained with the magnetron fitted into the manufacturers modulator test rig, such that the data set had to be optimised to achieve low jitter.

1.22 The magnetron may be tuned to transmit on one of 6 frequencies, set by the 6 channel STALO. At the frequency selected the magnetron cathode peak current is set to produce 1 MW peak RF o/p.

The efficiency of the magnetron varies across the band 2.7 GHz to 2.9 GHz, typically 48% to 65%. Therefore, to achieve 1 MW peak RF o/p the magnetron peak cathode current needs to be varied and so the mean input power to the magnetron varies. It follows that in order to have the cathode at the optimum temperature to achieve low jitter, the heater voltage also needs to be varied.

It is possible to get the magnetron to operate with a fixed nominal heater voltage however optimum low jitter performance will not be achieved.

1.23 To evaluate the variation of "integrated output" level (proportional to mean input power to the magnetron) with variation in magnetron efficiency:

The pulse duty is set at 0.001344.

1. For the 48% efficiency case

RF o/p set to 1 MW peak (1344 W mean).

∴ Input peak power required = $1.10^6/0{\cdot}48$ = 2·083 MW peak.

Assuming that the cathode voltage is relatively constant at 34 kV:

Peak cathode current = $2{\cdot}083.10^6/34.10^3$ = 61·27 Amps peak.

B13 produces a 6·127 volt cathode current pulse sample.

Approximate integrated output level (io):

(6·127 - 0·6).0·001344 = 7·43 mV.

2. For the 65% efficiency case

RF o/p set to 1 MW peak (1344 W mean).

∴ Input peak power required = $1.10^6/0{\cdot}65$ = 1·538 MW peak.

Peak cathode current = $1{\cdot}538.10^6/34.10^3$ = 45·24 Amps peak.

B13 produces a 4·524 volt cathode current pulse sample.

Approximate integrated output level (io):

(4·524 - 0·6).0·001344 = 5·27 mV.

For the variations in efficiency of the magnetron the io level varies between: 7·43 mV and 5·27 mV.

1.24 Referring to Figure 1.14, when the S2055 is transmitting, the MCHC will operating in the region between the io limits calculated above as the efficiency of the magnetron varies.

From the graph the variation in magnetron heater power supply control voltage varies between 1·1v and 0v.

Using the heater power supply o/p voltage/input control voltage ratio 16, the variation in heater power supply voltage is (1·1.16) = 17·6v to 0v.

1.25 Optimisation of Profiles

In the region of the profile in which the MCHC is operated, the profile is optimised, such that at all duties and cathode peak currents to achieve 1 MW RF o/p, the Standard Deviation of the jitter is minimised.

To determine the "vc" (heater power supply control voltage) levels within the region of operation, the transmitter was operated at a number of points. At each point, the magnetron was allowed to thermally stabilize (45 minutes typically) and the jitter performance assessed using the method described in appendix 3.

At each point the magnetron heater voltage was manually adjusted very slowly, to find the ideal level of vc that yielded the lowest jitter standard deviation.

Using the computer program described to rapidly modify the heater turndown profile, the EPROM was reprogrammed, fitted into the MCHC. The transmitter was operated again at a number of duties within the region of operation to verify that the MCHC was controlling the heater as required to yield lowest jitter.

It was proved using a number of magnetrons that the profile need not be adjusted for each magnetron.

1.26 The profile for the MG5403 turned out to be a simple straight line law as shown in Figure 1.15. Other magnetron profiles in code pages 2 to 9 were not straight profiles.

The set of 10 data pairs for code page 1 were set at equal points across the profile as shown in Figure 1.15. However should it so be desired to achieve increased accuracy of profiling over the region of normal operation, the first two pairs of data points could be used to define the profile between the non transmitting vc level and the lower limit of the operating region. The other 8 pairs of data points then used to tailor the profile in the normal operating region.

The computer program calculates the "vc" data assuming a y= -mx +c law (m=gradient,c=constant) between each pair of data in the set. Beyond the 10th data pair the program calculates the data assuming the previous law until vc =0v.

The computer program also provides options to print out, for each code page, the actual "io","io x 200" and "vc" programmed into each address in the EPROM also the m and c values defining the laws between each pair of vc/io input data.

The print facilities were designed in as a development tool to enable an engineer to have rapid visibility of the profiles.

1.27 Within the normal operating region there is a point where the magnetron heater voltage is reduced to 0v. Operating the magnetron at peak cathode current levels and duties above the vc = 0v point, makes the cathode temperature entirely dependant on back-bombardment power alone. A point is reached where the jitter performance starts to degrade due to excessive cathode temperature, as such valve life starts to be reduced. The MCHC design should extend valve life.

1.28 Digital-Analogue Converter

For reasons of low cost and availability, an industry standard AD7541AJN device was chosen for IC37, to convert the 8 bit "vc" data output from the EPROM IC33. The AD7541AJN device is a 12 bit monolithic multiplying DAC. The four lowest significant bits are not used and are connected to ground.

The requirement for 8 bit binary input and a 0v to +5vdc o/p led to the "Unipolar Binary Operation" configuration as recommended in the applications notes for the device in the Analog Devices data book[7].

An OP177FP was chosen to convert the D-A Converter $I_{OUT\,1}$ current into a 0 to +5v HTR CONTROL voltage which is used to control the magnetron heater power supply. The low SR (slew rate) of the OP177FP, typically 0·3 V/μs was more appropriate for the MCHC design rather than an AD544L(SR 13V/μs) suggested in the data book application notes. The low V_{OS} (input offset voltage) of typically 10μV, long term V_{OS} stability of 0·3μ/Month, TCV_{OS}(offset voltage drift with temperature) of 0·1μV/°C MAX and low I_B (input bias current) 1·2 nA gave a high accuracy solution requiring no adjustment. Also the OP177FP is used elsewhere in the circuit and therefore no need to add another OP-AMP type to the inventory.

The -5v reference for the D-A converter is provided by an LT1019A-CN8-5 precision reference, connected to give -5v.

CHAPTER 2

Modulator H.T. Stabilizer §

Design Study

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CHAPTER 2

Modulator H.T. Stabilizer †

Design Study

2.1 Introduction

To achieve good overall system Moving Target Indication (MTI) Improvement Factor performance, it is essential that the radar transmitter pulsed RF output has high frequency and amplitude stability.

The Coaxial Magnetron selected for the S2055 transmitter offers high frequency stability due to a high "Q" outer stabilizing coaxial cavity. However variation in the peak amplitude of the voltage applied to the cathode and subsequent variation in the cathode current from pulse to pulse, causes variation in the frequency of oscillation. Therefore, to obtain good stability, on a pulse to pulse basis, it is necessary for the modulator primary energy storage capacitors to be charged to the same voltage before each pulse.

The Modulator HT Stabilizer controls and stabilizes the charging of the modulator capacitors before each modulator discharge, and stabilises the voltage irrespective of the use of Pulse Repetition Frequency (PRF) STAGGER (6 period +/-14%).

2.2 Design Aim

The initial design aim was to achieve < 350Hz frequency stability, which yields a Stability Limitation Factor of:

$I_{\Delta f} = 20\text{Log}(1/\pi.\Delta f.\tau)\text{dB}$. (or = $10\text{Log}(\pi.\Delta f.\tau)^{-2}$ dB [Skolnik1]) (2.2.1)

where τ is the RF Pulse width and Δf is the Standard Deviation(σ) of the pulse to pulse frequency.

$$I_{\Delta f} = 20\text{Log}(1/\pi.350.1{\cdot}6.10^{-6}) = 55{\cdot}1 \text{ dB} \quad (2.2.2)$$

Assuming that the variation of frequency about the mean frequency of transmission is random and thus has a Normal or Gaussian distribution, 99.7% of frequency samples will occur between the limits of the mean frequency +/- 3.σ (3 sigma limits). Therefore the peak to peak frequency variation = 6 x 350 = 2100 Hz. Using the 15kHz/Amp pushing figure, defined on the valve data sheet:

The peak to peak $\Delta I_{a\,max} = 2100/15.10^3 \times 1$ Amp = 0·14 Amps (2.2.3)

where ΔI_a is the variation in magnetron cathode current.

2.3

With the aid of the magnetron cathode current monitoring transformer B13 , detailed in Chapter 1, it was possible to measure the:

Δ Modulator Primary HT (Vp) versus ΔI_a , sensitivity of the Solid State Modulator.

A variation of 10 volts about a typical -350v modulator HT level causes a variation of 5·2 amps in the magnetron cathode peak current.

$\therefore$ Sensitivity Figure S = 0·52 Amps/Vp volt. (2.3.1)

2.4 Using the $\Delta I_{a\,max}$ value derived above and the Sensitivity Figure the variation in modulator primary voltage to achieve 0·14 Amp change in the magnetron cathode current is determined:

$$\Delta Vp = \Delta I_{a\,max} / S \qquad (2.4.1)$$

$$\Delta Vp = 0{\cdot}14 \ / 0{\cdot}52 = \underline{269}\ \text{mV (peak to peak).} \qquad (2.4.2)$$

The MTI signal processor used performs 4 pulse cancellation , therefore it is reasonable to aim for a ΔVp of $<$ 269 mV pk-pk in 350v(nom) over groups of 4 PRI intervals.

2.5 Background

The proposed idea † for Modulator HT Stabilization required an inductor and MOSFET switches to be inserted in series, between the Modulator HT Power Supply and the Solid State Modulator, together with associated control circuits as shown in Figure 2.1:-

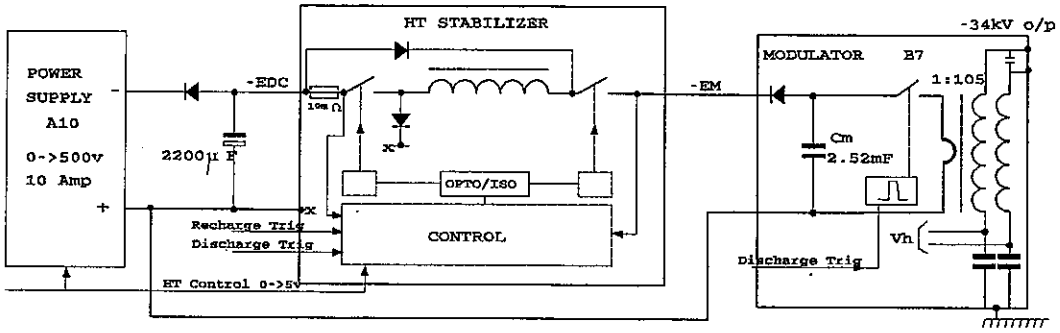


Figure 2.1

The concept is that the charge lost in "Cm" due to a modulator pulse is replaced during a time interval before the next pulse. The start of a charge is initiated by a Recharge Trigger, which causes the MOSFET switches either side of the inductor to close. The Recharge Trigger is set at a fixed interval before the Discharge Trigger, to ensure that the time delay between the modulator voltage reaching the required level and the point at which the modulator is discharged is constant, even with staggered PRF operation. When the MOSFET's switch ON, a step voltage difference (EDC - EM) is placed across the inductor and the current through L1[¶] into the modulator Cm capacitance starts to increase in a uniform ramp.

Note: The level -EM, and thus the voltage drop across the stabilizer is set by a ratio circuit and comparator on the stabilizer control board which will be described in detail later. Both -EDC and -EM will vary together as controlled by circuits on the PBA Regulator, which maintains the peak magnetron cathode current constant The PBA Regulator control loop has a slow response, 2 to 3 seconds.

The self induced emf generated across the inductor is related to the value of inductance L, the charge time t and the increasing current I :-

Induced EMF 'e'(in the inductor) is proportional to $-\delta I/\delta t$

or $e = -\text{constant}.\ \delta I/\delta t$

The constant in this case is the inductors "Inductance" L

Hence $e = -L.\delta I/\delta t$

or $L = e/\delta I.\delta t$ ignoring the "-" which is due to Lenz's Law.

In Fig 2.1 $\delta i_L = V_L.\delta t/L$ or $V_L = L.\delta i/\delta t$

Where δi is the change in charge current, and δt is the charge time.

Design of the proto-type inductor[1]

Assumed the use of a 450v power supply and set V_L to 50 volts. The value of inductance was calculated to allow operation at PRF, Duty & Stagger requirements of 1500Hz,0·0014 & +/- 14% respectively: PRF of 1500 Hz = PRI of 666μs

14% of 666μs = 666μs x 0·14 = 93·4μs

minimum pulse repetition interval = 572μs

Choosing a recharge duty of 0·76

Giving a charge time of 666μs x 0·76 = 506μs.

A preliminary mean modulator current was derived at 10.3 Amps.

The peak inductor current was calculated:

I_{pk} = 2 x I_{mean}/Recharge Duty

I_{pk} = 2 x 10·3/0·76 = 27·1 Amps

And using: L = V.t/I

The required inductor value was calculated:

L = 50 x 506.10^{-6}/27·1 = 933 μH.

The inductor used for the prototype was based on the design proposed, and had a value of 1·1mH.

The charge is terminated when the modulator voltage has reached the level required, monitored at the o/p of the stabilizer; the two MOSFET switches are opened isolating the modulator from the HT Stabilizer and the modulator power supply. The energy stored in inductor L during the charge time is recycled back into the 2200μF input capacitor when the MOSFETS are switched OFF via D1 and D2.

The current in series with L and the power MOSFET's is monitored, and should the current exceed a safe value, the MOSFET's are switched OFF. This facility is used during the initial charging up of the modulator Cm capacitors from 0v, where Cm is charged in a number of charge cycles.

The modulator capacitor "Cm" consists of 21 identical capacitor/FET switch modules configured in parallel. Each module has 120μF of low inductance capacitance, giving a total storage capacitance of 2·52mF.

Each module also has a hold off diode, to prevent energy discharging back via the HT Stabilizer. **End of Background**

2.6 To Derive the Modulator Charge Current

To derive the actual modulator charge current delivered to the modulator by the stabilizer before each pulse, we start at the magnetron and work back:-

The manufacturers of the valve have indicated that the typical efficiency of the valve as 56%, however the efficiency does vary from one valve to another and when tuned across the band (2·7GHz - 2·9GHz).

The peak output power required is 1 MW therefore:-

Peak I/P Power = $1.10^6/0.56$ = 1·79 MW (2.6.1)

The difference between the valve input power and the RF output power is used to heat the cathode surface and lost in the form of heat which is removed by forced air cooling. In this case:

Mean Power lost = (mean input power)-(mean RF o/p power)

Mean Power lost = $(1{\cdot}79.10^6.0{\cdot}001344)-(1{\cdot}0.10^6.0{\cdot}001344)$ = 1062 Watts.

2.7 From the manufacturers data, the peak cathode voltage during oscillation is 34kV, therefore the required peak cathode current is:-

Ipk = Peak Power input/Peak Cathode Voltage

Ipk = $1{\cdot}79.10^6 / 34.10^3$ = 52·65 Amps (peak). (2.7.1)

2.8 The turns ratio of the HV Pulse Transformer delivering the 34kV pulse to the magnetron cathode is 1:105. Therefore, the peak pulse transformer primary current is: 105 x 52·65 = 5528 Amps (2.8.1)

Mean primary current=5528 x 0·001344= 7·43 Amps.Neglecting the efficiency of the modulator.

2.9 The peak voltage pulse required across the pulse transformer primary is:

34kV/105 = 323·8 volts. (2.9.1)

2.10 Due to the finite R_{dsON} resistance of the MOSFET's used in the modulator, a voltage will be dropped:-

There are 6 MOSFET switches used in a parallel configuration in each of the 21 modules. The R_{dsON} resistance of each FET is 0·4 ohms for the APT6040 devices used. Therefore, the effective ON resistance of the switch in each module is:

$0.4 / 6 = \underline{0{\cdot}06'}$ ohms. (2.10.1)

The pulsed current from each module is: $5516/21 = \underline{262{\cdot}7}$ Amps(pulsed), (2.10.2)

therefore, the voltage dropped due to MOSFET R_{dsON} is:

$V = 262{\cdot}7 \times 0{\cdot}06' = \underline{17{\cdot}5}$ volts. (2.10.3)

Therefore the modulator capacitors are required to charge to 323·8 + 17·5 volts

$= \underline{341{\cdot}8}$ v after each pulse. (2.10.4)

This theoretical value is similar to the actual value measured on the reference transmitter.

2.11 The change in the modulator voltage Δv after each pulse is determined:-

The charge ΔQ input to the pulse transformer primary/pulse:-

ΔQ = Peak Pulse Transformer Primary Current(2.8.1) x Pulse Width

$= 5516 \times 1{\cdot}6\mu s = \underline{8{\cdot}8256.10^{-3}}$ Coulombs (2.11.1)

and using:- Charge Q = Capacitance C x Voltage V

$\Delta v = \Delta Q / C_m$ Where C_m =Total modulator primary capacitance

$\Delta v = 8{\cdot}8256.10^{-3} / 2{\cdot}52.\ 10^{-3}$ $\Delta v = \underline{3{\cdot}5}$ volts (2.11.2)

2.12 Modulator HT Power Supply

For reasons of power supply reliability, lower ripple and increased VA rating(5KW), it was decided to use a 500 Volt/10 Amp, 3 Phase I/P, Thyristor controlled Linear Power Supply, rather than the 450 Volt Switch Mode supply suggested. The supply chosen was the same type of supply used on a previous version of the transmitter.

The benefits include proven design & commonality of spares.

To reduce the current output from the power supply for a given power output, it was decided to increase the voltage difference across the HT Stabilizer from the 50v proposed, to 80v. The output voltage from the power supply would be increased to: 80v + 341·8 = 421·8 Volt (Note 341·8v predicted in Para 2.10).

2.13 The actual mean current into the modulator from the stabilizer will be higher than the 7·4 Amps mean predicted in Para 2.8, due to various losses in the modulator which have not been taken into account.

The designer of the modulator has indicated that the typical modulator efficiency is in the order of 87%.

The mean power to be supplied by the modulator was predicted to be:

$1{\cdot}79.10^6$ x 0·001344 = 2406 Watts mean in Para 2.6.

Therefore the predicted input power at 87% efficiency: 1/0·87 x 2406 =2765·5 **W.**

Hence, with a predicted 341·8v modulator primary HT voltage, the revised modulator mean input current is: 2765·5/341·8 = 8·1 Amps. (2.13.1)

2.14 The Surveyor system PRF is 840 Hz (PRI = 1·19 ms).

It was decided to charge the modulator in approximately 600μs, and the signal processing engineer was instructed to set the timing of the recharge trigger at 820μs before discharging the modulator, leaving 220μs to allow for extended charge time should lower efficiency magnetrons be fitted.

Therefore the recharge duty is 600μs/1·19ms = 0·5 (2.14.1)

The charge current (ramp) will have a peak value of:-

Ipk = (2 x I_{mean})/ recharge duty (2.14.2)

Ipk = (2.8·1)/0·5 = 32·4 Amps. (2.14.3)

2.15 Using:- $v = L.\delta i/\delta t$

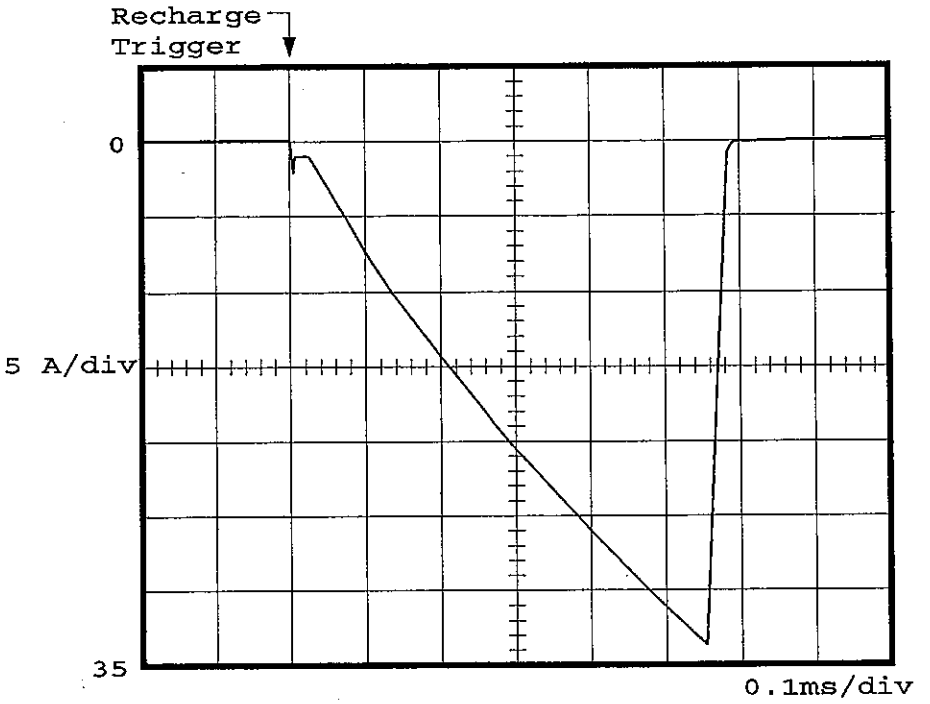
Estimated inductor value required: $L = (v.\delta t)/\delta i$ (2.15.1)

$L = (80.600.10^{-6})/32{\cdot}4$ (2.15.2)

L = 1.48 mH (2.15.3)

The design of the inductor has since been carried out by a specialist sub contract manufacturer, to improve the design: reducing losses, resulting in cooler operation, reduced physical size and cost. The production version is approximately 60% of the size of the prototype.

Figure 2.2 shows a typical charge current waveform monitored at the output of the HT Stabilizer, transmitter o/p power set to 1 MW pk.



Typical Modulator Charge Current Waveform

Figure 2.2: Monitored in the -EM o/p of HT Stabilizer,waveform not idealised.

2.16 Selection of MOSFETS for TR1 and TR2

TR1 & TR2 devices were selected to meet the following requirements:

a, To switch up to 500vdc + transients up to 700 volts.

b, To switch high currents up to 40 Amps.

c, High speed switching to reduce switching power losses.

d, Low Rds_{ON}, Drain Source ON resistance, to achieve low power dissipation.

The devices chosen to meet the above requirements and provide high reliability due to performance in excess of that required were APT 8018JNR.

Rated at:V_{DSS} max 800 volt, at I_D =40 Amps(continuous),160 Amps pulsed.

Rds_{ON} =0·18 ohm. Typical speed of switching: Turn-ON delay t_d =21ns,

tr =19ns,t_d(off) =70ns,t_f =13ns.

Device package: ISOTOP SOT-227, providing easy mounting on a proprietary heat sink unit (see Figure 2.3), using 2 fixings and heatsink compound only. Connections between the Gate,Drain & Source of the devices and the underside of the PBA HT Stabilizer are made via low inductance nickel plated bushes.

2.17 To estimate the worse case power dissipation in TR1 & TR2, it is necessary to determine the worse case RMS modulator charge current:

Consider a lower magnetron efficiency of 48%. The range of efficiencies obtained so far with 8 magnetrons has been between 50 and 64%.

For 1MW peak o/p RF power at a duty of 0·1344, ie; mean power o/p 1344 Watts. (2.17.1)

Required i/p power to magnetron: (1/0·48).1344 = 2800 Watts. (2.17.2)

Taking the modulator efficiency at 87%:

The required mean input power to the modulator=(1/0·87).2800=3218·4 Watts. (2.17.3)

Using a modulator HT of 342v, the mean i/p current to the modulator:

I_{mean} = I/P power to modulator/modulator HT = 3218·4/342 = 9·4 Amps. (2.17.4)

Using the chosen inductor value of 1·4mH, with 80 volts drop across the stabilizer and a charge duty of 0·5, the peak of the charge current:

I_{pk} = (2.I_{mean})/charge duty = (2.9·4)/0·5 = 37·6 Amps peak. (2.17.5)

To calculate the equivalent RMS value of the charge current it is reasonable to consider the waveform shape as a triangular ramp. The appropriate mathematical model to use:- $I_{RMS} = I_{PEAK}.(D/3)^{1/2}$ Where D = charge duty = 0.5. (2.17.6)

$I_{RMS} = 37·6.(0·5/3)^{1/2} = 15·35$ $Amps_{RMS}$. (2.17.7)

The most significant contributor to the power dissipated by the MOSFET's is conduction loss, caused by current flow through the Rds_{ON} resistance. The power dissipated is:

$Pd = I^2.Rds_{ON}$

$Pd = 15{\cdot}35^2.0.18 = \underline{42{\cdot}6}$ Watts, rounding up to say 45 Watts to allow for switching loss contribution (very low).

2.18 Cooling

A proprietary forced air cooled heat sink assembly was chosen for convenience and low cost, to provide cooling for TR1 & TR2 (see Figure 2.3 and photo 2P1). The location of the devices to be cooled is shown and the ideal location of the PBA required to mount the power MOSFET drive and control circuits. To allow direct screw (bush) connections to TR1 & TR2, 3oz copper plating was specified for the PBA, such that the M4 plated through holes are robust.

The manufacturer of the heat sink assembly provides design data in the form of graphs relating effective thermal resistance between the device mounting surface to ambient temperature to airflow/sector and heatsink/quadrant designs See Figure 2.4.

2.19 It was decided to use two sets of 4 quadrants (type 24WF-0137).

From the graph in Figure 2.4, it can be seen that using a standard 119mm x 119mm x 38mm axial fan having an air flow of 94.2 CFM, which gives 23.5 CFM/Quadrant, it is possible to achieve 0.83 deg C/Watt thermal resistance.

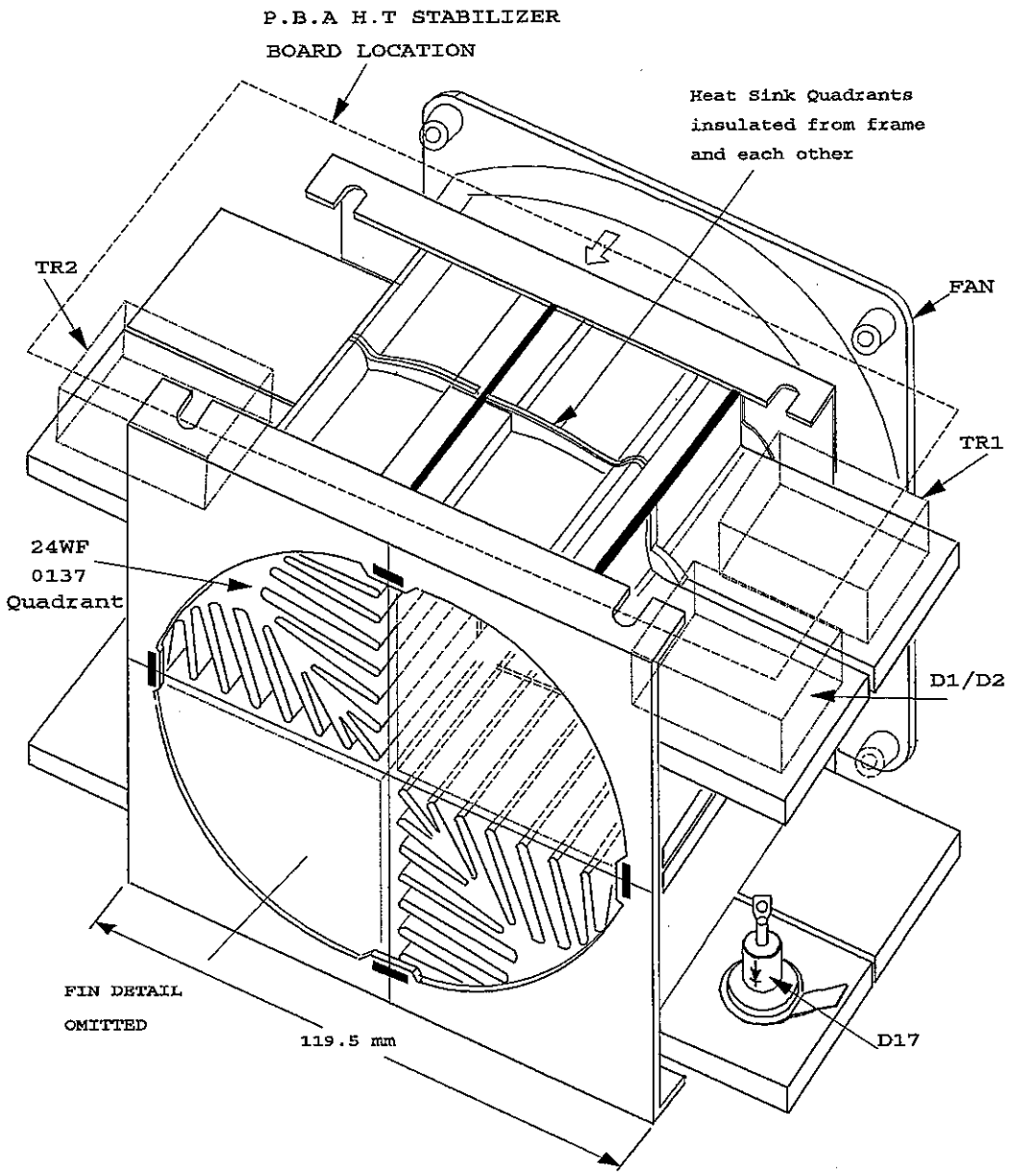

P.B.A H.T STABILIZER
BOARD LOCATION
Heat Sink Quadrants
insulated from frame
and each other
TR2
FAN
TR1
24WF
0137
Quadrant
D1/D2
FIN DETAIL
OMITTED
119.5 mm
D17

Figure 2.3

Proto type HT Stabilizer

2 P 1

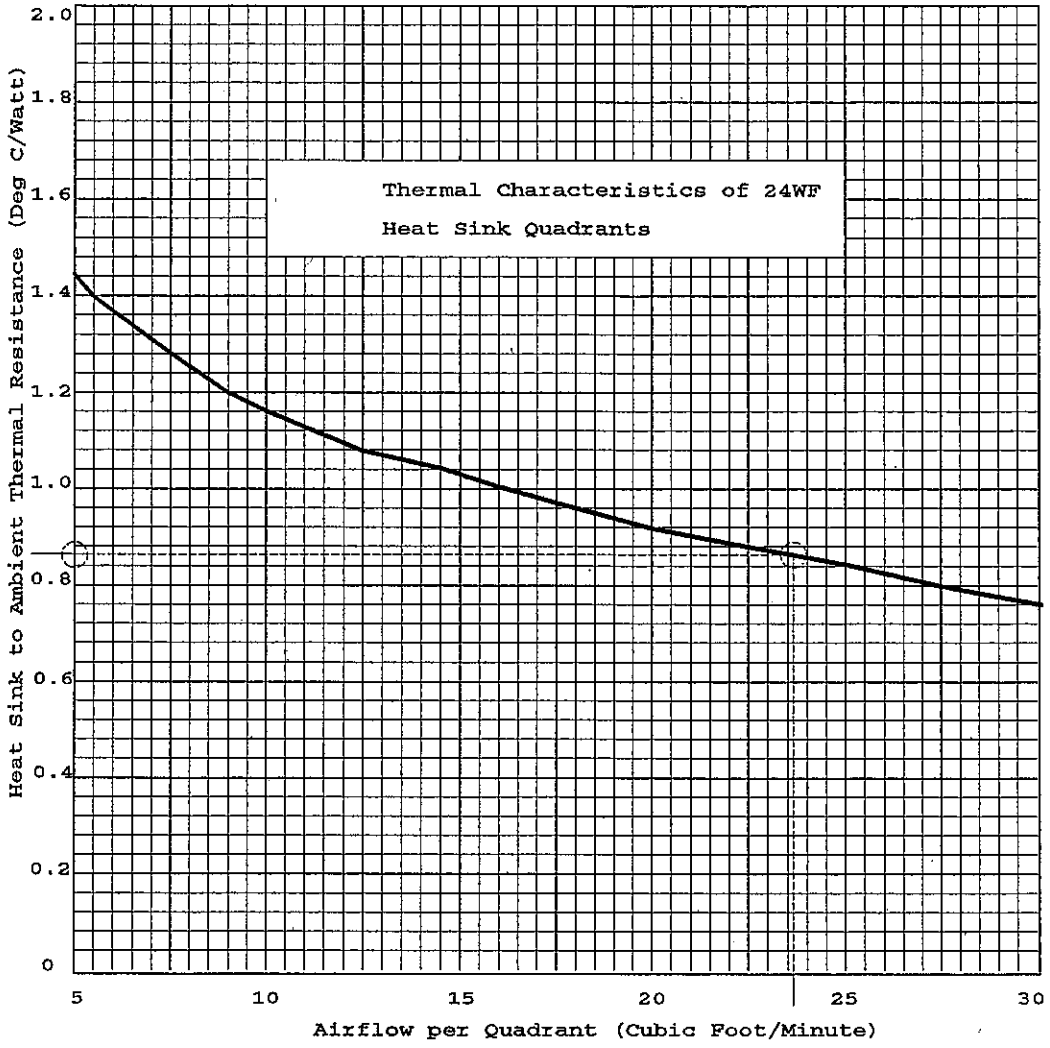


Figure 2.4

To predict the device junction temperature at the worst case ambient temperature (50°C) it is necessary to sum up the total thermal resistance between the junction of the device and ambient air:Thermal Resistance °C/Watt

Device Junction to Case	$R_{\theta JC}$	0· 18
+Device Case to Heat Sink	$R_{\theta CS}$	0· 05
+Heat Sink to Ambient Air	$R_{\theta SA}$	0· 83 Total $R_{\theta T}$= 1· 06 °C/Watt

The junction temperature is calculated:

T_j = (Power Dissipated x $R_{\theta T}$) + $T_{AMBIENT}$

T_j = (45.1· 06) + 50· = 97·7 °C.

The predicted maximum junction temperature of 97·7°C is satisfactory, as the maximum allowable junction temperature of the devices is 150°C.

The chosen heat sink configuration has capacity in hand should it be required for operation a higher duty.

2.20 Control Requirements

The HT Stabilizer required the following control facilities:

1 To receive a recharge trigger, and respond by switching ON TR1 & TR2.

2 To sense the modulator charge voltage (-EM), and when voltage has charged to a specific level, derived by monitoring the HT Control (0 --5v) level, switches OFF TR1 & TR2. (This sets the difference voltage across the stabilizer).

3 To sense the charge current into the stabilizer, and switch OFF TR1 & TR2 if the peak current exceeds a safe level. This facility is to limit the peak charge current during the initial charging of the modulator capacitors from 0v (initial charging takes a number of charge cycles) and also to protect TR1 & TR2 in the event of a short circuit at the o/p of the stabilizer.

4 Should TR1 & TR2 fail to switch OFF before the modulator is due to be pulsed, TR1 & TR2 are switched OFF by the Discharge Trigger.

5 To sense the modulator voltage -EM and provide an Over-Voltage monitor and logic output.

A block diagram Figure 2.5 shows the required control functions:

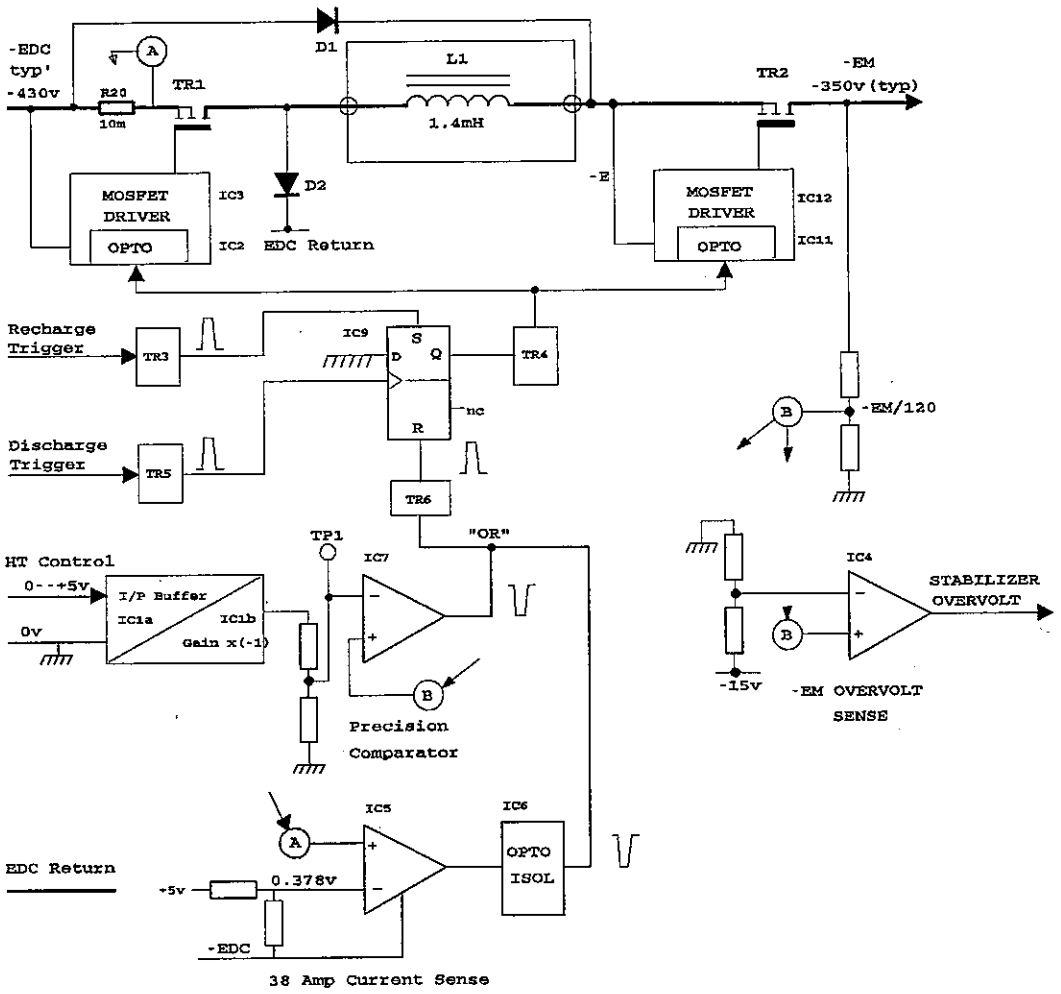


Figure 2.5: HT Stabilizer Block Diagram

2.21 HT Stabilizer Control Circuit

Modulator Charging and HT Stabilization is initiated by a Recharge Trigger input from the Signal Processor.

The Recharge Trigger is a +13.5v (nom) pulse, 1 μs PW at 840 Hz PRF (nominal), occurring at a **fixed** 820 μs before the Discharge Trigger which triggers a modulator discharge. The PRF of both triggers may be STAGGERED (6 period +/-14%) if selected.

A pulse receiver circuit was required on the HT Stabilizer to monitor the Recharge pulse and provide protection against possible voltage transients. The pulse is terminated in 50 ohms on PBA Control.

The circuit chosen to perform the function was a simple transistor emitter follower with a diode clamp protection circuit on the base input. The pulse receiver circuit was required to provide a high active set pulse for IC9, a CMOS 4013B D Type flip-flop. The transistor chosen for the pulse receiver was a 2N2907A, a fast PNP switching device.

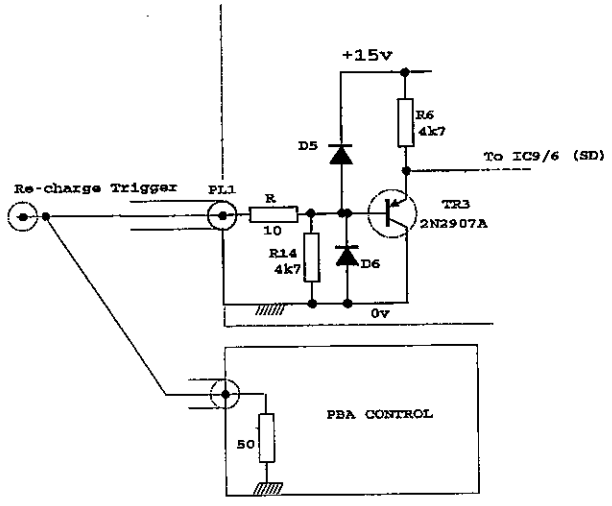


Figure 2.6

The base of TR3 is connected to 0v via R14/4k7 which biases the transistor in the ON state in-between pulse inputs. This is to ensure that the SD input of the D type flip flop IC9 is firmly clamped at a low potential (≈0·7v) to ensure that the D type is not set by noise transients.

The load on the (50Ω) pulse input is set by the value of R14 due to the very high input resistance of the emitter follower

Rin = hie+(1+hfe)R6. ≈hfe.R6 = 470 kΩ minimum.

An identical circuit (TR5) is used to buffer the Discharge trigger.

The Discharge trigger i/p is only used as a back-up to reset IC9 (to switch OFF TR1 & TR2) should the normal IC9 reset from IC7/TR6 fail due to a fault.

2.22 The ON/OFF state of TR1 and TR2 is controlled by the output of a D type flip flop IC9/1. Q o/p = High TR1/2 ON, Q o/p = Low TR1/2 OFF.

A CMOS 4013B device was chosen for reasons of:

a, Low dynamic power dissipation

b, High immunity to noise, due to 15v supply. The logic 1 threshold is typically 0.5 x Vcc supply voltage.

The electromagnetic environment where the PBA HT Stabilizer is located is very harsh (noisy) with a high risk of transients being induced in any track or wire. It is essential when using 4000 series CMOS that all inputs and output are adequately buffered and protected against voltage transients. The 4000 series CMOS devices are prone to a phenomenon called "SCR latch-up effect[8]" if techniques are not used to control transients.

2.23 The Q output of IC9 is buffered by TR4 (VNO300M), an N channel power MOSFET configured as a High Side Switch. A P channel MOSFET is usually better used as a High Side Switch, however the VNO300M is a very popular low cost device ideal for interfacing logic devices to peripheral devices requiring high voltage (V_{DS} 30v), high current (I_D 0·67A) and fast switching (t_{ON} t_{OFF} 30ns). The device also has low ON resistance (R_{DSON} 1·2Ω) for low dissipation.

TR4 is used to provide the drive current for two opto-isolators, which are connected between the source and 0v (ground).

The o/p voltage available at the source is:

$V_{o/p} = V_{GG} - V_{GS(th)}$ Where V_{GG} is the logic high o/p from IC9 eg, 14.95v. and $V_{GS(th)}$ is the Gate/Source threshold voltage 2.5v max (0.8v typ).

$V_{o/p} = 14.95 - 0.8 =$ 14.15v typical.

2.24 Opto-Couplers IC2 & IC11

The Gate/Source drive circuits for TR1 and TR2 are floating at -EDC and -EM respectively, therefore have to be opto isolated from the ground referenced circuits. The opto-couplers chosen for IC2 & IC11 are Hewlett Packard HCPL-2211 devices.

From the HPCL-2211 data sheets the recommended I_F (Forward Input Current) is 2.2mA to provide 20% Current Transfer Ratio degradation guard-band.

And using a typical input diode forward characteristic graph provided the V_F (Input Forward Voltage) is determined at 1.45v.

The required value of resistor for R18 and R19:

$R = (V_{o/p} - V_F)/I_F$

$R = (14.95 - 1.45)/2.2.10^{-3} = \underline{6.136}k\Omega$, nearest lower preferred value $\underline{5.6}$ kΩ.

Therefore the I_F is slightly higher, approximately 2.4 mA.

TR4 provides current drive for IC2 and IC11, ie 2 x 2·4 mA = $\underline{4{\cdot}8}$mA for 600μs in 1·19mS ie, the charge duty 0·5 (2.14.1)

Therefore TR4 I_D mean current = $4{\cdot}8.10^{-3}$ x 0·5 = $\underline{2{\cdot}4}$ mA.

The mean power dissipation is $I_D^2.R_{DSON}$

$= (2{\cdot}4.10^{-3})^2.\ 1{\cdot}2 = \underline{6{\cdot}9}\ \mu W$. negligible.

2.25 TR1/TR2 MOSFET Drive Circuits

The high active outputs of the HCPL2211 opto-couplers are used to drive TC4420 power MOSFET gate drive IC's. The TC4420 is used to provide a very low source & sink impedance required to deliver high transient current (6 Amp peak)to charge the Gate-Source input capacitance (Ciss) of power MOSFETS. Fast charging of Ciss leads to fast switching and low switching losses. The TC4420 gate drive IC's are placed as close as possible to the Gate/Source connections of TR1 & TR2 to minimise the inductance. A 10μF tantalum and 0.1μF ceramic capacitors are placed directly across the supply connections of IC3 & IC12 to source the current required to charge the gates.

Two independent floating +15v supplies are provided as inputs to the PBA HT Stabilizer, for the TR1 & TR2 Drive Circuits, which are floating at -EDC (-430vDC typical) and -EM (-350vDC typical).

2.26 A sample of the modulator power supply HT Control voltage is buffered by a unity gain voltage follower IC1a and then inverted by IC1b. An AD708JN Dual OP AMP[4] was chosen for reasons of precision, low drift, low offset & low cost.

For a typical -EDC of -430v, a modulator voltage -EM of -350v is required, setting the voltage across the stabilizer at 80v.

-EM is monitored using a potential divider network comprising 2 x 68k(1 Watt rating) connected in series to the -EM o/p and a 1k14 0.1% resistor down to ground. The values were chosen to set the pot down ratio to -EM/120.

Therefore with -EM at -350v, -EM/120 = -2.916'volts.

Refer to Figure 2.9 below:

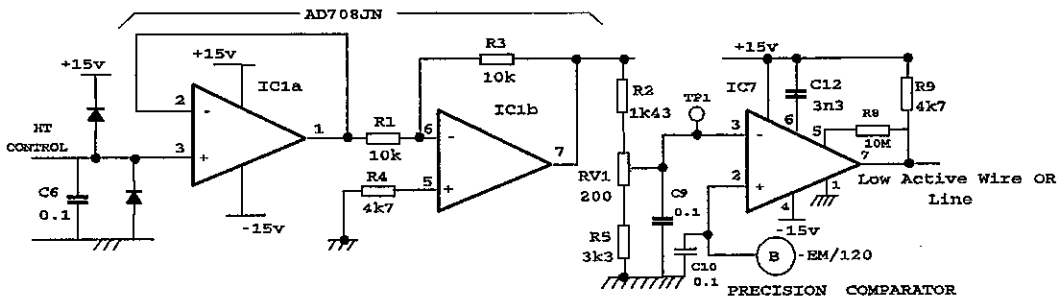


Figure 2.7

For a -EDC of -430v it is required that the HT Stabilizer ceases charging the modulator when -EM reaches -350v, therefore the reference level on TP1 needs to be set at -2.916' volts when the HT Control voltage i/p is 4.3 volt.

The potential divider network R2,RV1 & R5 is used to set the reference level on TP1, input to precision comparator IC7(LT1011A[9]). The HT Control voltage i/p is a relatively clean integrated DC level free from modulator power supply ripple and surges due to PRI STAGGER. -EDC tracks with the HT Control voltage.

2.27 IC1,IC7,IC5,IC6,IC9,IC4 and associated components have been carefully laid out to reduce induced noise, by minimising track lengths, use of a ground plane and generous supply rail decoupling using 10μF and 0.1μF capacitors.

A variation of 10mV on the -EM voltage level (typically -350v) gives a variation of 20mV/120 = 166.7μV at the +ve input of comparator IC7. To achieve stabilization of 20mV in 350v over 4 PRI intervals, the noise fluctuations on the reference (TP1) and -EM/120 track needed to be less than 166.7 μV.

Noise fluctuations on the reference or -EM/120 just before the modulator voltage -EM reaches the required level adds uncertainty in the point where IC7 comparator switches, which causes TR1 & TR2 to switch OFF, to cease modulator charging. C9/0.1 and C10/0.1 ceramic capacitors have been added to filter noise at the inputs of IC7.

2.28 The o/p of IC7 is an open collector with a pull up resistor R9, and when the modulator voltage sample -EM/120 compares with the reference, it switches low. The o/p of IC7 is used to drive the gate of a VNO300M MOSFET which is used to produce a high active reset level for IC9, to terminate the modulator charge as described previously. The o/p of IC7 track is effectively a wire OR line, shared with the open collector of the o/p transistor of opto-coupler IC6.

2.29 IC6 opto-coupler input is driven by another comparator IC5/LT1116 which is used to sense the modulator charge current into the source of TR1 via R20/10mΩ. Comparator IC5 and associated 5v regulator IC10 are floating on the -EDC supply input, hence the need to be optically coupled to the ground referenced control circuits. The reference input on IC5/3 (-ve) is set to 0·38v by potential divider R10/3k3 and R11/270.

Should the voltage sample from R20, input on IC5/2 exceed +0·38v more positive than the reference input, the o/p on pin 7 switches high (+5v relative to -EDC) which used to drive current into the LED of the opto-coupler.

IC5 circuit is used to detect the condition when the modulator charge current exceeds 38 Amps, and cause the switching OFF of TR1 and TR2.

During transmission when the modulator voltage is required to be topped up by 3 to 4 volts after each modulator discharge (ref:para 2.11) the charge current is typically between 32 to 35 Amps, and IC5 never switches.

IC5 comparator protects TR1 and TR2 during initial modulator charging, where charging requires a number of PRI's and provides short circuit protection of the HT Stabilizer.

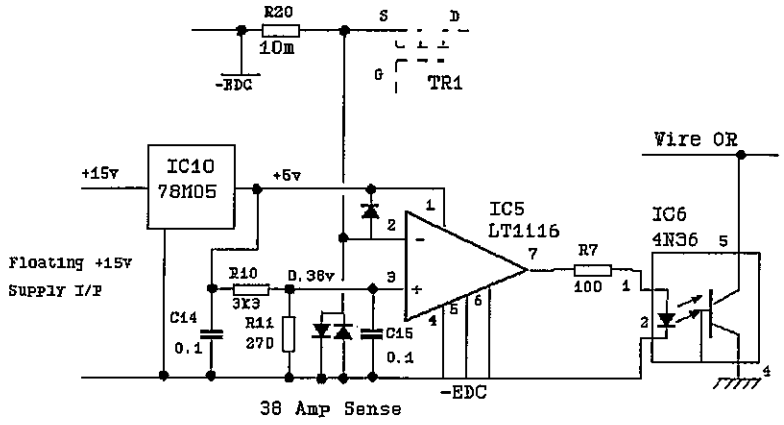


Figure 2.8

The HT Stabilizer circuit diagram and component layout are shown in Figures 2.11 and 2.12 (pages 88 & 89 respectively).

2.30 Performance

The modulator HT stabilization performance was measured using the test apparatus described in Appendix 6. Calibration of the equipment was carried out using 100mV,80mV,60mV,40mV and 20mV pulses.

The stabilization achieved far exceeded the design aim, and was measured to be better than 20mV Peak to Peak (typically 10mV) in -350v over any group of 4 modulator charge / discharge cycles. Actual plots shown in Figures 2.9 & 2.10: Conversion of the Peak-Peak modulator HT stability "ΔVp" into Peak to Peak magnetron cathode current stability "ΔI_a" is performed using the dynamic sensitivity figure S = 0.52 Amps/ Vp volt (Ref: para 2.3):

Worse Case:

Vp = 20mV

Therefore $\Delta I_a = 0.52 \times 20.10^{-3} = \underline{10{\cdot}4}$ mA.

Using the 15 kHz/Amp pushing figure of the valve, the Peak to Peak frequency modulation is:

$$\Delta f = 15.10^3 \times 10{\cdot}4.10^{-3} = \underline{156} \text{ Hz}$$

Using +/- 3σ limits, ie. 6 standard deviations within the peak to peak, assuming that the variation of Vp is random caused by noise at the inputs of IC7:

The Standard Deviation of the frequency modulation is 156/6 = $\underline{26}$ Hz.

Stability limitation factor contribution due to frequency pushing:

$I_{\Delta f} = 20\text{Log}(\ 1/\ \pi.\Delta f.\tau\ )$ dB[1] $= 20\text{Log}(7651{\cdot}7) = \underline{77{\cdot}7}$ dB.

Where Δf is the frequency pushing in standard deviation & τ = 1·6 μS PW.

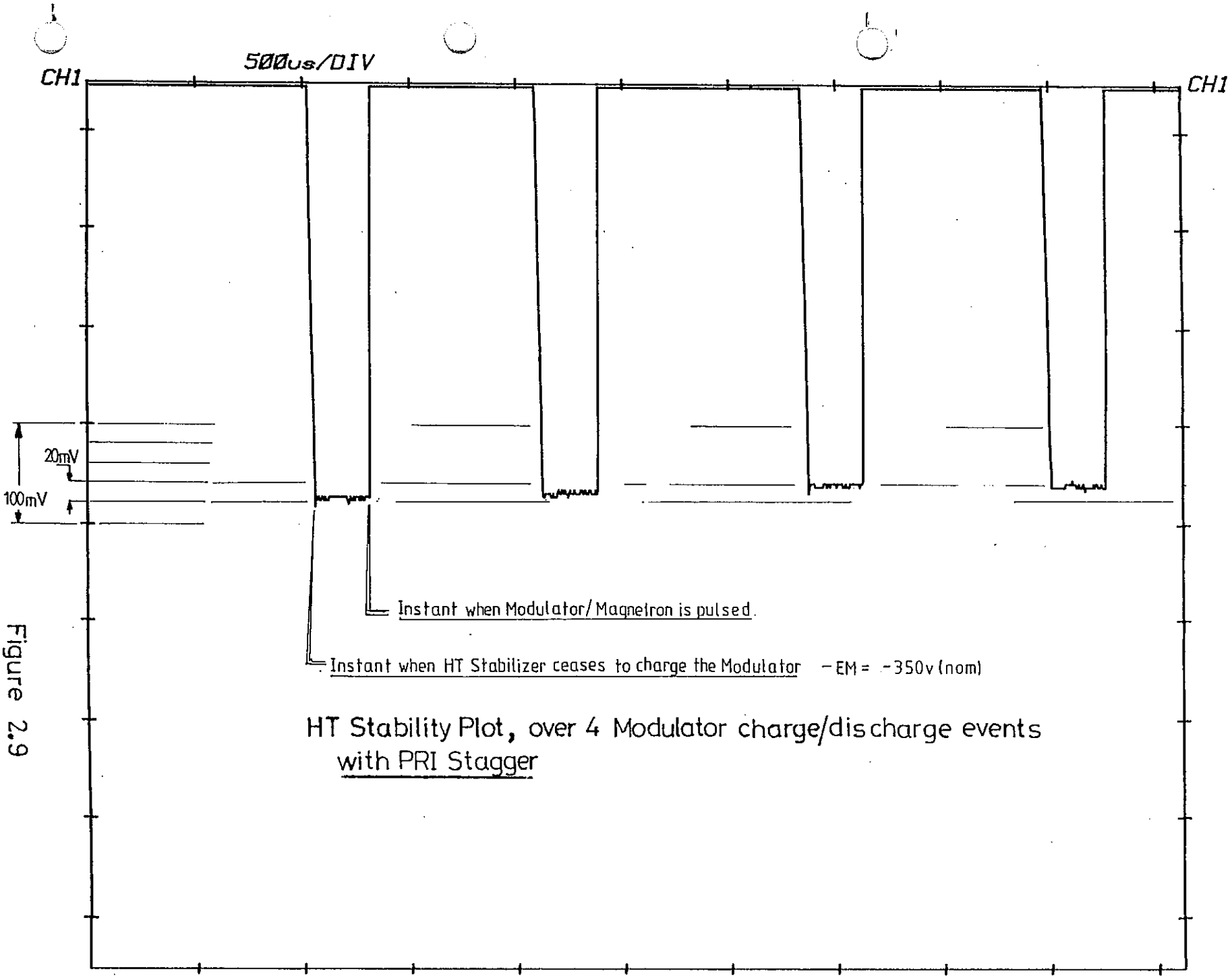


Figure 2.9

HT Stability Plot, over 4 Modulator charge/discharge events with PRI Stagger

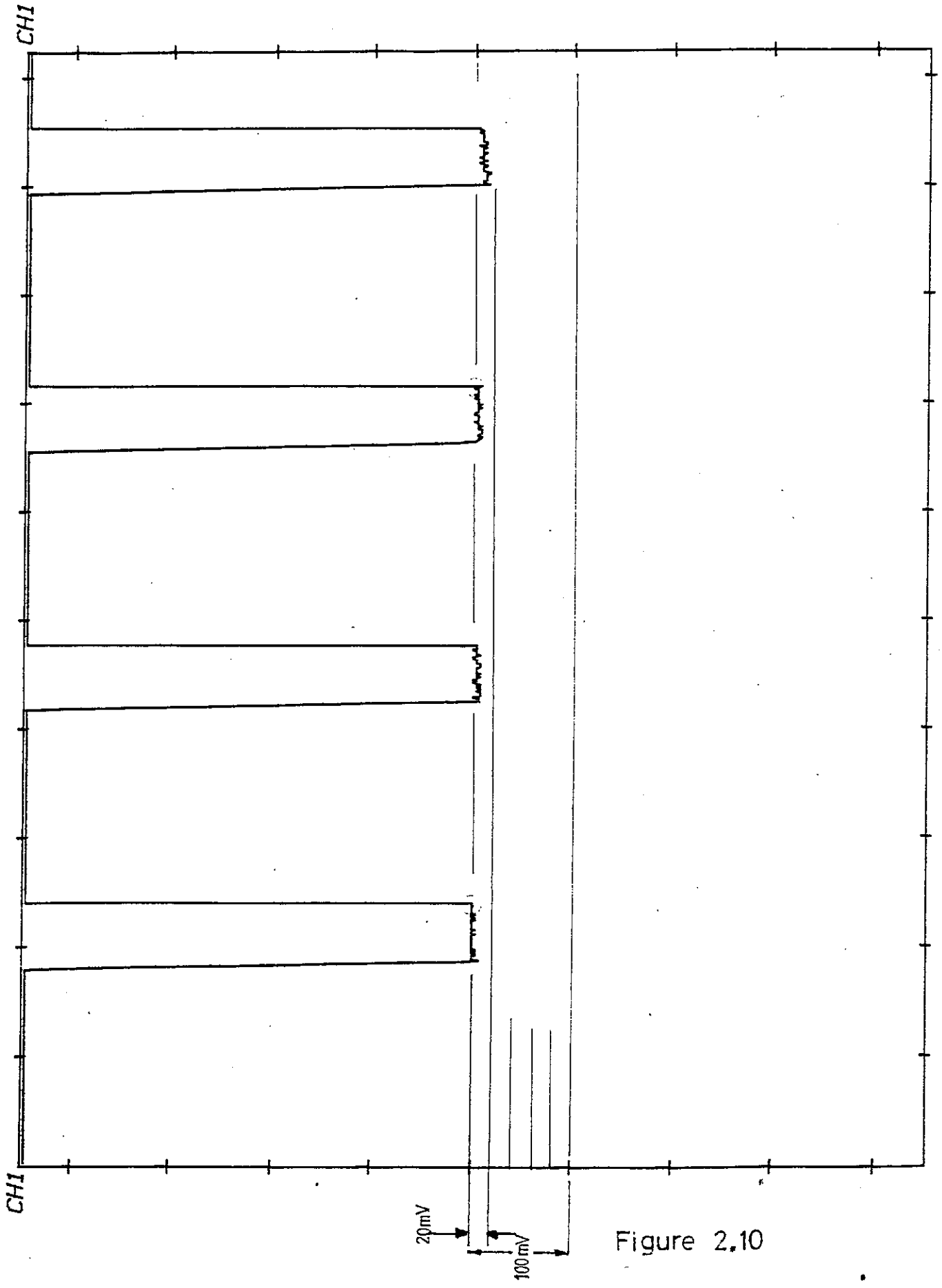


Figure 2.10

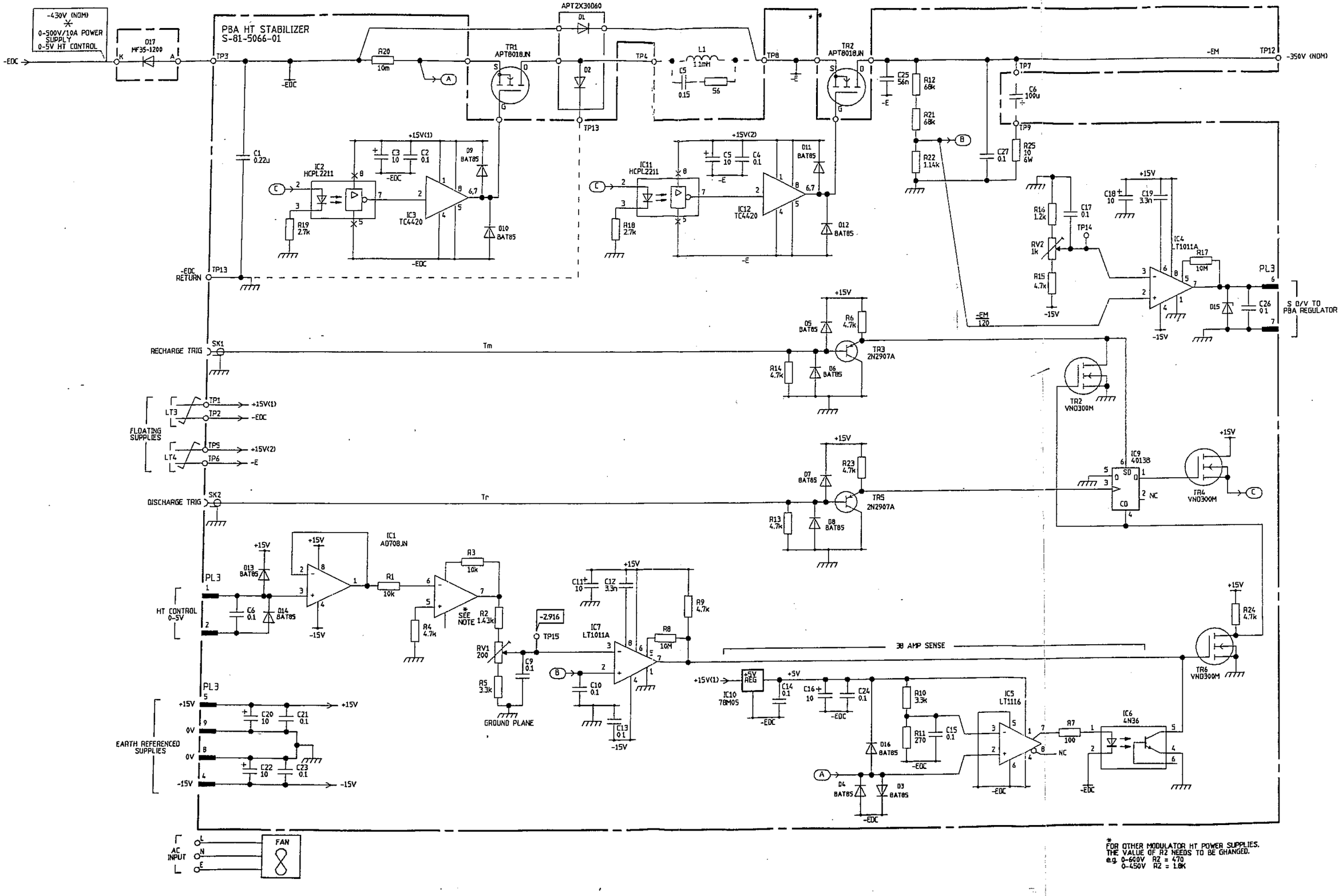


Figure 2.11: HT Stabilizer Assembly

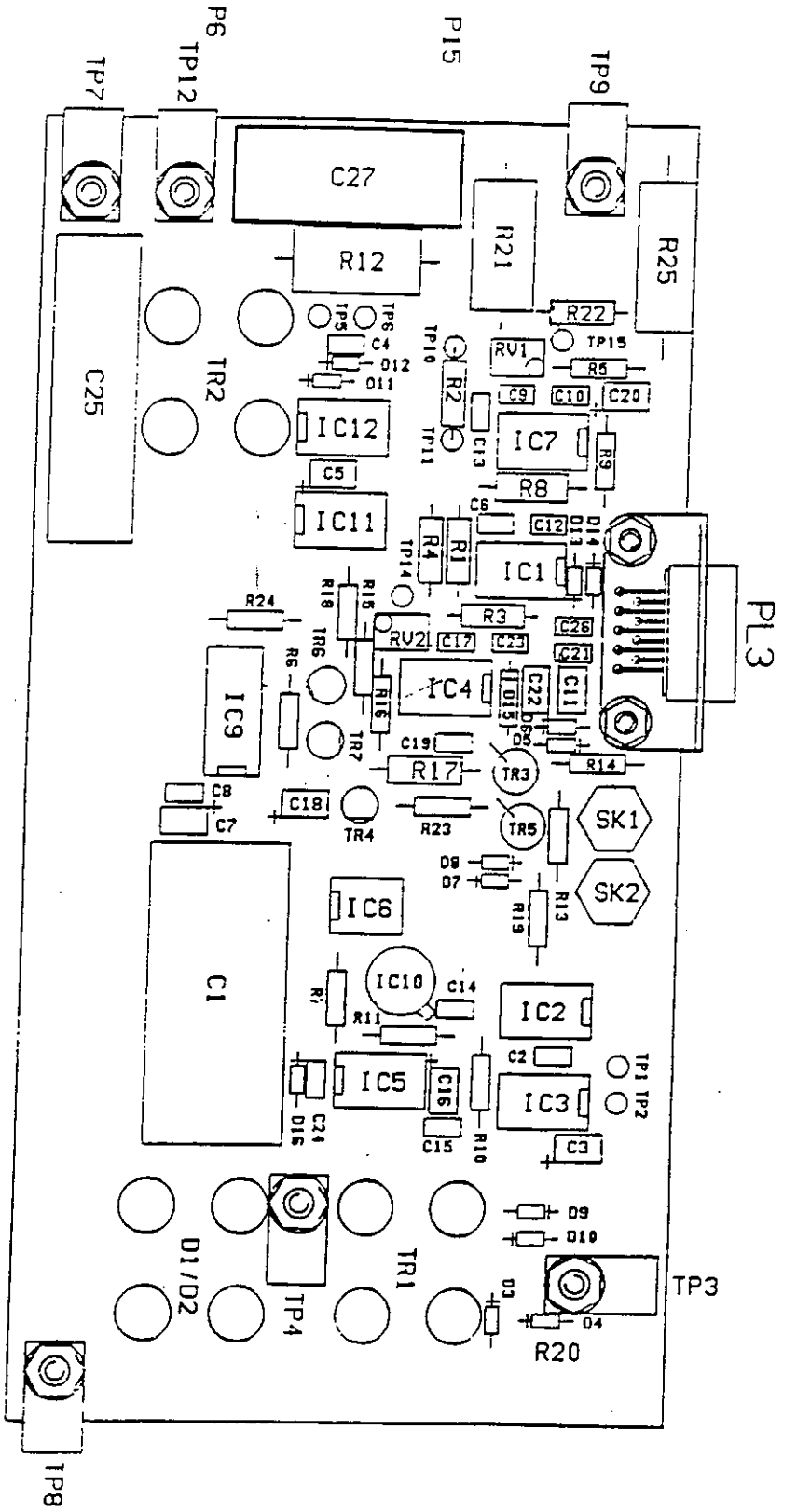


Figure 2.12: PBA HT Stabilizer

3.1 Introduction

The Solid State Modulator used in the S2055 produces a typical -34KV, 52 Amp pulse, which has a rise time (rate of rise) too fast to apply directly to the magnetron cathode, the magnetron would arc and fail to oscillate.

The initial rate of rise of a cathode voltage pulse is usually controlled by fitting a capacitor between the HV pulse output from the modulator and ground. The capacitor in conjunction with the effective source impedance of the HV pulse, forms a filter which filters high frequency components of the HV pulse and so reduces the rate of rise. The arrangement is often referred to as a De-Spiking network.

It is possible to get a coaxial magnetron to operate with a simple capacitor rate of rise control, however efficient start up of oscillation, subsequent low jitter on the front edge of the RF pulse and long tube life is not obtained.

To achieve efficient start up of oscillation in the magnetron at the frequency to which the outer stabilizing cavity is tuned requires the front edge rate of rise of the voltage pulse to be reduced and profiled in a particular manner. The manufacturer of the MG5403 tube specifies that the initial rate of rise should be between 100 and 150KV/μs, and that the final rate should be between 30 and 60KV/μs up to the full HT. It has been found during the development of the PVCU that the final rate of rise and the threshold of the rate of rise change are critical if the lowest jitter is to be obtained. The measurement of jitter using just an oscilloscope is inadequate, and only an indication. The equipment described in Appendix 3 must be used to evaluate the standard deviation and peak to peak jitter. The causes of RF Pulse Jitter is detailed in Appendix 8.

3.2 Design Aims

The design aims were:-

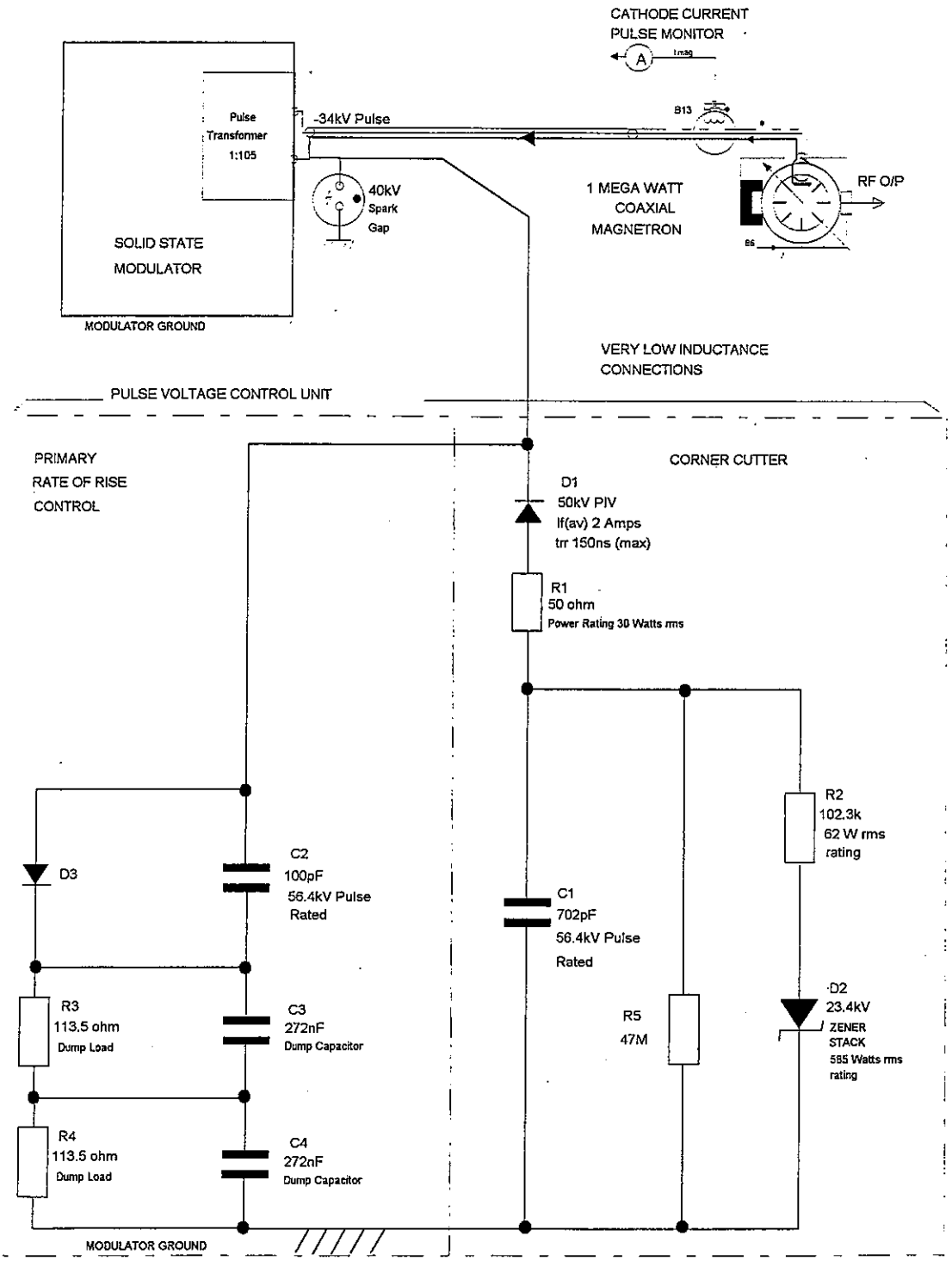
a, To develop a compact, low cost rate of rise profiling network, without the use of transformer oil.

b, To achieve rate of rise transitions, in a clean smooth manner, such that, within the coaxial magnetron, once the rotating space charge has reached the minimum circumferential velocity for synchronisation, the flow of energy from the space charge into the slow wave structure is not disrupted. Any cathode voltage fluctuation at this critical phase will cause delay in synchronisation which results in jitter.

3.3 Background

The network required to profile the front edge of the cathode voltage pulse is known as a Corner Cutter, and is not a new technique. A corner cutter unit used at the tube factory in a test facility for the MG5403 tubes is an oil filled design. An oil tank cooling arrangement adds considerable cost and size to the unit. Consultation with the tube manufacturer yielded a simple schematic without component values, similar to that shown in Figure 3.1.

An initial investigation was carried out to examine the types of components used in existing corner cutter designs with a view to finding lower cost alternatives. Following the development of the S2055 Pulse Voltage Control Unit a similar schematic to Figure 3.1 was found in a book[3], however a picture of the associated front edge profile of the cathode voltage pulse showed an undesirable ring (voltage disturbance) just after the rate of rise change, which would cause degradation of jitter performance. The final rate of rise transition to full HT must be smooth.



PVCU Simplified Circuit

Figure 3.1

3.4 Corner Cutter Operation

During the first pulse, secondary rate of rise control does not occur.

C1 is fully discharged and as soon as the cathode voltage starts to go negative, D1 conducts to charge C1 via R1. C1 charges up to the peak cathode voltage. When the voltage on C1 approaches the peak cathode voltage pulse level D1 switches off, to disconnect the C1 load.

During the interpulse period C1 discharges via R2 and zener diode stack D2(23·4kV). The potential on C1 eventually reaches that where D2 ceases to conduct, leaving only a small leakage current through D2 and the C1 voltage sharing resistors R5. The voltage on C1 acts as a reverse bias on D1, a threshold beyond which a cathode voltage pulse level must exceed before D1 switches ON to connect the C1 load. The threshold is the zener stack voltage which is approximately 70%, however the actual threshold is set for lowest jitter on the front edge of the RF pulse which in the case of Surveyor was 117 x 200v zeners.

Primary Rate of Rise Control

The primary rate of rise is controlled by C2.

C3,C4,R3 & R4 form a power dump to dissipate the energy stored in C2 during the pulse when it transfers to C3 & C4 as the cathode voltage pulse returns to 0v at the end of the pulse.

3.5.1 Criteria for Physical Form

It was required that the Solid State Modulator, Magnetron and associated units had to fit in the lower half of a standard 19" width cabinet. See Preface, Figure 3 and Chapter 1, Figure 1.2. It became apparent when considering the locations of the major units that the location and volume available for the Pulse Voltage Control Unit could only be at the rear of the HV Pulse Transformer. In order to minimise the length and inductance of the HV connection between the HV Pulse Transformer and PVCU, the HV connection (top of the PVCU) had to be adjacent to the top of the HV Pulse Transformer. It is good practice to minimise parasitic inductances in the electrical connections between components of High Voltage and Current circuits where transient changes occur in the circuit. Even very small connection inductances can store energy ($1/2LI^2$ Joules) which can cause high transient voltage disturbances should the current charging the inductance be suddenly discontinued. Parasitic inductance and capacitance in a circuit that is likely to be subjected to high voltage transitions with fast rates of rise can ring (oscillate). With this in mind, it must be remembered that as the instantaneous cathode voltage increases from 0v negatively along the rate of rise profile towards the peak cathode voltage, the circumferential velocity of the cylindrical space charge in the interaction space between the cathode and anode vanes, is increasing proportionally.

3.5.2 In the initial stages of the design it was not certain that an air cooled design was feasible due to high power dissipation, and that the components would have to be immersed in a cooling tank filled with Shell Dialla B transformer oil.

It was decided to proceed with a design that could be adapted for either solution.

3.5.3 It was decided to mount the components on two large PECs, supported by an insulating frame, vertically to allow cooling currents (oil or air) to rise up through the components. The largest practical PEC size (14"x 23") was determined from consultation with the Printed Circuit Techniques Group. The requirement for large PECs was decided by the envisaged number of discrete components.

3.5.4 The form of the PVCU emerged as a tall rectangular frame, supporting a PEC on each side. It was decided to mount the components on the inside faces of the PECs such that forced cooling could be directed up through the middle and in an air cooled solution to purge out any ions as they are produced.

The material used for the frame parts needed to have very high surface insulation,high dielectric strength, low absorbtion of moisture, high physical strength (to support weight of PECs and components) and fire resistance.

It was decided to use electrical grade glass epoxide laminate, Permaglass MER20 produced by Permali (Gloucester).

Specification:-

Surface Resistivity $>10^{14}\ \Omega$

Volume Resistivity $>10^{14}\Omega$CM

Comparative Tracking Index >600V (BS5901)

Dielectric Strength 9kV/mm

Water Absorbtion 0·025%

The material is very strong and provides rigid support for the large PECs. The PECs are secured to the frame using nylon screws. 1 cm diameter nickel plated brass rods are used to provide low inductance connections between the PECs. The nickel plating is used to minimise electrolytic corrosion to ensure good conductivity. The PEC tinned copper lands, pads & tracks are 3oz plate.

3.5.5 Due to the high voltage nature of the unit, the author manually designed and produced component layout drawings, using a creep distance figure of 5kV/inch and slot techniques to enhance creep distances between components and reduce circuit inductances. The production form of the unit is almost identical to the prototype unit made by the author, see photographs 3.P.1 to 4. The final solution was air cooled following design improvements to reduce power dissipation.

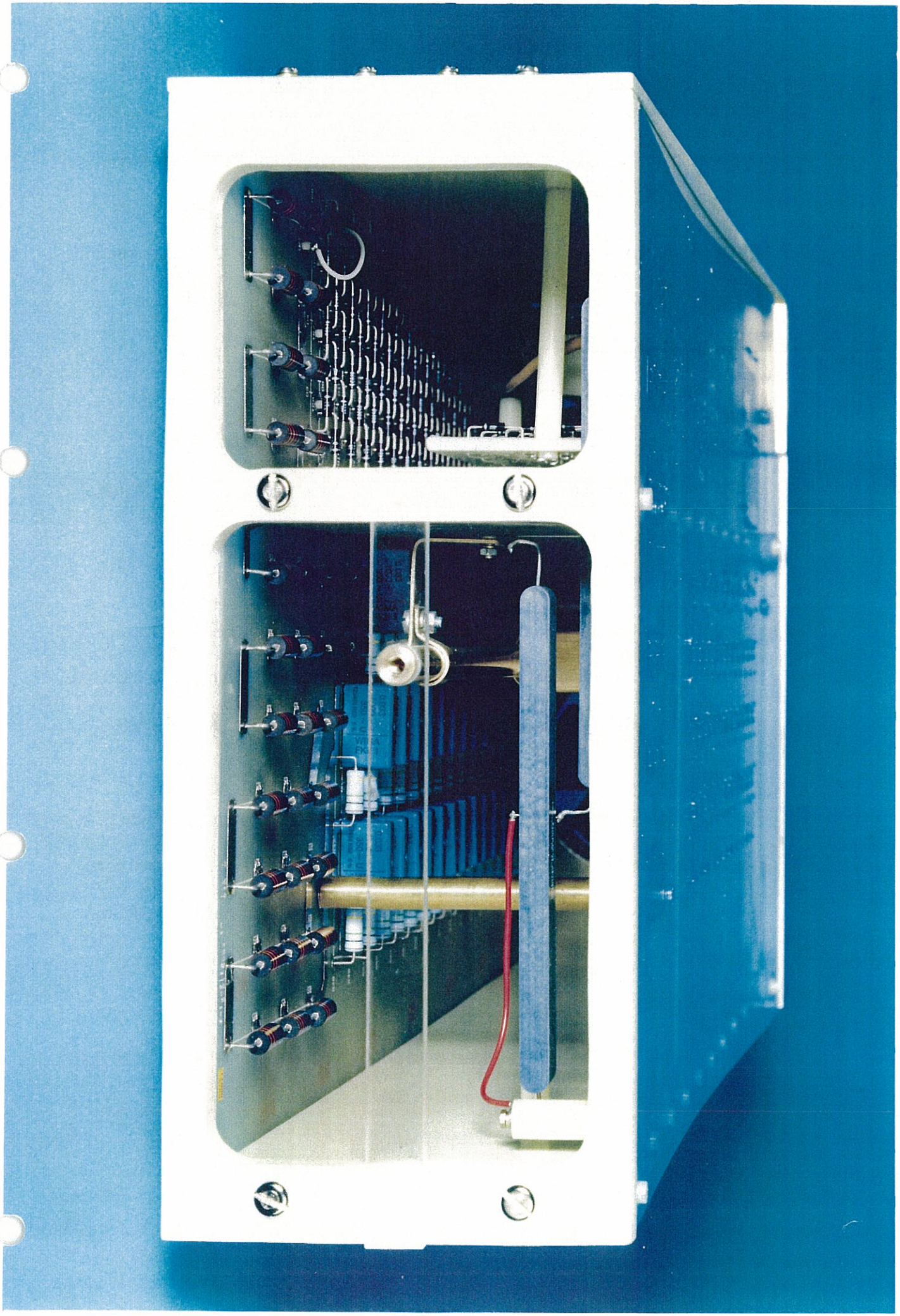
3.6.1 Circuit Simulation

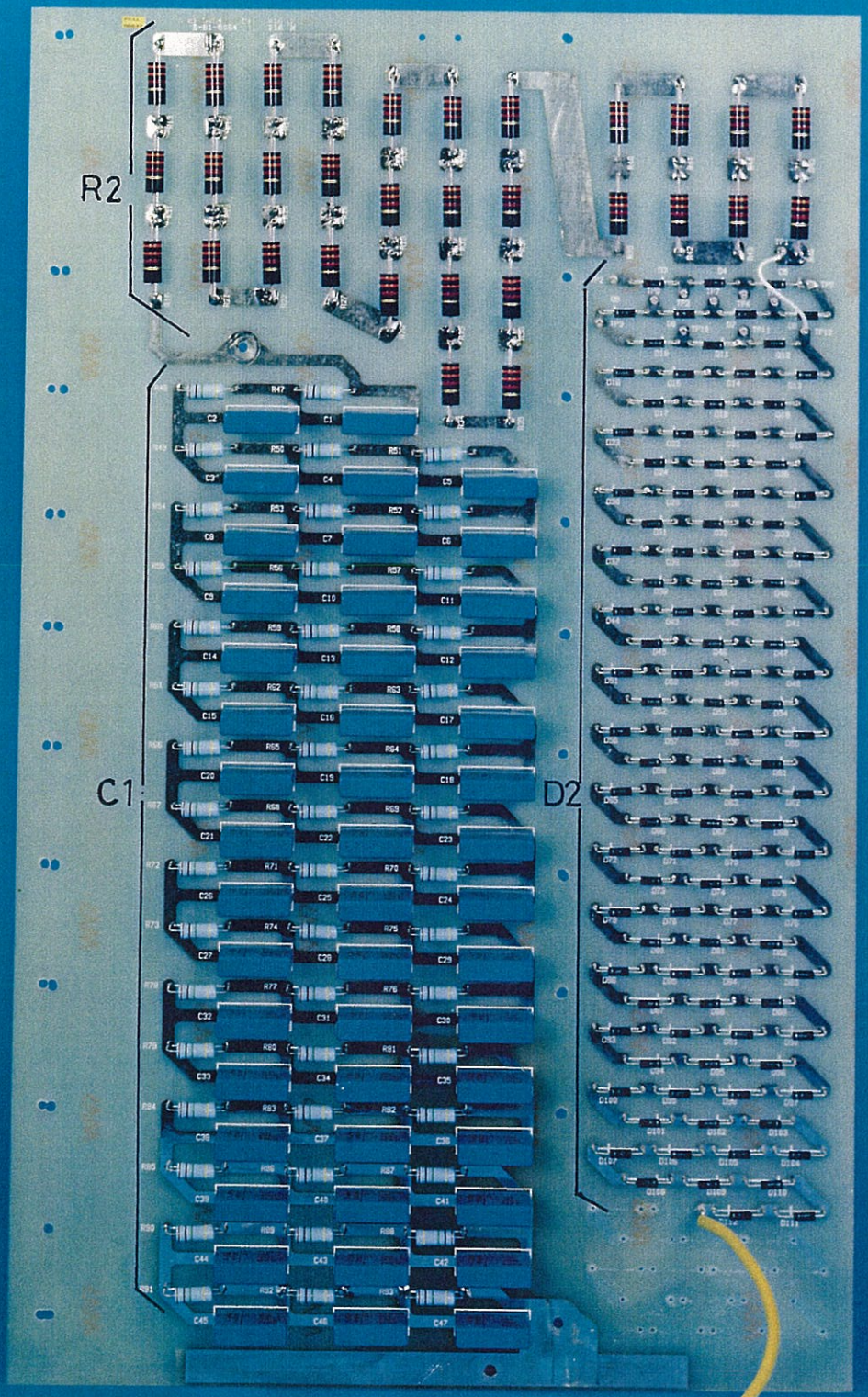
Circuits operating at high voltages & currents levels require components of specialized nature, and can be very expensive with long lead times. The uncertainty with respect to the power dissipations with the technical and financial risk of having to go for an oil tank solution led to the need for computer simulation. PSPICE(Student Version) was used.

3.6.2 A lumped element circuit model was prepared see Figure 3.2, 3.2.1 & 3.2.2. Using PSPICE it was possible to determine initial component values to achieve the rates of rise profile required, and to quickly determine the average and RMS current and power in any component.

The PVCU was originally constructed with the initial value components fitted, then installed into the S2055 prototype. The test apparatus and method described in Appendix 3 was used to adjust C1, C2 values & D2 zener voltage threshold levels.

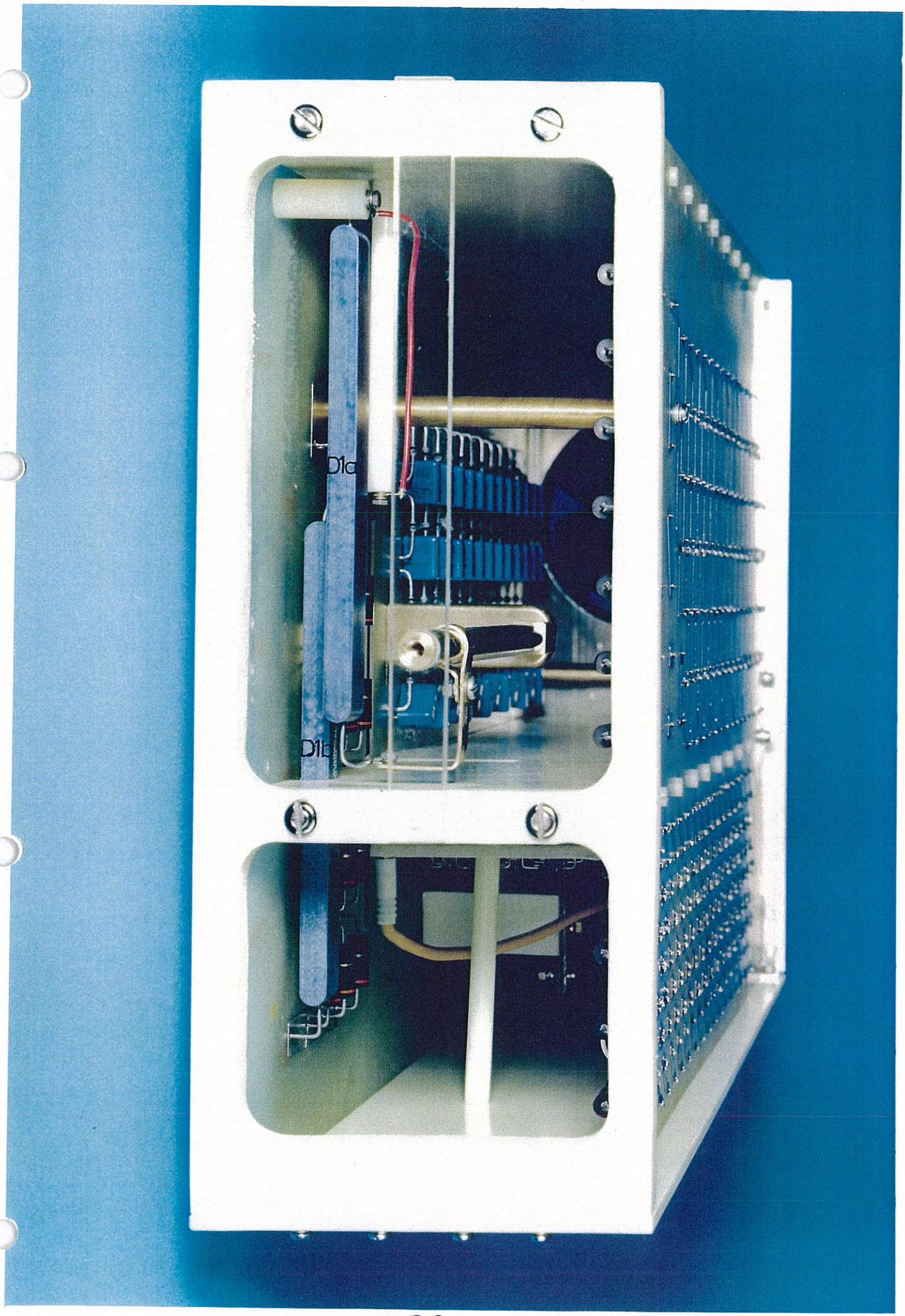
The two waveforms of significance are shown in Figures 3.3, 3.4 & 3.5, resemblance to the actual waveforms monitored in the S2055 reference transmitter can be seen in Appendix 8 Figure 5.



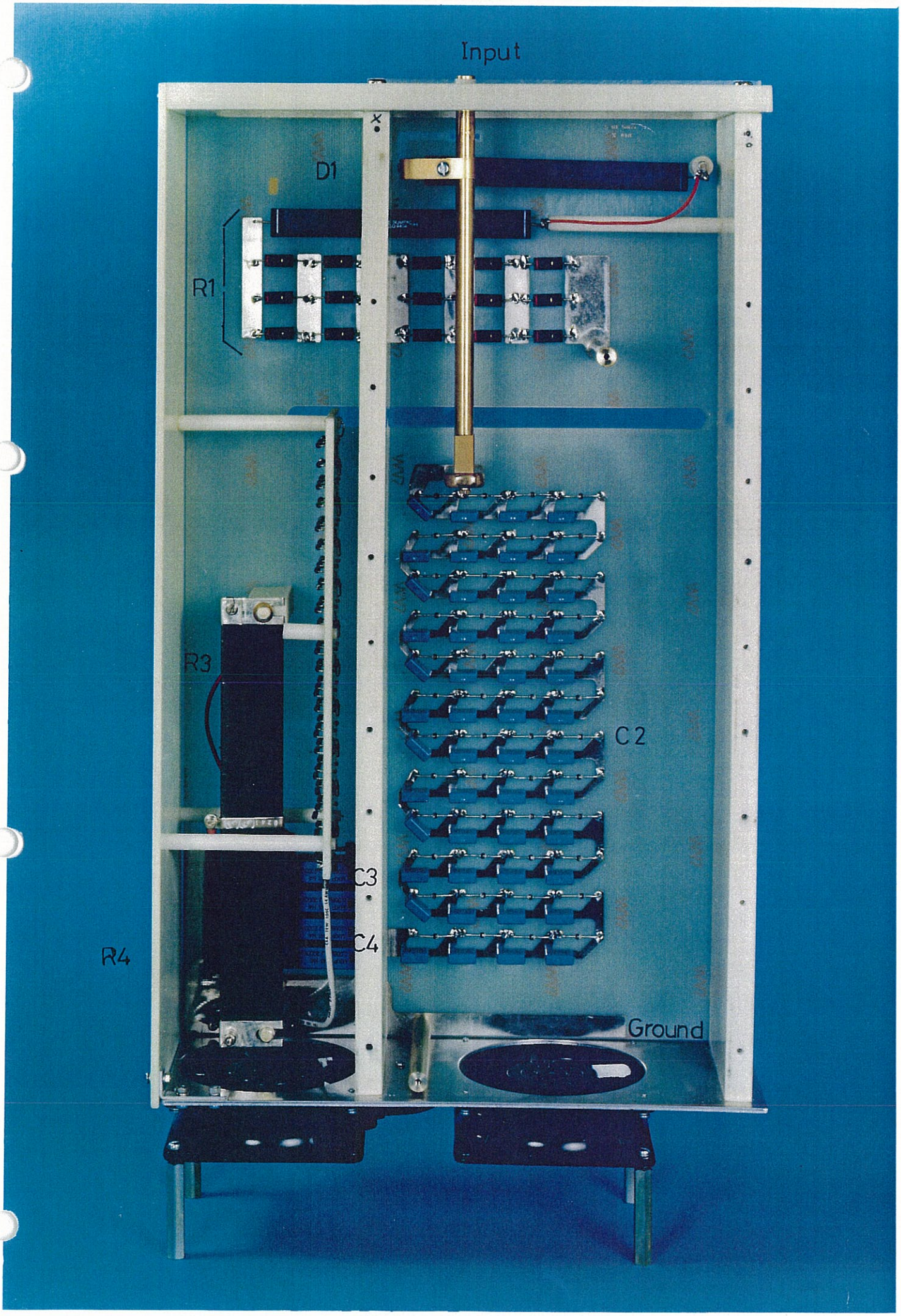


Prototype

3.P.2



3.P.3



3 P 4

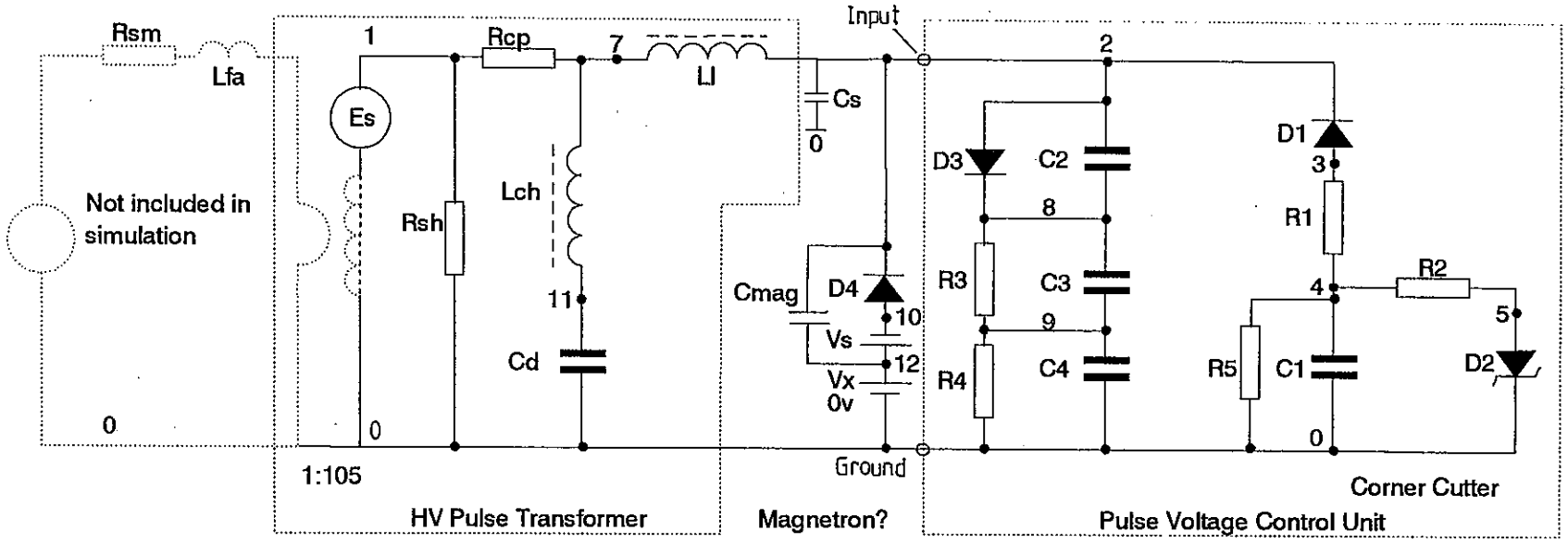


Figure 3.2 PSPICE EVALUATION OF P.V.C.U. (Circuit)

```
* Corner Cutter

.OPTIONS RELTOL=0.05  ITL5=0
* Input pulse simulating "Es" a -34kv pulse at 840Hz
* having a pulse width of 1.6 micro seconds..
VPULSE 1 0 PULSE (0 -34E3 0NS 10NS 10NS 1.6E-6 1.19E-3)

*----------------
*Simulation of Pulse Transformer
*Secondary equivalent circuit, Es=-34KV
*Wire copper loss
Rcp 1 7 10
*Leakage Inductance
Ll  7 2 100E-6
*Core Shunt Loss
Rsh 1 0 6.6E4
*Charging Inductance
Lch 7 11 1.5E-5
*Transformer Capacitance
Cd 11 0 1.25E-10
Cs 2 0 85E-12
*----------------
*Corner Cutter
D1  3 2 D6537S
R1  3 4 50
C1  4 0 702E-12
R2  4 5 102.3E3
D2  5 0 D1N5388S; 23.4kV
R5  4 0 47E6
*-----------------
*Initial RRV Control
C2  2 8 100E-12
D3  2 8 D6537S
```

Figure 3.2.1

```
*DUMP
R3   8 9 113.5
C3   8 9 272E-9
R4   9 0 113.5
C4   9 0 272E-9
*------------------
* Simulated Magnetron ?
D4   10 2 DMAG
Vs   12 10 32.0E3
Cmag   2   12 25E-12
*------------------
Vx   0 12 DC 0v; To measure current
*------------------
*MODELS
.MODEL D6537S D(IS=100E-15 RS=16 CJO=2PF TT=12NS BV=50E3 IBV=100E-15)
.MODEL D1N5388S D(IS=0.5UA RS=400 BV=23.4E3 IBV=0.05UA)
.MODEL DMAG D(IS=250mA RS=27 VJ=0.6 N=3 CJO=1PF XTI=2 TT=10NS BV=60E3 IBV=100E-2)
.TRAN 10E-9 80E-3
.PROBE
.END
```

Figure 3.2.2

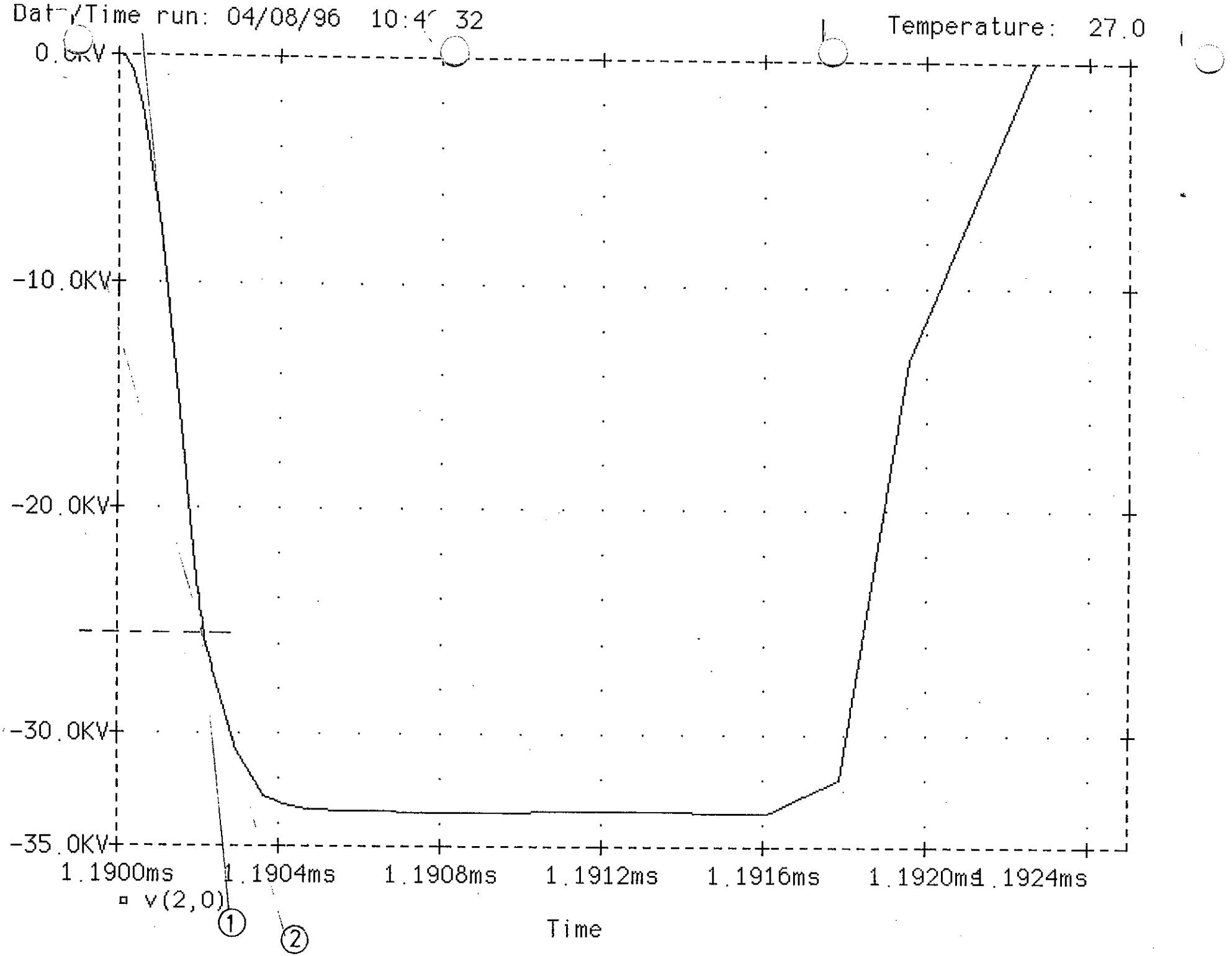

Dat /Time run: 04/08/96 10:4 32
Temperature: 27.0
0.0KV
-10.0KV
-20.0KV
-30.0KV
-35.0KV
1.1900ms
1.1904ms
1.1908ms
1.1912ms
1.1916ms
1.1920ms
1.1924ms
v(2,0)
Time

Figure 3.3

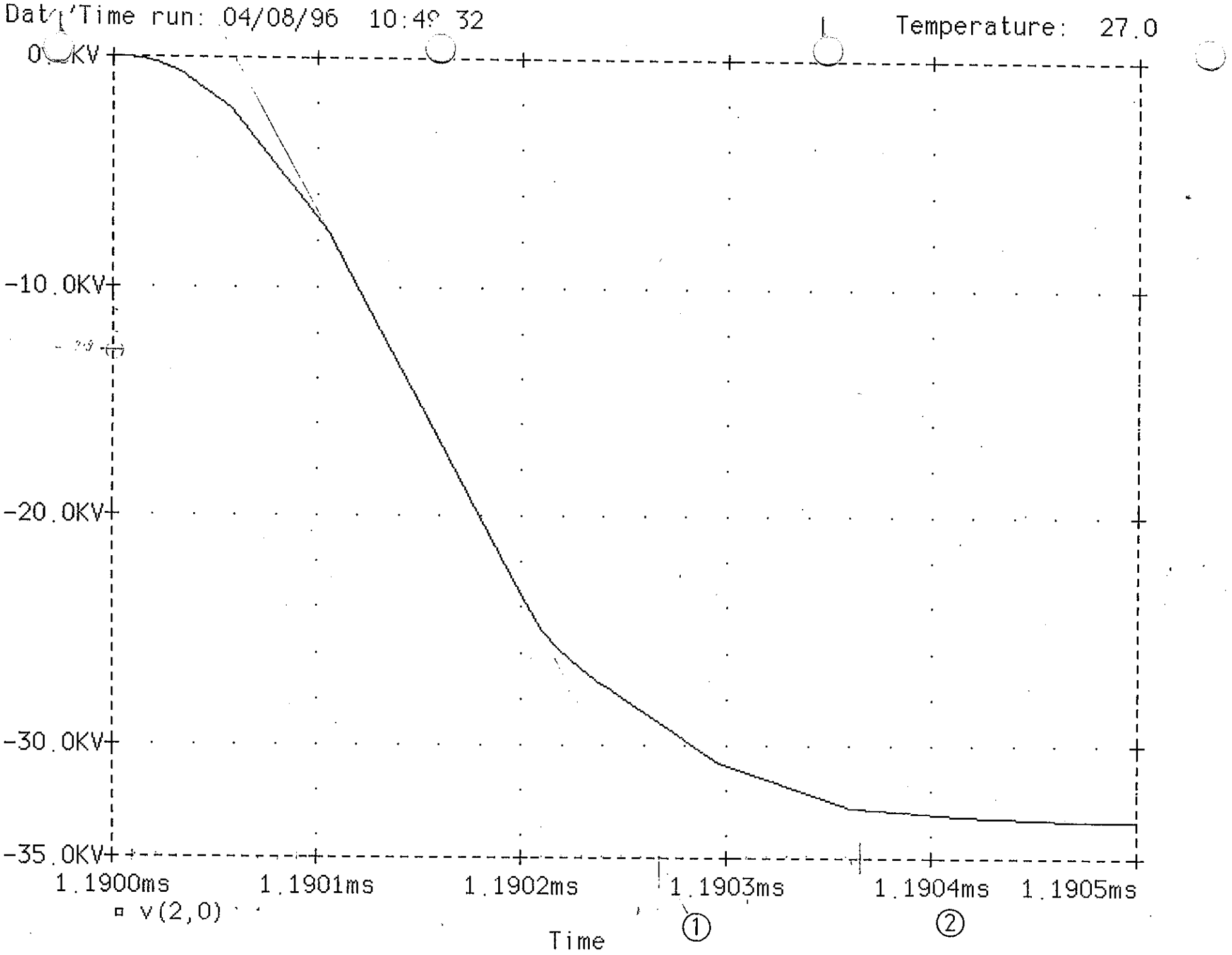

Date/Time run: 04/08/96 10:49:32
Temperature: 27.0
0.0KV
-10.0KV
-20.0KV
-30.0KV
-35.0KV
1.1900ms
1.1901ms
1.1902ms
1.1903ms
1.1904ms
1.1905ms
V(2,0)
Time
1
2

Figure 3.4

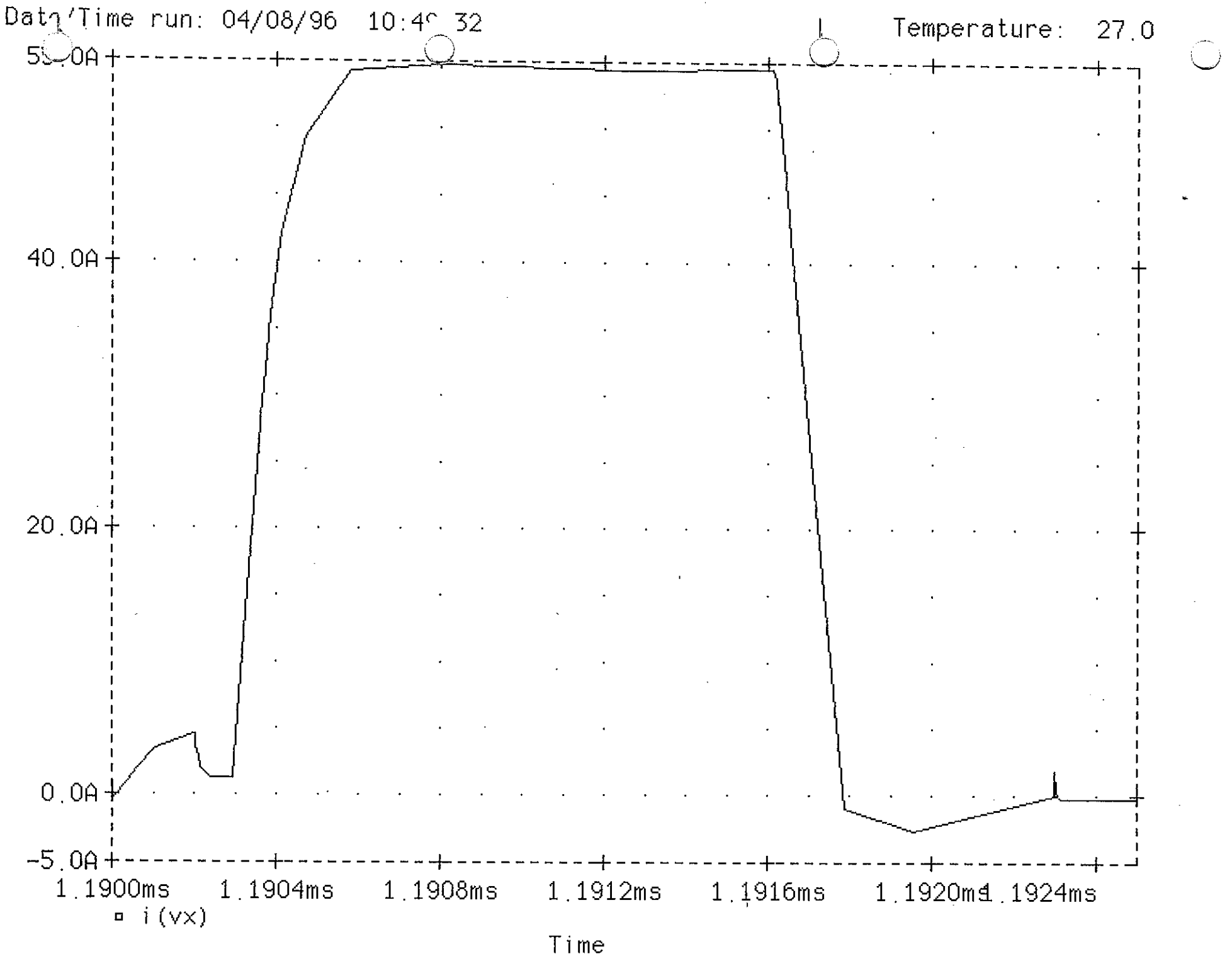

Data/Time run: 04/08/96 10:4? 32
Temperature: 27.0
40.0A
20.0A
0.0A
-5.0A
1.1900ms
1.1904ms
1.1908ms
1.1912ms
1.1916ms
1.1920ms
1.1924ms
i(vx)
Time

Figure 3.5

3.6.3 Selection of Capacitors

Rather than going for expensive single unit high voltage capacitors, the required capacitors have been made up of a number of low cost capacitors connected in a series arrangement. To achieve voltage sharing between the individual capacitors, resistors and diodes have been used. Voltage sharing is also improved by the use of 2.5% tolerance capacitors.

Due to the very high transient currents to be passed by the capacitors, making up C1 and C2 in particular, WIMA FKP1 type capacitors have been selected, having low inductance and specifically designed for very high pulse currents.

3.6.4 C1

The final required capacitance value for C1 was found to be 702.13pF, made up using 47 discrete FKP1/1250v capacitors. The original initial value for C1 was 1nF. The change of C1 value yielded a significant reduction in power dissipation in the corner cutter. Most of the power dissipation in the corner cutter is when C1 having charged up to V_k=34kV during a pulse, then discharges to V_z=23.4kV via R2 and D2 zener stack. Note, the zener stack voltage of 23.4kV was determined by dynamic tuning using Appendix 3 test method, and gave the best jitter performance. The reduction in power dissipation is calculated as follows:-

With C1 = 1nF The ΔW energy exchange from C1 to R2/D2 network:-

$$\Delta W = 0{\cdot}5C_1(V_k)^2 - 0{\cdot}5C_1(V_z)^2 \qquad (3.6.4.1)$$

$$\Delta W = 0{\cdot}5.1.10^{-9}(34.10^3)^2 - 0{\cdot}5.1.10^{-9}(23{\cdot}4.10^3)^2 \qquad (3.6.4.2)$$

$$\Delta W = \underline{0{\cdot}30422} \text{ Joules.} \qquad (3.6.4.3)$$

Power = Joules x PRF

$$\text{Power} = 0{\cdot}30422.840 = \underline{255{\cdot}5} \text{ Watts.} \qquad (3.6.4.4)$$

With C1 = 702·13pF

The ΔW energy exchange from C1 to R2/D2 network:-

$\Delta W = 0{\cdot}5C_1(V_k)^2 - 0{\cdot}5C_1(V_z)^2$

$\Delta W = 0{\cdot}5.702{\cdot}13.10^{-12}(34.10^3)^2 - 0{\cdot}5.702{\cdot}13.10^{-12}(23{\cdot}4.10^3)^2$ (3.6.4.5)

$\Delta W = \underline{0{\cdot}21360}$ Joules. (3.6.4.6)

Power = 0·21360.840 = $\underline{179{\cdot}43}$ Watts. (3.6.4.6)

C1 at 702·13pF reduced the power dissipation by 76 Watts. (3.6.4.7)

Should the corner cutter be operated at the maximum PRF of 1500Hz, the dissipation in the R2/D2 network would increase to:-

0·21360.1500 = $\underline{320{\cdot}4}$ Watts. (3.6.4.8)

3.6.5 The maximum DC operating voltage of the C1 network is:-

$V_{DCmax} = 47 \times V_r$ Where V_r is the rated voltage of each capacitor.

$V_{DCmax} = 47 \times 1250 = \underline{58{\cdot}75}$ kV. (3.6.5.1)

Selection of 1250VDC V_r adequate, and specifying 2·5% Tolerance to improve voltage sharing. The PVCU is protected at its HT input by a 40kV Spark Gap. When the PVCU is operating the peak voltage across the C1 network is -34kV, therefore yielding 34/47 kV = $\underline{723{\cdot}4}$ volts peak across each capacitor. (3.6.5.2)

Using PSPICE the RMS voltage across the C1 network was computed to be:-

V_{C1rms} = $\underline{23{\cdot}8}$ kV rms. See Figure 3.6.

Predicting a V_{rms} across each capacitor of: $23{\cdot}8.10^3)/47 = \underline{506{\cdot}38}$ V_{rms} (3.6.5.3)

3.6.6 The result (3.6.5.3) has an impact on the maximum peak pulse current capability of the FKP1 capacitors. From the WIMA FKP1 data sheets, the rated $\delta V/\delta t$ MAX with the capacitors operating at the rated V_r = 1250V is 1200V/μs.

The $\delta V/\delta t$ MAX rating is enhanced by operating at less than V_r (1250VDC).

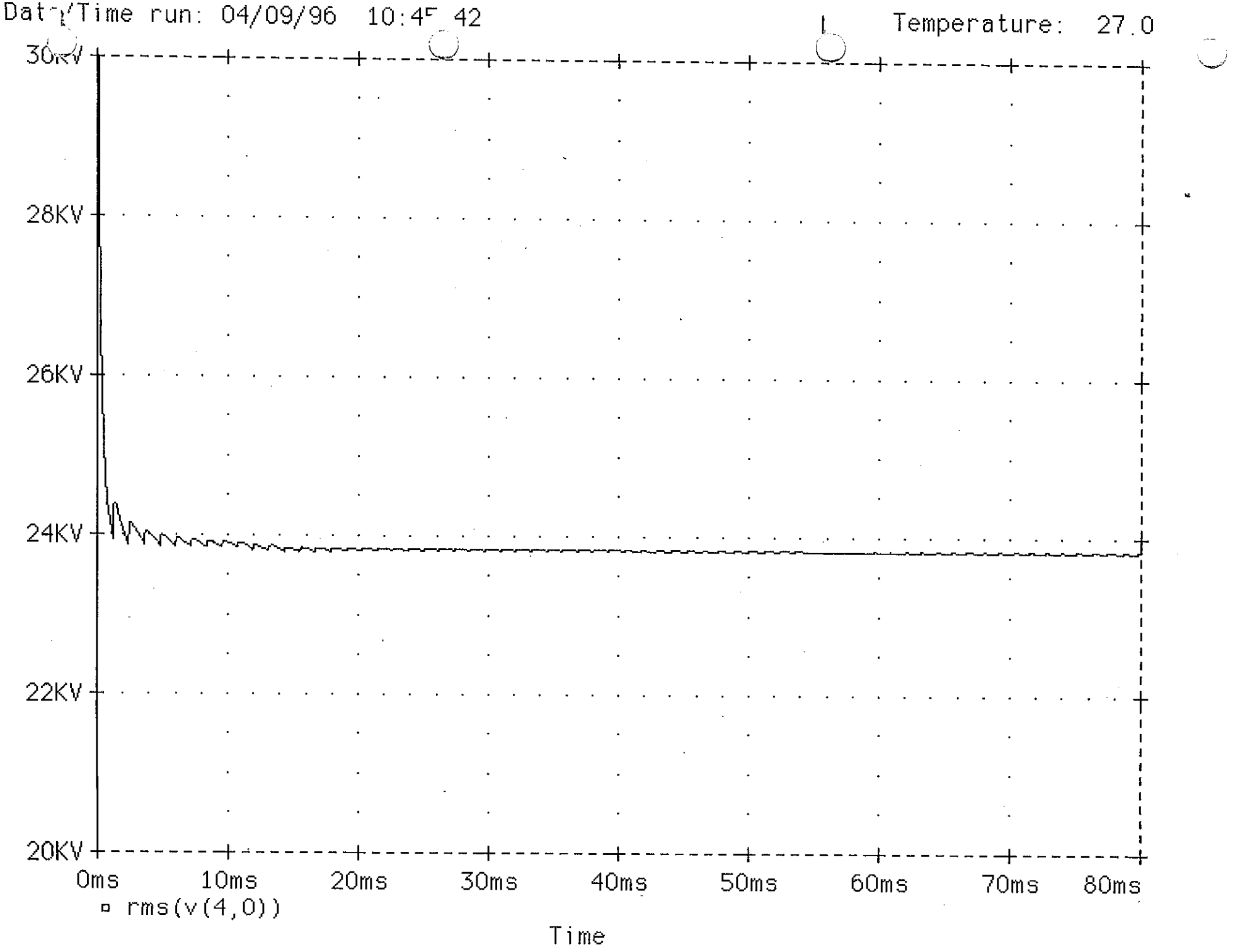

Date/Time run: 04/09/96 10:45:42
Temperature: 27.0
30KV
28KV
26KV
24KV
22KV
20KV
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
rms(v(4,0))
Time

Figure 3.6

3.6.7 From the WIMA FKP1 data sheet, the enhancement in $\delta V/\delta t$ (F_{MAX}) is derived using:-

$$F_{MAX} = (V_r/V_{OPERATING}) \times F_r \quad \text{Where } F_r = 1200 \text{ V}/\mu\text{s}. \quad (3.6.7.1)$$

Therefore:-

$$F_{MAX} = (1250/506{\cdot}38).1200 \quad (3.6.7.2)$$

$$F_{MAX} = \underline{2962{\cdot}2} \text{ V}/\mu\text{s}. \quad (3.6.7.3)$$

When the PVCU is operating the worse case of $\delta V/\delta t$ is found during the first modulator pulse, when C1 is charging up for the first time. After the first pulse C1 charges from V_z to V_k.

Using PSPICE to predict the rate of rise on C1 during the first pulse gave the result shown in Figure 3.7. From the graph, the rate was measured to be 36kV in $0{\cdot}7\mu$s. Which is $\underline{51{\cdot}4}$ kV/μs. (3.6.7.4)

Each of the 47 capacitors will experience:

$$F_{OPERATING} = 51{\cdot}4.10^3/47 \text{ V}/\mu\text{s} \quad (3.6.7.5)$$

$$F_{OPERATING} = \underline{1094} \text{ V}/\mu\text{s}. \quad (3.6.7.6)$$

The result (3.6.7.6) $\delta V/\delta t$ is significantly lower than the F_{MAX} (3.6.7.3) result and lower than F_r (1200 V/μs).

3.6.8 The F_{MAX} $\delta V/\delta t$ is used to determine the maximum peak pulse current that can be displaced through each capacitor in C1 network:-

The WIMA FKP1 data sheet provides the formula:-

$$I_{PK,MAX} = F \times C \times 1{\cdot}6 \quad \text{Where C is in } \mu\text{F} \quad (3.6.8.1)$$

& I is in Amps.

$$I_{PK,MAX} = F_{MAX}.0{\cdot}033.1{\cdot}6 \quad (3.6.8.2)$$

$$I_{PK,MAX} = 2962.0{\cdot}033.1{\cdot}6 = \underline{156{\cdot}39} \text{ Amps peak.} \quad (3.6.8.3)$$

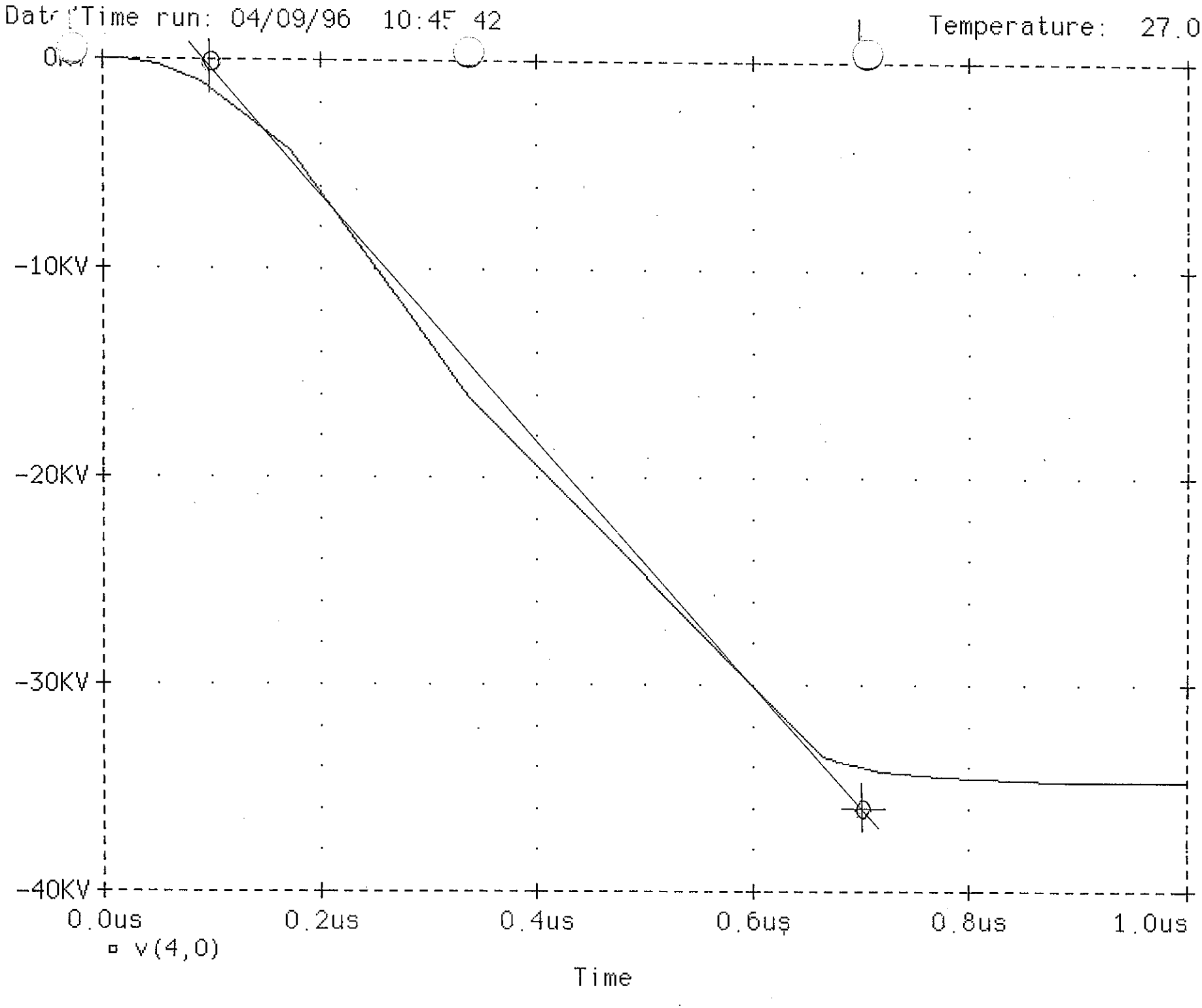

Date/Time run: 04/09/96 10:45:42
Temperature: 27.0
0V
-10KV
-20KV
-30KV
-40KV
0.0us
0.2us
0.4us
0.6us
0.8us
1.0us
V(4,0)
Time

Figure 3.7

3.6.9 Using PSPICE the peak current in C1 was plotted and peaks at 64 Amps. See Figure 3.8. Peak pulse amplitudes after the first pulse are 40 Amps.

The peak current in C1 (and through D1 & R1) is limited not only by the value of R1 and dynamic impedance of D1, but also the effective source impedance of the 34kV pulse.

The rates of rise measured in the S2055 reference equipment are less than those indicated in Figure 3.4 therefore the actual transient peak current in C1 will be less than that derived by PSPICE.

The peak current capability of the FKP1 capacitors chosen for the C1 network is considered satisfactory.

3.6.10

C1 is formed using 47 capacitors connected in series. Across each capacitor a 1MΩ/1Watt resistor is fitted to provide voltage sharing. This effectively places a 47 MΩ load across C1.

The C1 ,C/R series network and all other networks have been deliberately laid out in a snake fashion, so as to reduce stray inductance. See photograph 3.P.2.

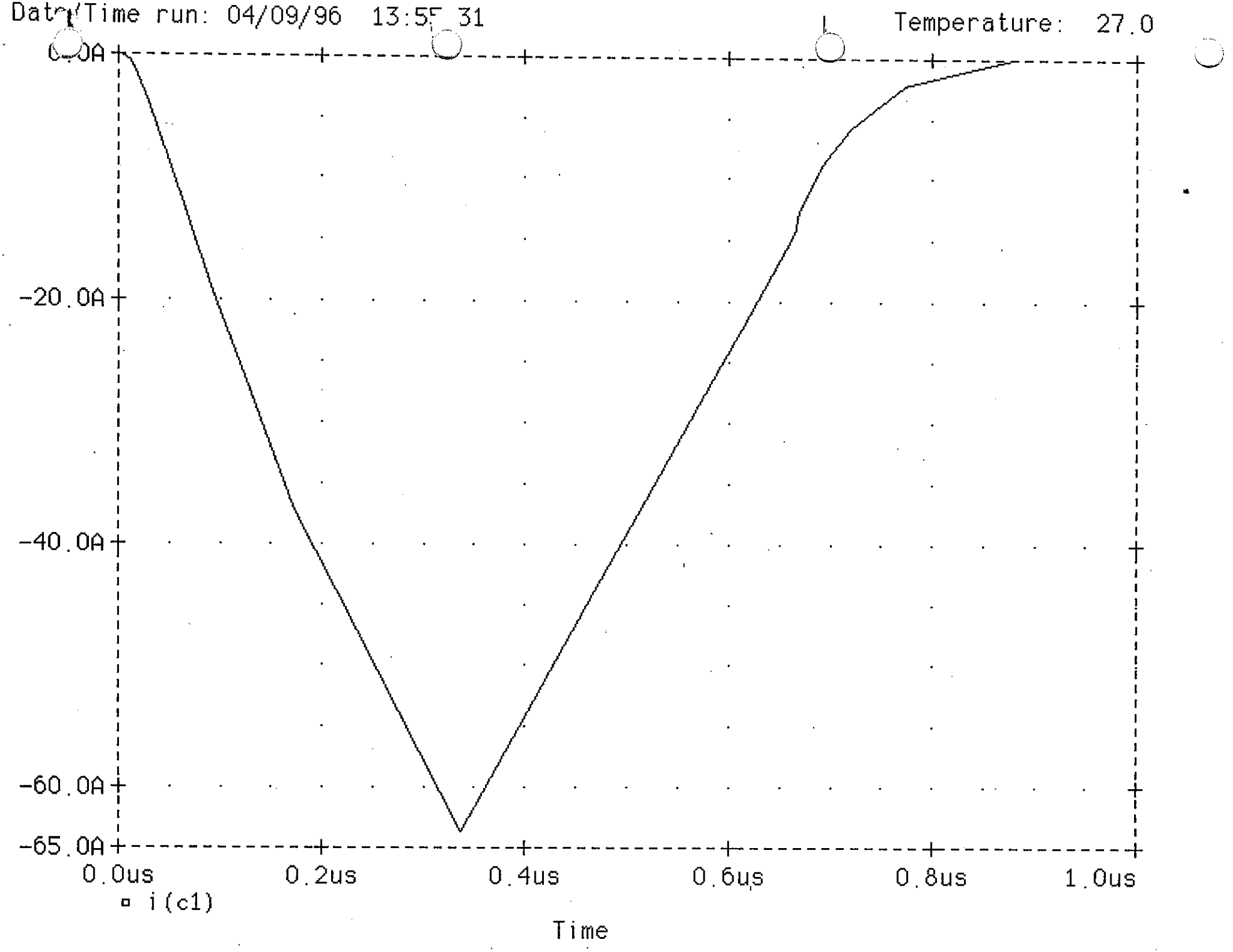

Date/Time run: 04/09/96 13:55:31
Temperature: 27.0
0.0A
-20.0A
-40.0A
-60.0A
-65.0A
0.0us
0.2us
0.4us
0.6us
0.8us
1.0us
i(c1)
Time

Figure 3.8

3.7.1 R1

The purpose of R1 is to provide a load to dissipate the power of the high frequency components of the cathode pulse as required to achieve the secondary lower rate of rise when D1 is conducting.

The type of resistors chosen to form the R1 network are Hot Moulded Carbon Composition types in order to achieve low inductance and ability to withstand high transient peak energy.

3.7.2 Using the PSPICE, the RMS current in R1 was computed to be 0·45 Amps. See Figure 3.9.

The RMS Power in R1 = $(0{\cdot}45)^2.50$ = 10·125 Watts.

The peak transient current was predicted to be 41 Amps. See Figure 3.10.

The current transient is due to C1 charging from -23·4kV to -34kV.

When the voltage on C1 approaches the magnetron cathode potential -34kV, D1 rapidly switches off.

3.7.3 In order to dissipate the power and withstand the peak transient voltage, R1 is formed by 15 x 30Ω, 2 Watt resistors connected in a series/parallel arrangement to obtain the 50Ω required.

The power dissipation in each 30Ω resistor = 10·125/15 = 0·675 Watts.

3.7.4 Using the formula $E_{MAX} = \sqrt{PR}$ to determine the RMS voltage rating of the resistors used:- $E_{MAX} = \sqrt{2.30}$ = 7·746 volts

Using PSPICE the RMS voltage across the R1 network is computed to be 23 volts. See Figure 3.11.

The network is arranged as 5 x (3x30Ω in parallel) in series, therefore the RMS voltage across each set of 3 30Ω resistors is 23/5 = 4·6 volts.

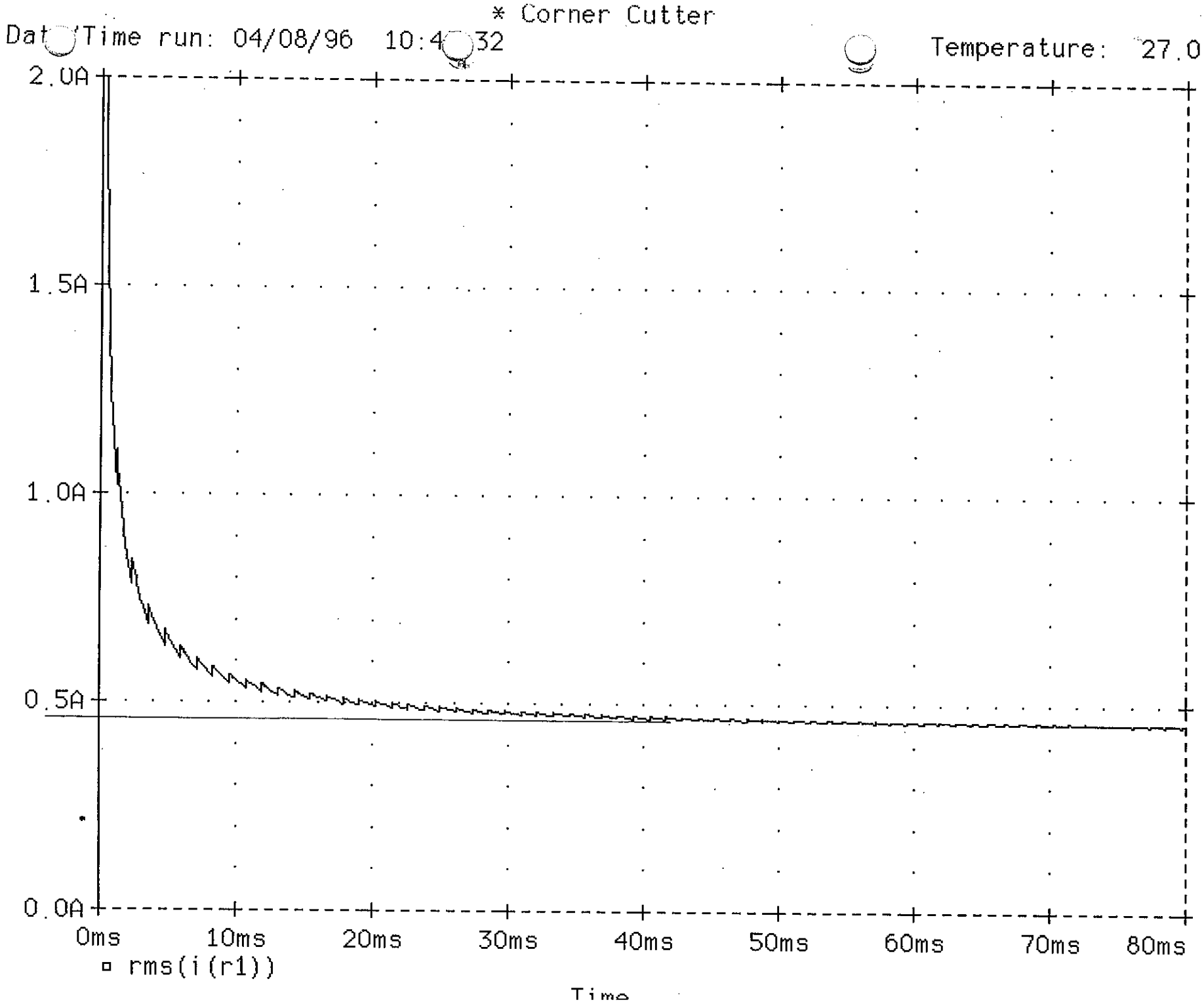

* Corner Cutter
Date/Time run: 04/08/96 10:4 32
Temperature: 27.0
2.0A
1.5A
1.0A
0.5A
0.0A
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
rms(i(r1))
Time

Figure 3.9

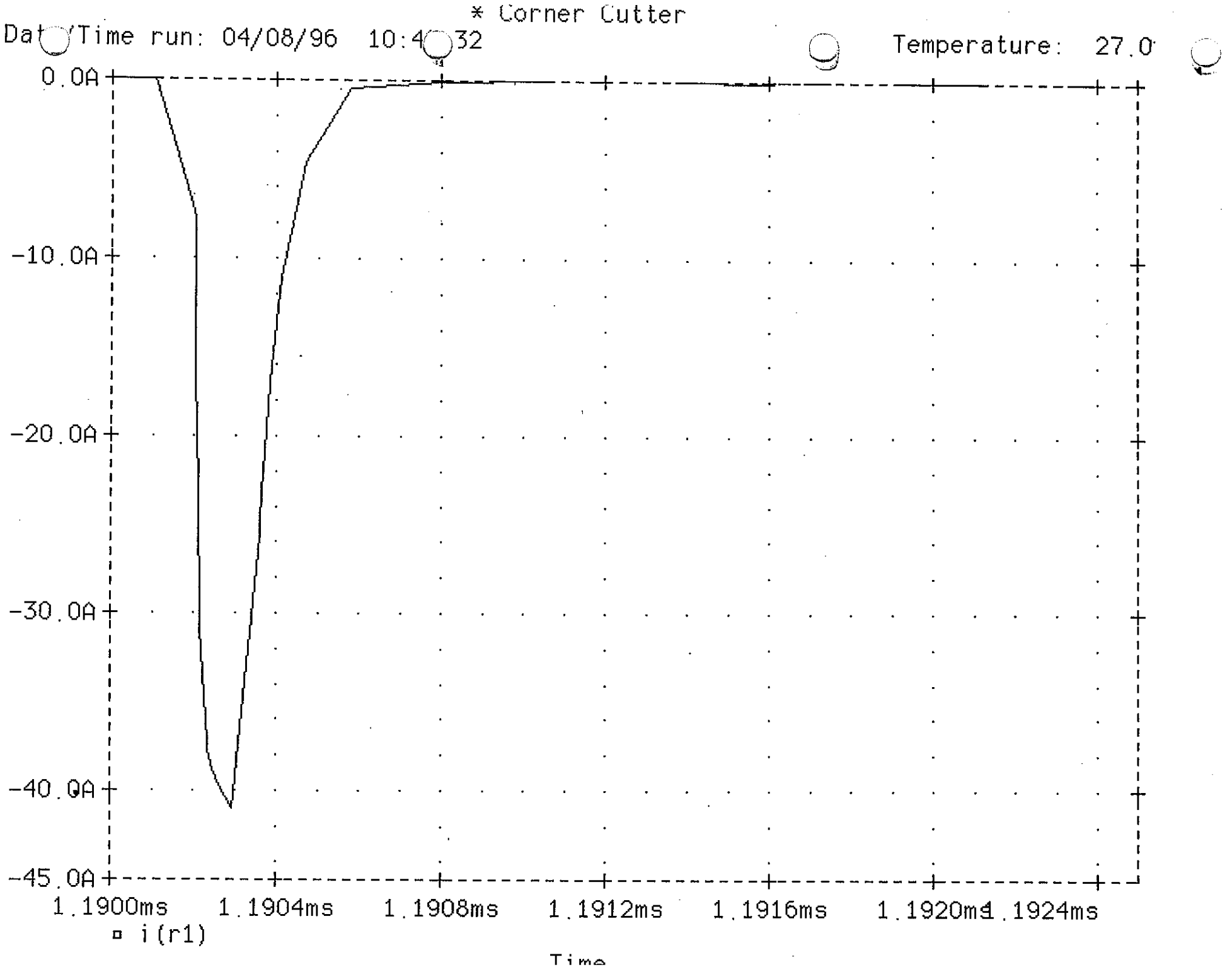

* Corner Cutter
Date/Time run: 04/08/96 10:4 32
Temperature: 27.0
0.0A
-10.0A
-20.0A
-30.0A
-40.0A
-45.0A
1.1900ms
1.1904ms
1.1908ms
1.1912ms
1.1916ms
1.1920ms
1.1924ms
i(r1)
Time

Figure 3.10

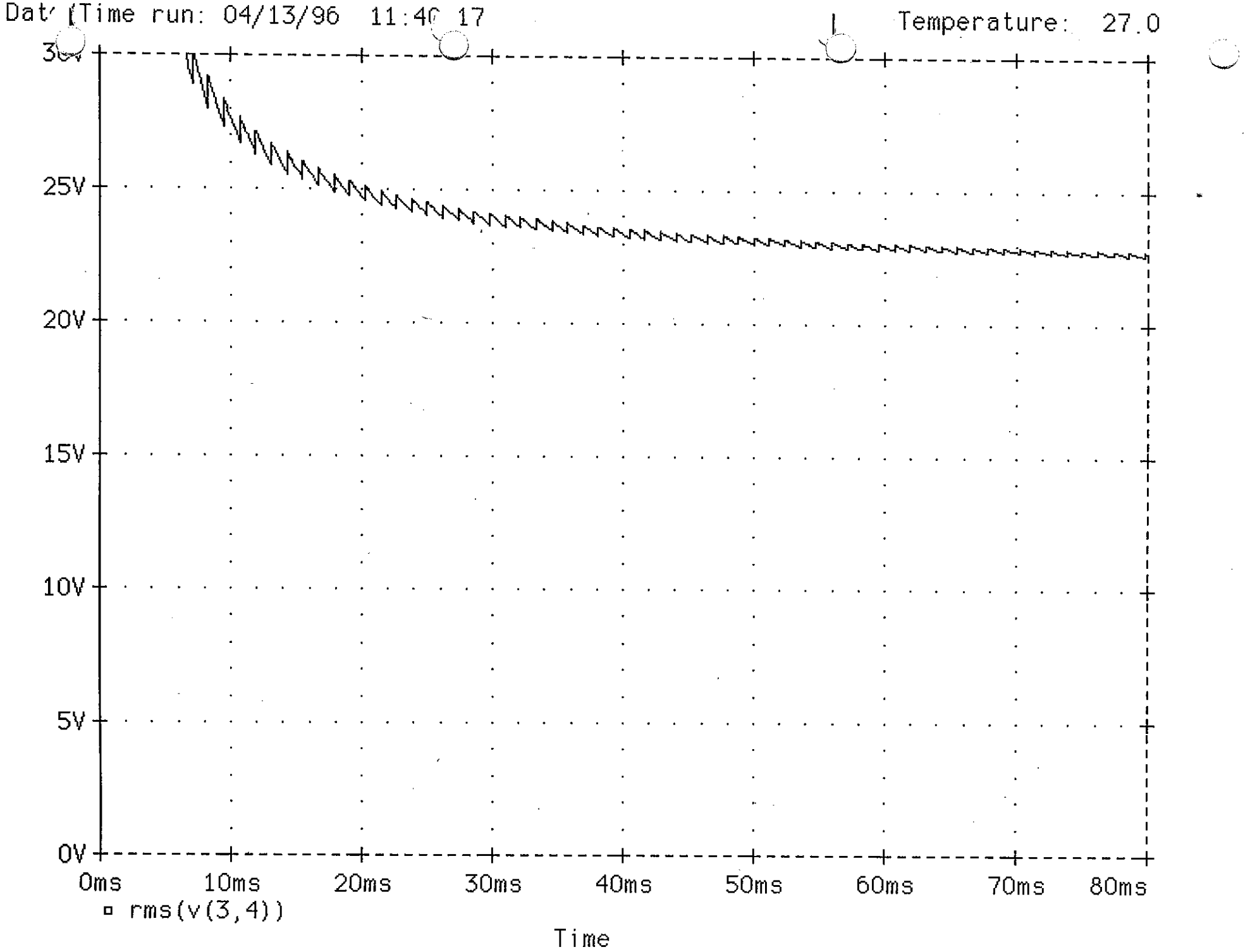

Dat (Time run: 04/13/96 11:40 17
Temperature: 27.0
30V
25V
20V
15V
10V
5V
0V
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
rms(v(3,4))
Time

Figure 3.11

3.8 D1

A fast 50kV PIV diode was required for D1.

The corner cutter used in the magnetron manufacturers modulator test rig uses 5 high voltage diode stacks, connected in series. To reduce cost, inductance and achieve a more compact arrangement it was decided to have a 25 kV PIV stack manufactured specially for the S2055 corner cutter, by SEMTECH. The diode stack has a rating of 2.5 Amps(average),fast recovery (150ns) and is designed to withstand the transient peak current levels. The diode type SG6537 is registered for GEC-MARCONI use only.

Two of the 25kV stacks have been connected in series to achieve the 50kV PIV required.

3.9 R2

The value of R2 was chosen to ensure that at the highest PRF 1500 Hz (PRI 666·6'μS) C1 fully discharges from 34kV to the zener stack voltage 23·4kV.

Neglecting the dynamic impedance of the zener stack initially:

and using Time = 5 x $C_1.R_2$ ie 5 time constants (3.9.1)

$$R_2 = 667.10^{-6}/ (5.702.10^{-12}) \quad (3.9.2)$$

$$R_2 = \underline{190}\ k\Omega\ MAX \quad (3.9.3)$$

R2 needed to be less than 190 kΩ, so it was decided to form R_2 using 31 3k3/2W hot moulded carbon composition (to reduce inductance and withstand high transient peak power) giving a total resistance of 102·3 kΩ(3.9.4).

The discharge current in **R2-D2** network is due to C1 discharging from -34kV to -23·4kV in-between modulator pulses at the PRF of 840 Hz (1500 Hz worse case). The transient current pulse whilst the cathode voltage pulse is present and the current discharge via the 47MΩ voltage sharing resistors may be neglected.

The mean current $I_{MEAN} = C.(dV/dt)$ (3.9.5)

and as $1/dt = PRF = 840$ Hz (3.9.6)

$$I_{MEAN} = C.dV.PRF \quad (3.9.7)$$

Therefore $I_{MEAN} = 702.10^{-12}.(34.10^3 - 23{\cdot}4.10^3).840 = \underline{6{\cdot}25}$ mA. (3.9.8)

(approximately the same as the PSPICE result Figure 3.12)

and $I_{MEAN} = 702.10^{-12}.(34.10^3 - 23{\cdot}4.10^3).1500 = \underline{11{\cdot}16}$ mA worse case. (3.9.9)

The total mean power in $R_2 = I^2.R_2 = (6{\cdot}25.10^{-3})^2.102{\cdot}3.10^3 = \underline{4}$ Watts. (3.9.10)

and $=(11{\cdot}16.10^{-3})^2.102{\cdot}3.10^3 = \underline{12{\cdot}74}$ Watts worse case. (3.9.11)

Therefore power in each resistor $=4/31 = \underline{0{\cdot}13}$ Watts.

Worse case $12{\cdot}74/31 = \underline{0.4}$ W (3.9.12)

3.10 D2 ZENER STACK

A 23·4 kV zener diode was required to set the bias on C1 which determines the cathode voltage at which D1 starts to conduct, to cause the rate of rise change. The zener network had to be capable of dissipating the maximum power of 320·4 W determined in para 3.6.4.8, where Surveyor is operated at 1500 Hz PRF. During the development phase it was necessary to adjust the total zener voltage to achieve best jitter performance.

For reasons of low cost, ease of adjustment and spreading the power dissipation it was decided to form the zener stack using a large number of discrete zeners.

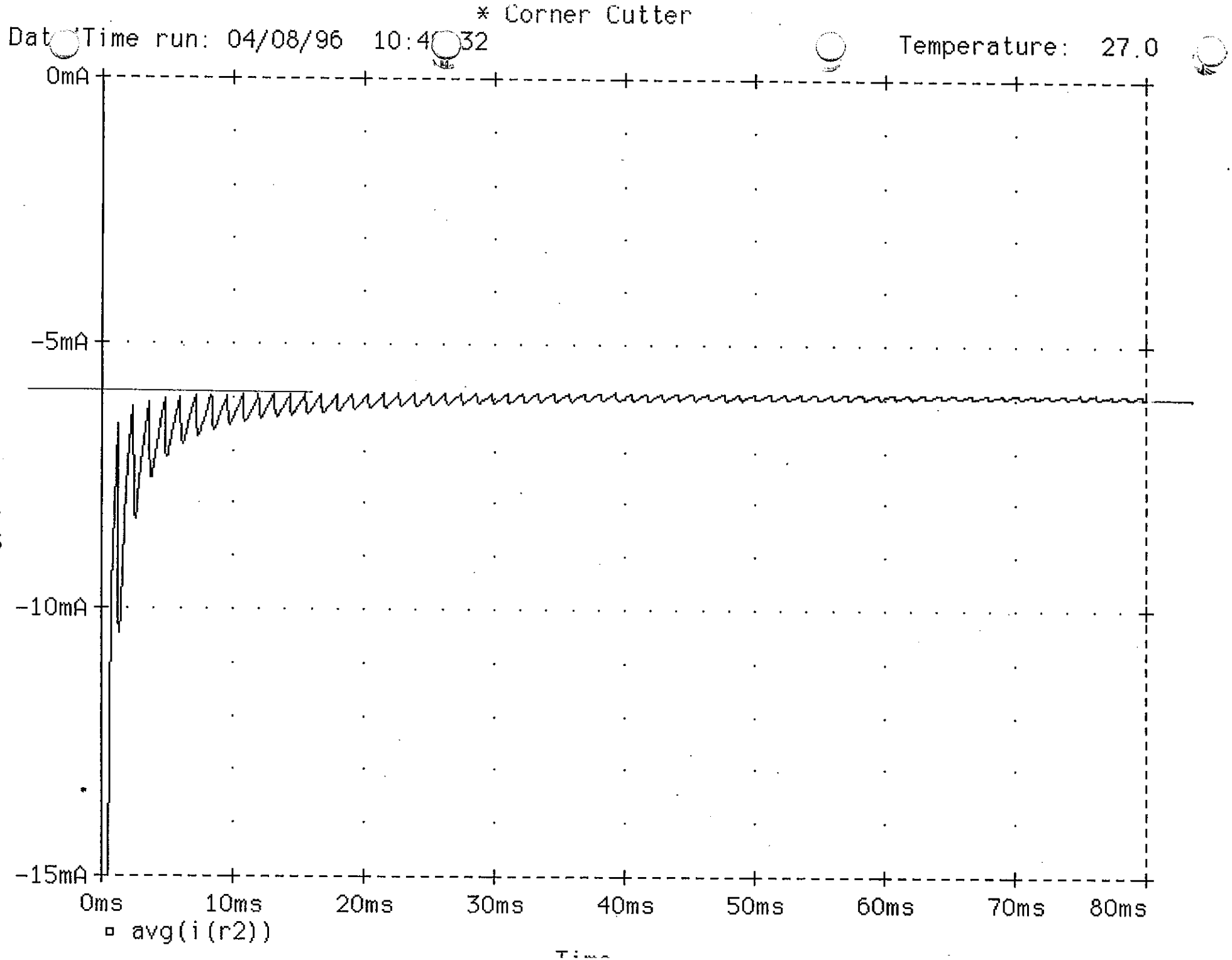

* Corner Cutter
Date/Time run: 04/08/96 10:40:32
Temperature: 27.0
0mA
-5mA
-10mA
-15mA
0ms
10ms
20ms
30ms
40ms
50ms
60ms
70ms
80ms
avg(i(r2))
Time

Figure 3.12

The manufacturers of the magnetron use an oil filled corner cutter, employing approximately 123 Unitrode UZ5119(190v) 5 Watt zener diodes to form the zener stack. The UZ5119 zeners cost approximately £7 each, therefore would cost £862 in the Surveyor corner cutter. A search was made to find a lower cost zener diode with equivalent or better parameters for the application.

The zener diode selected is a 1N5388B(200v) 5 Watt zener costing only **11 pence**.

Total cost of D2 = 117 x 11 pence = £12.87.

3.11 Power Dissipation

The worse case power dissipation in the zener stack is:

P_{MAX} = 320·4 W - 12·74 W = 307·66 Watts (PRF at 1500 Hz) (3.11.1)

This power dissipation is independent of transmitter pulse width.

Assuming that the total power is equally divided between the 117 zeners:

Power in each zener = 307·66/117 = 2·63 Watts (worse case). (3.11.2)

In all Surveyors manufactured to date operating at 840 Hz PRF:

P_{MAX} = 179·43 W - 4 W = 175·43 Watts (3.11.3)

Power in each zener = 175·43/117 = 1·5 Watts. (3.11.4)

3.12 Cooling

The zeners are rated at 5 Watts and are mounted as shown in 3.P.1 and 3.P.2 (pages 98 & 99), raised off the PEC to prevent hot spots. All of the components are mounted on the insides of the PEC's to form a vertical tunnel. Two axial fans are fitted in the base of the unit to force cooling air up through the components, not only to reduce the body temperature of components but to purge the unit of ions. A trial was conducted to monitor the temperature of the metal lead adjacent to the body of a zener, the maximum recorded was 33°C above ambient.

3.13.1 Performance The performance of the PVCU was evaluated by:

a, Measurement of the rates of rise of the front edge of the cathode voltage pulse, achieved on a production S2055 transmitter.

b, Jitter performance measurements carried out as described in Appendix 3.

3.13.2 Rates of Rise

The waveform below was monitored at the input of the PVCU (magnetron cathode) using a Capacitor Divider Potentiometer (Scaling Factor 1.5 kV/volt).

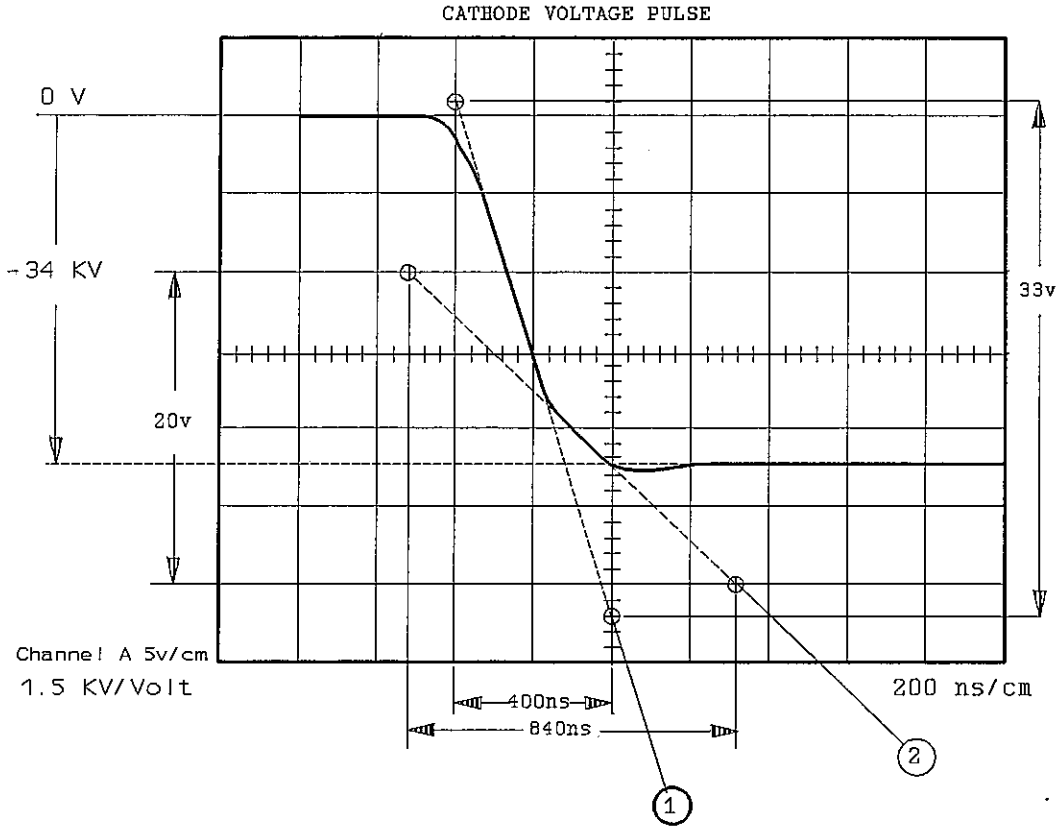


Figure 3.13

The waveform shown in Figure 3.13 is a precision copy from a photograph and not idealised. The primary and secondary rates of rise can be seen clearly indicated by lines 1 and 2 respectively. The rates are measured between the circle markers on the lines:

1 Primary Rate of Rise: (33 x 1·5.10^3 volts) in 400 ns

= 49·5 kV in 400 ns

= (49·5 kV x 2·5) kV/μs

= <u>123·75</u> kV/μs.

Specification required by valve manufacturer: 100 to 150 kV/μs.

2 Secondary Rate of Rise: (20 x 1·5.10^3 volts) in 840 ns

= 30 kV in 840 ns

= (30 kV x 1.19) kV/μs

= <u>35·7</u> kV/μs.

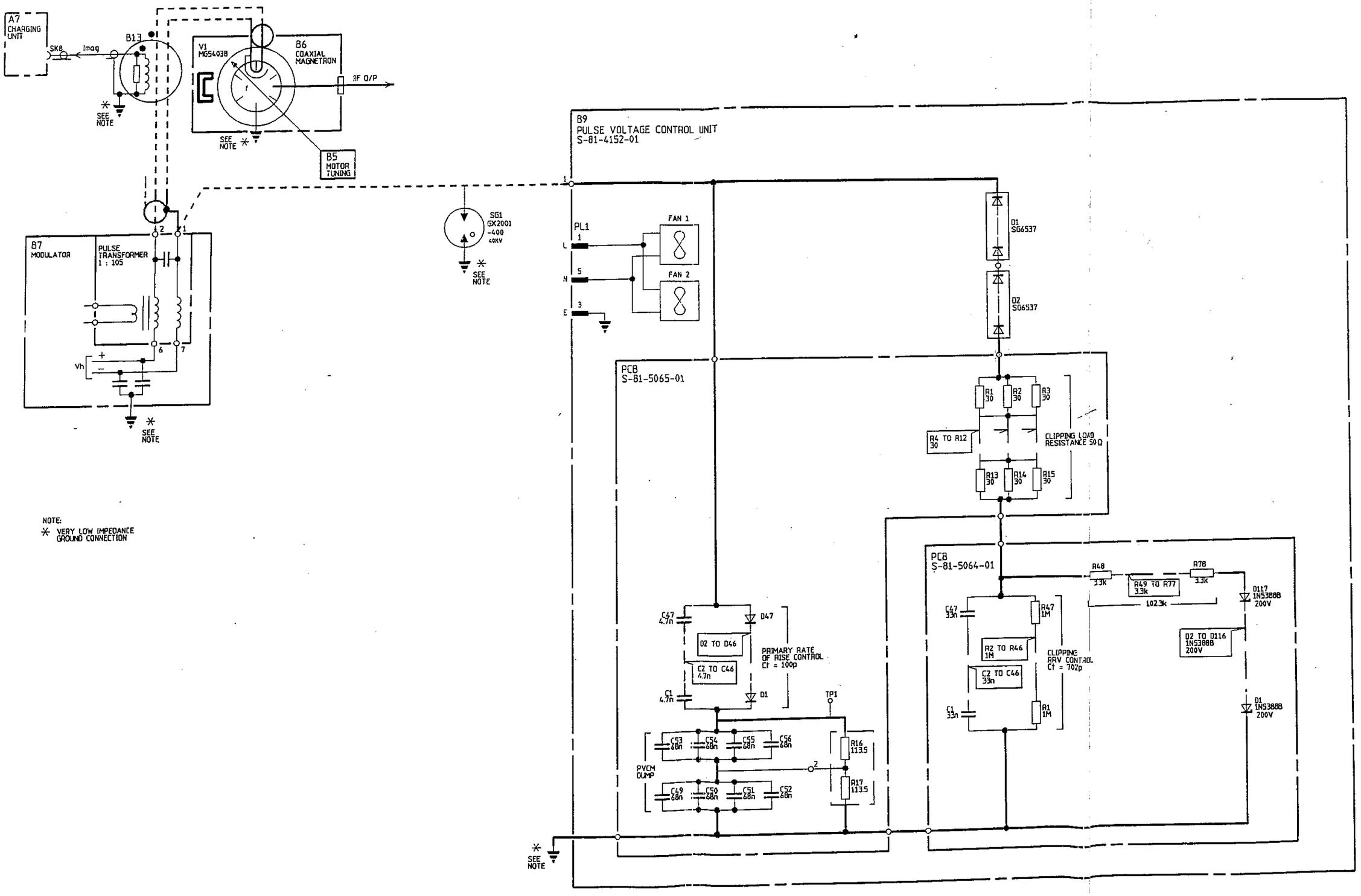
Specification required by valve manufacturer: 30 to 60 kV/μs.

3.13.3 Jitter Performance

The values of C1 network, C2 network and the corner cut threshold voltage (Number of zeners) have been optimised to achieve the lowest jitter (standard deviation SD).

Jitter performance measurements have been carried out with 3 magnetrons and have yielded a range of jitter SD between 890 ps and 6 ns across the band 2.7 to 2.9 GHz. The average of the results were in the order of 2.5 ns, only one case at 6 ns. (with PRF stagger +/-14%).

3.13.4 The full circuit of the PVCU is shown in Figure 3.14:



NOTE:
* VERY LOW IMPEDANCE GROUND CONNECTION

Figure 3.14 Pulse Voltage Control Unit S-81-4152-01 : Circuit

4 Conclusions

4.1 The design aims for the SURVEYOR performance have been achieved, due to the high stability (Jitter & Frequency) of the transmitted RF pulse from the S2055 transmitter.

The Overall MTI I/F of SURVEYOR (Reference Equipment) has been measured independently by Dr D. Heath, Future Systems, GEC-MARCONI, and proved to be approximately 50 dB. The results of the measurements carried out are included in Appendix 5.7. The work carried out by Dr D. Heath indicated that modification to the AFC control was necessary in order to consistently achieve 50 dB, which has since been carried out. The AFC now tunes the magnetron to give an IF closer to 45 MHz. It was also found that a flexible drive shaft between the AFC Motor and tuning shaft on the magnetron, was the cause of erratic tuning due to friction between the inner drive cable and an outer sleeve. The cable has now been replaced with a stainless steel straight telescopic drive shaft which provides smooth tuning.

4.2 Frequency Stability

The improvement in frequency stability as a result of modulator HT Stabilization and magnetron frequency pushing has surpassed the design aim. HT stability over any 4 consecutive pulses is better than 20 mV (typically 10 mV) in 350v with PRF Stagger switched ON. The modulation in magnetron cathode current is in the order of 10·4 mA Pk-Pk which produces a frequency modulation of 156 Hz Pk-Pk (26 Hz SD). 26 Hz SD gives a $I_{\Delta f}$ of 77.7 dB contribution.

4.3 Jitter Stability.

The improvement in jitter stability on the front edge of the RF pulse as a result of the new PVCU (magnetron cathode voltage rate of rise control) and the new MCHC (magnetron cathode heater controller) has met the design aim.

The average jitter (Standard Deviation) obtained is 2 ns which gives a I_{pwj} of 58 dB. The average figure is based on test results from 3 magnetrons, 2 development and one production.

4.4 Typical Waveforms taken from a production S2055 on test:

RF Pulse **Figures 4.1, 4.2, 4.3 and 4.4**

Spectrum **Figures 4.5, 4.6 and 4.7**

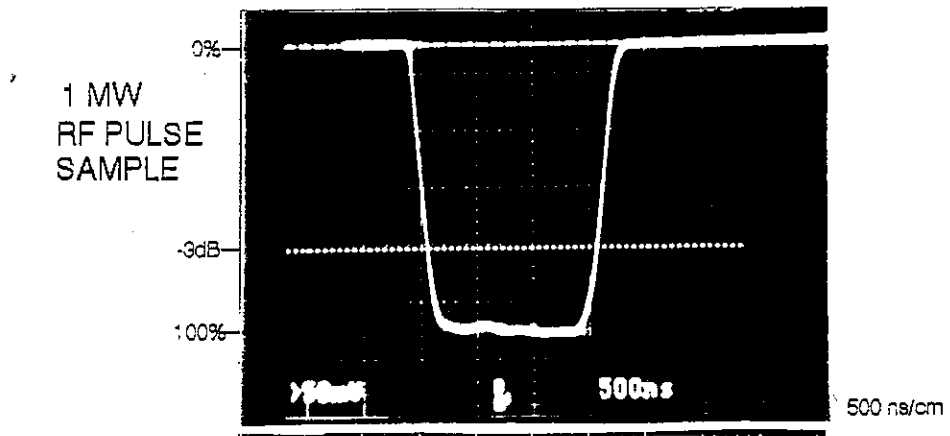


Figure 4.1

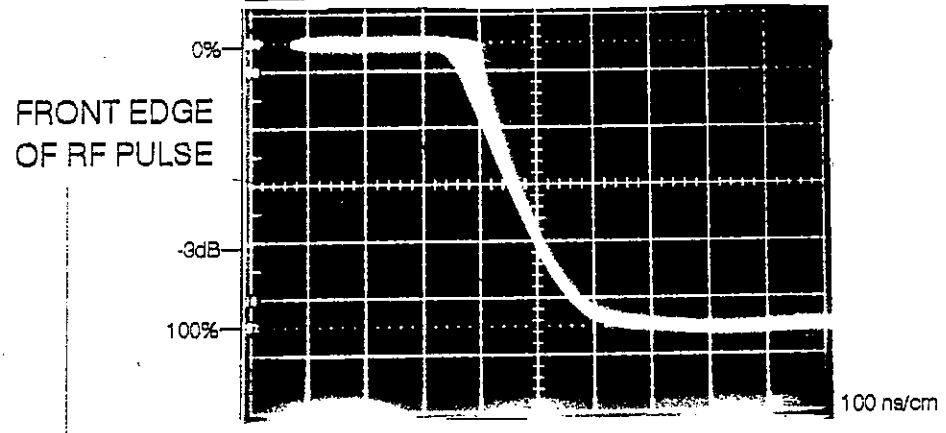


Figure 4.2

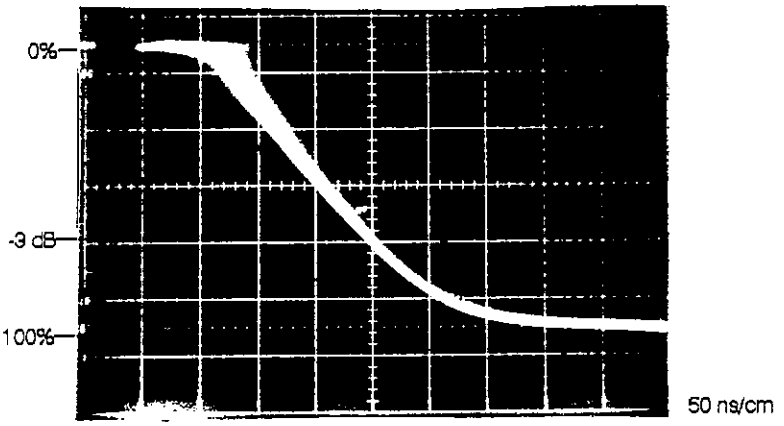


Figure 4.3

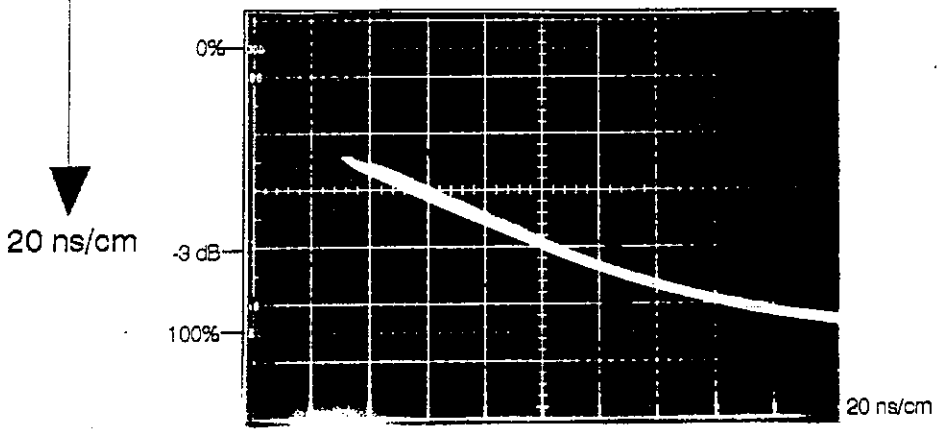


Figure 4.4

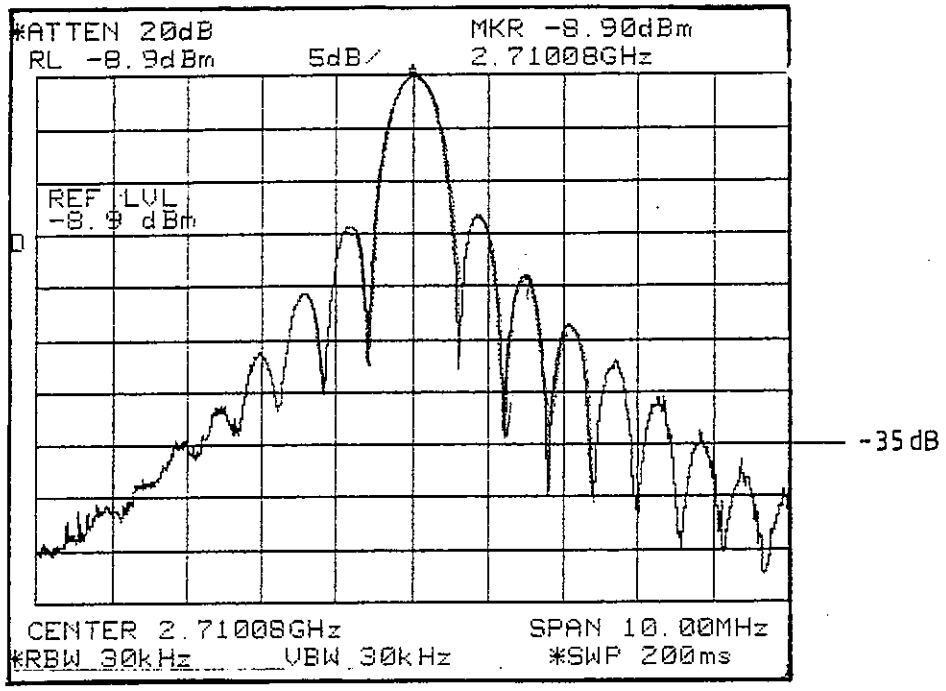


Figure 4.5

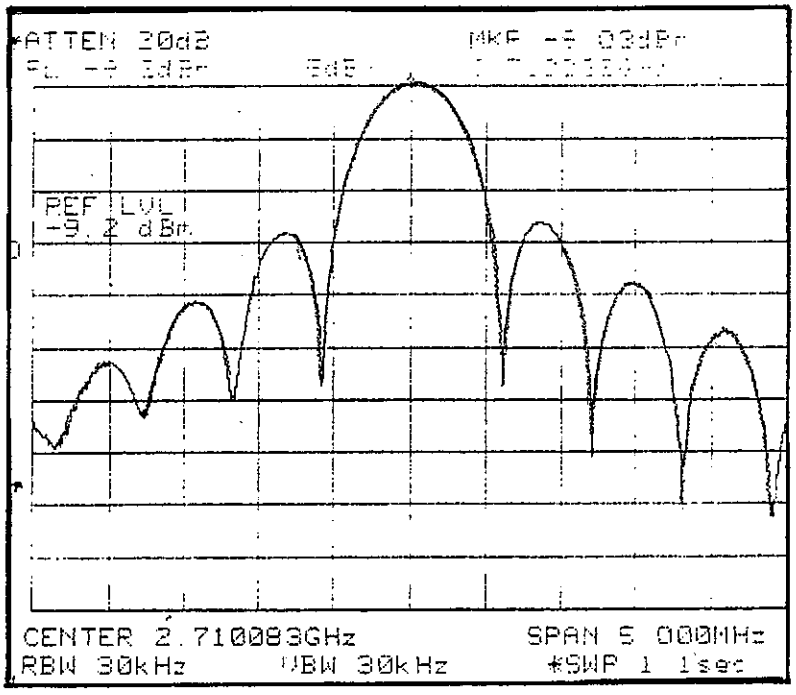


Figure 4.6

Typical Spectrum of Pulsed RF Output

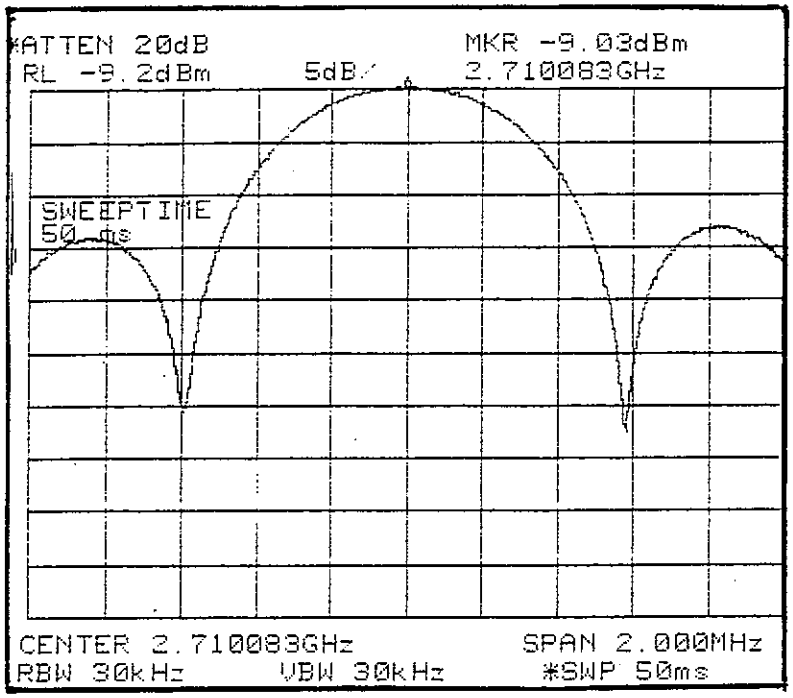


Figure 4.7 Typical Spectrum of Pulsed RF Output

APPENDICES

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5

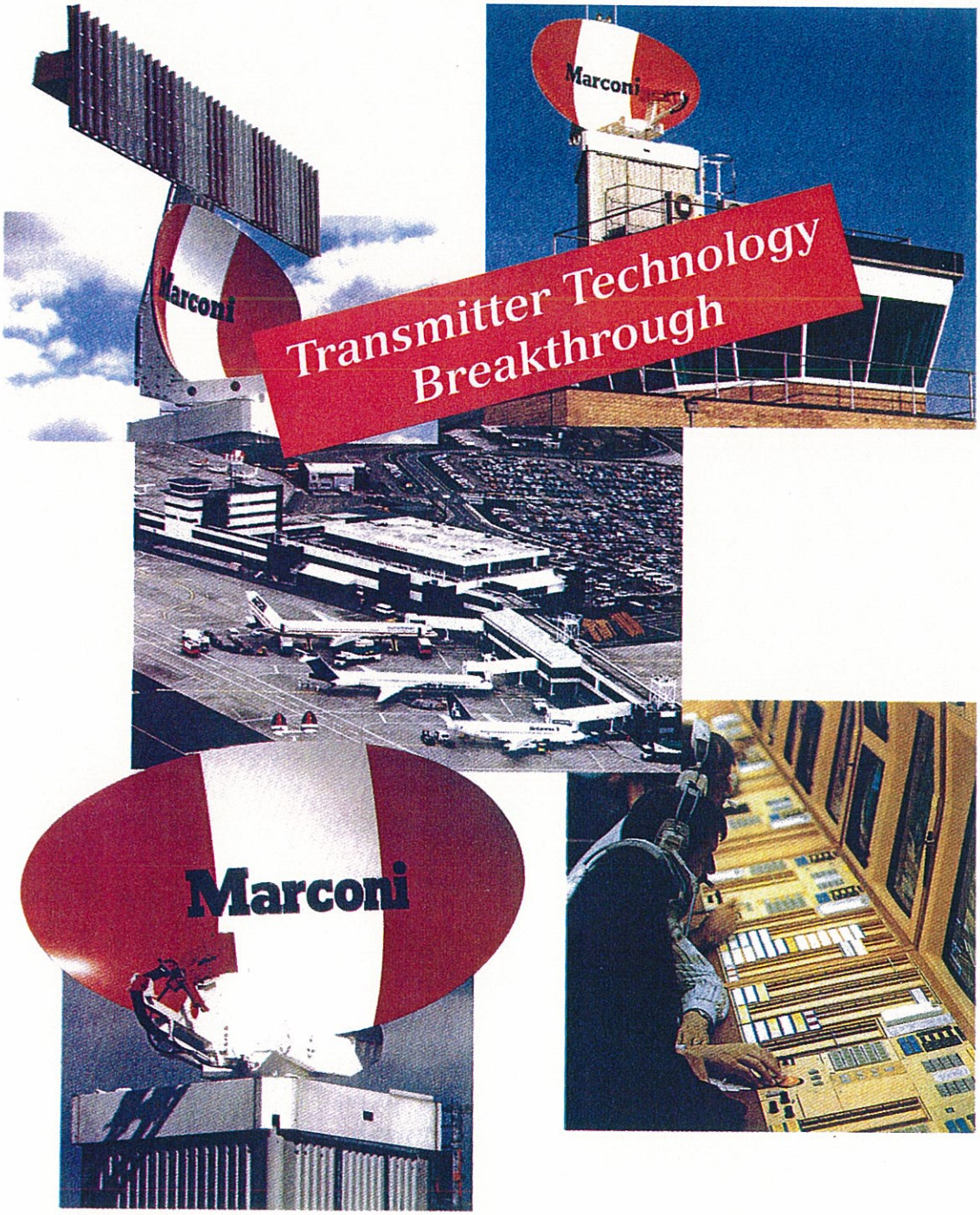
Appendix 1

SURVEYOR

Equipment Profile

SURVEYOR

Primary Surveillance Radar



ATC RADAR SYSTEMS

Marconi
Radar Systems

SURVEYOR

Marconi Radar has overturned the traditional view that Air Traffic Control radars need costly driven transmitters to acheive the necessary level of clutter supression. Several years of research have produced a new device - the Hystron - which gives the SURVEYOR primary surveillance radar a performance which matches or exceeds that of more expensive ATC radars.

The long life Hystron and solid state FET (Field Effect Transistor) modulator provide remarkable frequency and phase stability. The design is simple, rugged and safe - no EHT (Electrical High Tension) supplies, no pulse compression - to give ease of maintenance and outstanding reliability at a price to satisfy the most hard-pressed budgets.

Marconi pioneered the use of solid carbon fibre antennas for ATC radars many years ago and has constantly refined the techniques. SURVEYOR'S corrosion-free antenna and 100,000 hour turning gear exemplify the drive to reduce scheduled and unscheduled downtime.

Dualised electronics provide the performance benefits of frequency diversity and the confidence of full redundancy - at a lower price than most single channel systems.

Creative design and value engineering, based on a 40 year ATC pedigree, enable SURVEYOR to fill the most demanding ATC roles reliably with technology developed for affordability.

Features

- *More than 100nm Range on Small Targets*
- *Minimum Range of <0.5nm for SRA*
- *Adjustable Parameters for ACR/TMA Use*
- *Fully Adaptive MTD Processing*
- *Improvement Factor > 50db*
- *Single or Dual Channel Electronics*
- *25,000 Hour Transmitter Tube Life*
- *Remote Control and Monitoring*
- *Unattended Operation*
- *Provision for Co-mounted SSR Antenna*
- *Separate Weather Channel Option*
- *Fibre Optic Data Transmission Option*

SURVEYOR

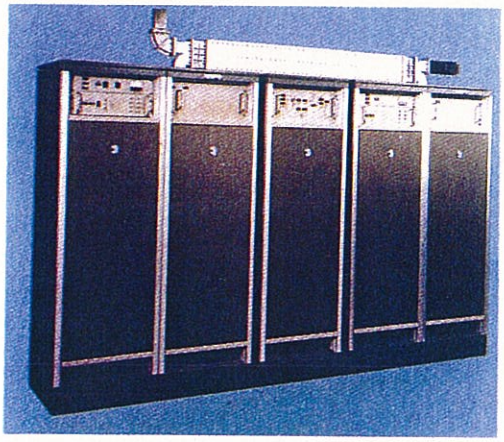
Maximum Flight Safety

Flight safety is paramount in the design of any Air Traffic Control System. The SURVEYOR Primary Surveillance Radar provides the ultimate in accuracy and reliability, conforms to ICAO standards and provides around the clock, all weather, radar coverage. Designed specifically for Civil Air Traffic functions, it is responsive to rapid increases in air traffic volumes and the consequent pressures on separation standards and landing rates.
Safety critical features include advanced transmitter and signal processing techniques to detect the smallest aircraft in the most severe clutter and weather conditions.

Minimum Cost of Ownership

Cost of ownership has been minimised by careful design both of equipment and support services.

Low capital cost	*Reduces initial investment*
Efficient design	
High overall efficiency	*Low running cost*
Easy maintenance	



Dual Transmitter / Receiver and Signal Processor Configuration

This is achieved by use of a Hystron output tube in the transmitter. The Hystron gives a performance level that equals or exceeds that of the most expensive radar transmitter but at a replacement cost of less than a quarter of that of comparable linear beam devices.

Maintenance staffing levels can be minimised as SURVEYOR does not require routine electronic maintenance and includes extensive fault location and module replacement features. Spares holdings are minimised due to the system's inherent reliability and the availability of fast turnaround support packages.

Maximum Revenue Earning Power

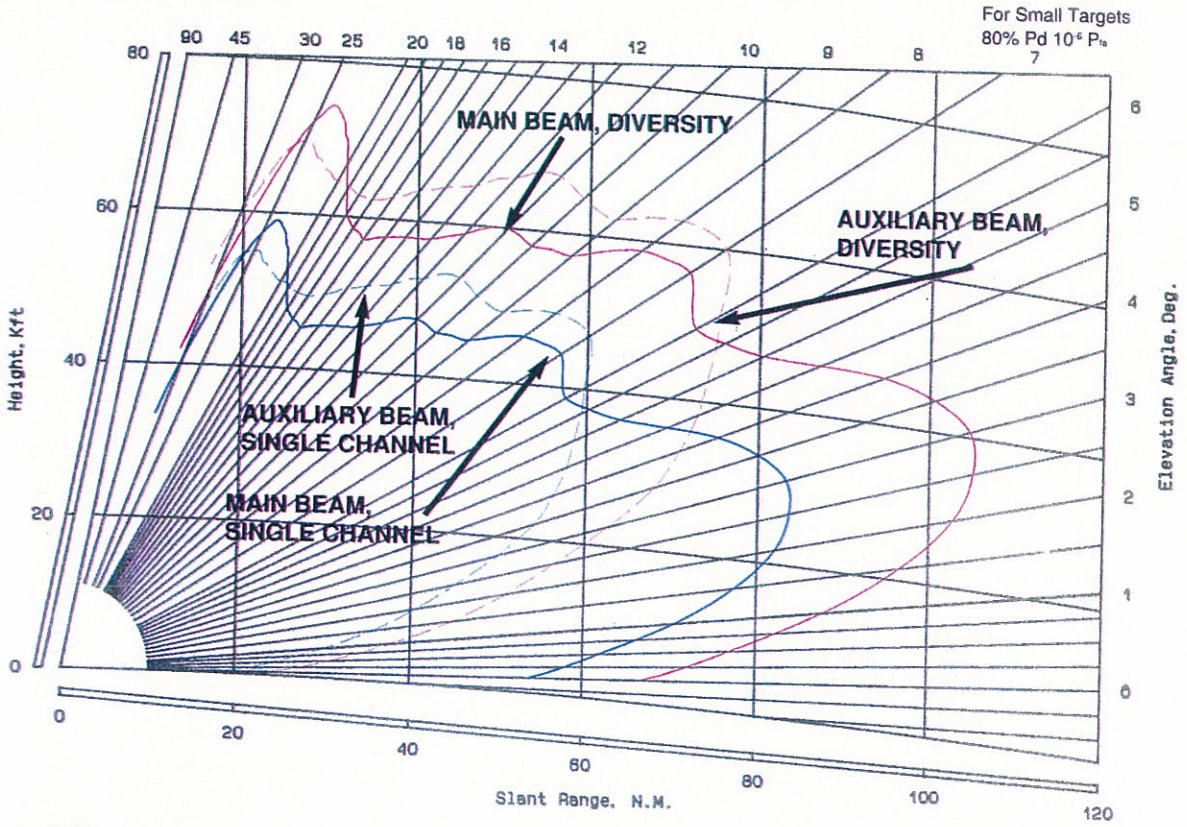
Airlines select airports with a reputation for efficient, reliable Air Traffic Control services offering minimum flight delays. In today's high traffic densities, this demands a modern radar system which can cope with bad weather conditions and provide a surveillance capability to touchdown all day, every day.

SURVEYOR fully meets these needs and offers the technical performance and reliability necessary to enhance airfield earnings by:-

- *Directly - Providing the best in Reliability and Services*
- *Indirectly - Enhancing the Airport's Reputation for Efficient Traffic Management*

thereby maximising the earnings-to-cost ratio.

SURVEYOR - Primary Surveillance Radar Performance



Specification

Radio Frequency Band

2.7 to 2.9 GHz

Antenna (2-beam)

Reflector	Carbon fibre composite
Gain	Main beam>34.0dB Aux. beam>31.5dB
Vertical pattern	Modified cosec²
Horizontal beam width	1.5°
Rotation speed	15 rpm
Polarisation	Circular/linear

Transmitter

Peak power	1MW
Mean power	1.5kW
Pulse duration	0.5 to 3μS
PRF	500-1500 pps
PRF stagger	6 period up to +/- 14%
Tube life	25,000 hours (typical)

Receiver

Noise factor	<=2.0 dB
IF	45MHz
Dynamic range	85 dB

Signal processor

Type	AMTD Parallel processing
Instrumented range	Configurable
Beam switching	Adaptive and range gated
Temporal threshold	Range/azimuth cell basis
Improvement factor	>50 dB

MTBF

Dual diversity	>6000 hours (one channel failed)
Single channel	>1750 hours

Marconi
Radar Systems
A division of Marconi Radar and Control Systems Limited

Marconi Radar Systems
Eastwood House
Glebe Road
Chelmsford
Essex CM1 1QW, UK
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MRCS/1058/09/94

Designed and produced in the U.K. by The Phase Group +44 (0) 1256 704140

5.2 Appendix 2 M.T.I. Improvement Factor

5.2.1 Overview

The performance of a radar system and its ability to extract wanted target signals out of clutter due to weather, land or sea reflections is specified in a quantity known as 'Overall MTI Improvement Factor (MTI I/F)'.

MTI I/F is usually specified in dB, the higher the dB factor, the better the system performance.

The Improvement Factor is defined as[1]:-

$$\frac{(\text{Signal/Clutter})\text{output}}{(\text{Signal/Clutter})\text{input}}$$

$$= \frac{\text{Clutter input}}{\text{Clutter output}} \times \frac{\text{Signal output}}{\text{Signal input}}$$

Over all target velocities

$$\frac{\text{Signal output}}{\text{Signal input}} = \frac{\text{Noise output}}{\text{Noise input}} = \text{Noise Gain}$$

So

Improvement Factor = Clutter Attenuation x Noise Gain

However, the total system Improvement Factor is limited by certain relevant stability factors, and for the S2055 transmitter/receiver, they are:

5.2.2 Transmitter Stability Limitation Factors

5.2.2.1 Frequency

The pulse to pulse variation in the frequency of the transmitted pulse from the magnetron.

Improvement Factor $I_{\Delta f}$ = $\underline{20\text{Log } (1/(\pi.\Delta f.\tau))\text{ dB}}$

Where Δf is the Standard Deviation of the pulse to pulse frequency, and τ = RF Pulse Width at the 50% or -3dB power level.

5.2.2.2 Jitter

RF Pulse width jitter or time jitter between the front edge of the input trigger from the signal processor to the front edge of the RF Pulse:

Improvement Factor I_{pwj} = $\underline{20\text{Log } (\tau/\Delta t)\text{ dB}}$

Where Δt = the Standard Deviation of the jitter.

5.2.2.3 Amplitude

Improvement Factor I_A(dB) = $\underline{20\text{Log } (A/\Delta A)\text{ dB}}$

or $\underline{10\text{Log } [(A/\Delta A)^2]\text{ dB}}$

Where A is the pulse amplitude

& ΔA is the Standard Deviation of the amplitude variations.

The I_A stability limitation in the S2055 design is such that it may be neglected in the overall MTI/IF calculation.

5.2.3 Receiver Stability Limitation Factors

5.2.3.1 Receiver Local Oscillator A crystal controlled STALO(STAble Local Oscillator) Improvement Factor $I_s = \underline{20\text{Log } (1/(2.\pi.\Delta f.T))\text{ dB}}$

Where T is the time to the target and return, a value of 308.7μs, corresponding to a target range of 25 nautical miles, was recommended by systems engineers.

and Δf is the Standard Deviation of the STALO frequency.

5.2.3.2 Coherent Oscillator

Coho frequency (or phase) instability:

Improvement Factor $I_c = \underline{20\text{Log } (1/(2.\pi.\Delta f.T))\text{ dB}}$

5.2.4 Signal Processor Factors

5.2.4.1 The Digital Signal Processor in use, uses two Analog to Digital (A/D) converters to digitize the phase and quadrature outputs of a base band mixer. The A/D converters used are 10 BIT output, and therefore divide the analog f.s.d range into a number of discrete amounts: 2^n-1, in this case 1023.

According to references Skolnik[1], the Improvement Factor is limited due to the Quantization Noise of the A/D used, and is calculated as:

$I_{qn} = 20\log([2^n-1]. (0.75)^{1/2})$ dB.

Therefore for a 10 bit system:

$I_{qn} = 20\text{Log}([2^{10}-1] (0.75)^{1/2})$

$= 20\text{Log}(1023. (0.75)^{1/2})$

$= 20\text{Log } 885.944$

$I_{qn} = \underline{58.98\text{dB}}$

5.2.4.2 Timing variation (pulse to pulse):

$I_T = 20\text{Log} (\tau / (\sqrt{2}. \Delta t))$ Db

Where τ is the -3dB R.F pulse width

& Δt is the Standard Deviation of the pulse timing.

5.2.5 Aerial Scanning Limitation Factor

According to Skolnik[1], a model for Improvement Factor limitation due to scanning, for a radar using 4 pulse Digital MTI Signal Processor; MTI filter having Bi-nomial weighting:

$$I_{scan} = n^6/16$$

Where "n" is the N° of pulse hits on a point target, as the antenna scans the target, within the -3dB beamwidth of the antenna.

The number of hits, is dependant upon:

The antenna -3dB Beamwidth Surveyor: 1.5°

The radar PRF 840 Hz

The rotation rate of the antenna 15 RPM

$$n = \frac{PRF}{Ant_{RPM}/60} \times \frac{BW_{-3dB}}{360}$$

$$n = \frac{840}{(15/60)} \times \frac{1.5}{360} = \underline{14} \text{ Hits.}$$

$$I_{scan} = \frac{14^6}{16} = \underline{470596}$$

$$I_{scan\ dB} = 10.\log 470596 = \underline{56{\cdot}73} \text{ dB.}$$

5.2.6 Calculation of Overall MTI I/F

Input Parameters assumed for the Calculations

Transmitted Pulse Width (τ): 1·6 μs

'T' 308·7μs

The stability factors are combined to yield an overall MTI/IF as follows:

Each of the stability factors I_x dB are converted into a power ratio:

Eg: $I_{\Delta f}' = \text{Antilog}_{10} I_{\Delta f}/10$

then:

$1/I_{total}' = 1/I_{qn}' + 1/I_{\Delta f}' + 1/I_{pwj}' + 1/I_A' + 1/I_s' + 1/I_c' + 1/I_T'$

The result is then converted back to dB:

$\text{MTI I/F}_{Total} = 10.\text{Log}_{10} I_{total}'$.

MTI improvement calculations is an ideal candidate for a computer program.

Refer to listings attached:

To illustrate the method of obtaining the overall MTI I/F, using the computer program listed and early predicted parameters:

Results

Transmitter Frequency Stability: 350 Hz		55·093 dB
Transmitter Pulse Width Jitter: 2·5 ns		56·124 dB
STALO Stability 0.01 rad/4 ms:	0·398 Hz	62·250 dB
COHO Stability 0.005 rad/4 ms:	0·2 Hz	68·225 dB
P.R.I Timing Jitter:	0·5 ns	67·093 dB
Quantization N° of Bits:	10	58·948 dB
Overall MTI I/F		51·06 dB

If the scanning effect is included the MTI I/F reduces to 50·018 dB

```
/* MTI I/F Program Header File  File Name "IF.H"                    */

/* Initial default stability limitation factors                     */

/* Transmitter Frequency Stability (Standard Deviation)             */
float txfs=350;                    /*Hz*/

/* Transmitter Pulse Jitter (Standard Deviation)                    */
float txpwj=2.5e-9;          /*s*/

/* STALO Frequency (phase) stability                                */
float   stalofs=0.3978874;  /*Hz*/
/* The rms change in phase over 4ms is better than 0.01 rad         */
/* this is equivalent to 0.3978874 Hz.                              */

/* COHO Frequency (phase) stability                                 */
float   cohofs=0.2;                /*Hz*/
/* The rms change in phase over 4ms is better than 0.005 rad        */
/* this is equivalent to 0.1989437 Hz                               */

/* PRI Timing Jitter                                                */
float   pritj=0.5e-9;          /*s*/

/* A-D Quantization                                                 */
int     nbit=10;               /*No of Bits*/

/* Transmitted RF Pulse Width @ -3dB level                          */
float   pw=1.6e-6;             /*s*/

/* Time to Target and Return T proportional to range                */
float   trtn=308.7e-6;         /*s equivalent to 25 nautical miles  */

/* Function Proto-types                                             */
float ifcalc(float txfs,float txpwj,float stalofs,float cohofs,
                        float pritj,float pw,float trtn,int nbit);
void show_default_params(float txfs,float txpwj,float stalofs,
                                float cohofs,float pritj,int nbit,
                                        float pw,float trtn);
float edit_txfs(float txfs);
float edit_txpwj(float txpwj);
float edit_stalofs(float stalofs);
float edit_cohofs(float cohofs);
float edit_pritj(float pritj);
int edit_nbit(int nbit);
float edit_pw(float pw);
float edit_trtn(float trtn);
```

```
/* IF.H continued                                    */

void ed1(void);
void ed2(void);
void ed3(void);
void ed4(void);
void ed5(void);
void ed6(void);
void ed7(void);
void ed8(void);
void calc(void);
void end(void);

/* End of IF.H                                       */
```

```
/* MTI I/F Program "main.c", File Name:IFACTOR.C          */
/* Show default parameters and allow editing              */
#include <stdio.h>
#include <math.h>
#include <stdlib.h>
#include <if.h>
main()
{
        char cp;
                do
        {
                show_default_params(txfs,txpwj,stalofs,cohofs,pritj,nbit,pw,trtn);
                cp = (getch());
        {
                case '1': ed1();
                break;

                case '2': ed2();
                break;

                case '3': ed3();
                break;

                case '4': ed4();
                break;

                case '5': ed5();
                break;

                case '6': ed6();
                break;

                case '7': ed7();
                break;

                case '8': ed8();
                break;

                case '9': ed9();
                break;
                case 'q': end();
                break;
                default:printf("\nInvalid Choice\n");
        }
}
        while (cp! = 'q');
        return 0;
}
```

```
/*IFACTOR.C continued                                                    */
void calc(void)
{
        float oif;
        oif = ifcalc(txfs,txpwj,stalofs,cohofs,pritj,pw,trtn,nbit); /*calculator*/
        printf("\n\n\tOverall MTI I/F=%.3fdB\n",oif);
        printf("\n\tpress any key to return to parameter list\n");
        getch();
        return;
}

void ed1(void)
{
        txfs = edit_txfs(txfs);
        return;
}

void ed2(void)
{
        txpwj = edit_txpwj(txpwj);
        return;
}

void ed3(void)
{
        stalofs = edit_stalofs(stalofs);
        return;
}

void ed4(void)
{
        cohofs = edit_cohofs(cohofs);
        return;
}

void ed5(void)
{
        pritj = edit_pritj(pritj);
        return;
}

void ed6(void)
{
        nbit = edit_nbit(nbit);
        return;
}
```

```
/* IFACTOR.C continued                                          */

void ed7(void)
{
        pw = edit_pw(pw);
        return;
}

void ed8(void)
{
        trtn = edit_trtn(trtn);
        return;
}

void end(void)
{
        clrscr();
}
```

```
/* MTI I/F Program  Calculator Function  File Name: IFCALC.C       */


#include <math.h>
#include <conio.h>
#define pi 3.141592654

float  ifcalc(float ifsc,float ipwjc,float isc,float icc,float itc,
                float pwc,float trc,int bits);

{
        float ifq;
        float iftxfs;
        float ifpwj;
        float ifs;
        float ifc;
        float ift;
        float iftot;
        float iftotal;
        {
         ifq=20*log10((pow(2,bits)-1)*(sqrt(0.75))); /*I/F Quantization*/
        }

        {
         iftxfs=20*log10(1/(pi*ifsc*pwc));  /*I/F TX Freq' Stability*/
        }

        {
         ifpwj=20*log10(pwc/ipwjc);  /*I/F TX Pulse Jitter*/
        }

        {
         ifs=20*log10(1/(2*pi*isc*trc));  /*I/F STALO Freq' Stability*/
        }

        {
         ifc=20*log10(1/(2*pi*icc*trc));  /* I/F  COHO Freq' Stability*/
        }

        {
         ift=20*log10(pwc/(sqrt(2)*itc));  /*I/F Timing*/
        }
```

```
/* IFCALC.C Continued                                              */

{
        clrscr();
/* Display Results */

printf("\n\n\tIndividual Improvement Factor Contributions\n");
printf("\tQuantization I/F\t\t\t=\t%.3fdB\n",ifq);
printf("\tTransmitter Freq Stability I/F\t\t=\t%.3fdB\n",iftxfs);
printf("\tRF Pulse front edge Jitter I/F\t\t=\t%.3fdB\n",ifpwj);
printf("\tSTALO Freq Stability I/F\t\t=%.3fdB\n",ifs);
printf("\tCOHO Freq Stability I/F\t\t=\t%.3fdB\n",ifc);
printf("\tPRI Timing Jitter I/F\t\t=\t%.3fdB\n",ift);
}

/* Calculation of Overall MTI I/F */
{
 iftot=1/(
          (1/(pow(10,(ifq/10))))+(1/(pow(10,(iftxfs/10))))
              +(1/(pow(10,(ifpwj/10))))+(1/(pow(10,(ifs/10))))
                +(1/(pow(10,(ifc/10))))+(1/(pow(10,ift/10))))
                                                                );

        iftotal=10*log10(iftot); /* dB */
}
        return(iftotal); /* dB */

}
```

```
/* MTI I/F Program File Name: SHOWDEF.C                    */
/* Displays S2055 Default Parameters                       */

#include <stdio.h>

void show_default_params(float fs,float stafs,float cohfs,
                         float prij,int bit,float pwid,float trn)

{
      clrscr();
      printf("\n\t\tDefault Parameters\n");
      printf("\n1\tTransmitter Frequency Stability\t=\t%.3f Hz\n",fs);
      printf("\n2\tTransmitter Pulse Width Jitter\t=\t%.3f ns\n",(pwj/1e-9));
      printf("\n3\tSTALO Frequency Stability\t=\t%.3f Hz\n",stafs);
      printf("\n4\tCOHO Frequency Stability\t=\t%.3f Hz\n",cohfs);
      printf("\n5\tP.R.I Timing Jitter\t\t=\t%.3f ns\n",(prij/1e-9));
      printf("\n6\tNumber of bits in Sig' Proc' A-D's\t=\t%d\n",bit);
      printf("\n7\tTransmitted RF Pulse Width(-3dB)\t=\t.3f micro-sec\n",
                                    (pwid/1e-6));
      printf("\n8\tTime to Target and Return\t=\t%.3f micro-sec\n",(trn/1e-6));
      printf("\n9\tCalculate I/F contributions & Overall MTI I/F\n");
      printf("\nTo edit a parameter, select as required\n");
      printf("\nenter 'q' to exit program\n");

      getch();
      return;

}
```

```
/* MTI I/F Program          File Name: ED.C                              */
/* Editing the Default Values                                            */
#include <stdio.h>
char inbuf[7];

float edit_txfs(float tfs)
{
        printf("\n\tEnter new value for Transmitter Frequency Stability (Hz)\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&tfs);
        return (tfs;
}

float edit_txpwj(float twj)
{
        printf("\n\tEnter new value for Transmitter Pulse Width Jitter\n");
        printf("\n\tNote: enter value in form eg: '2.0e-9' ie 2 ns\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&twj);
        return (twj);
}

float edit_stalofs(float stfs)
{
        printf("\n\tEnter new value for STALO Frequency Stability\n");
        printf("\n\tNote: enter value in form eg: '0.3' ie 0.3 Hz\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&stfs);
        return (stfs);
}

float edit_cohofs(float cofs)
{
        printf("\n\tEnter new value for COHO Frequency Stability\n");
        printf("\n\tNote: enter value in form eg: '0.1' or 1.0e-1 Hz\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&cofs);
        return (cofs);
}

float edit_pritj(float prij)
{
        printf("\n\tEnter new value for PRI Timing Jitter\n");
        printf("\n\tNote: enter value in form eg: 1e-9 ie 1ns\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&prij);
        return (prij);
}
```

```
/* ED.C Continued                                                    */

int edit_nbit(int bt)
{
        printf("\n\tChange number of bits in Sig' Proc'\n");
        printf("\n\tenter eg: 8, 10, 12 or 16 \n");
        gets(inbuf);
        sscanf(inbuf,"%d",&bt);
        return (bt);
}

float edit_pw(float pwidth)
{
        printf("\n\tEnter new value for RF Pulse Width\n");
        printf("\n\tenter value in form eg: 1.5e-6 ie 1.5 micro-sec\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&pwidth);
        return (pwidth);
}

float edit_trtn(float tr)
{
        printf("\n\tEnter new value for 'Time to Target & Return'\n");
        printf("\n\tenter value in form eg: 308.7e-6 ie 308.7 micro-sec\n");
        printf("\t the value is proportional to range eg: 25 nautical miles\n");
        gets(inbuf);
        sscanf(inbuf,"%f",&tr);
        return (tr);
}

/*                    END OF PROGRAM                                 */
```

5.3 Appendix 3 Jitter Measurements

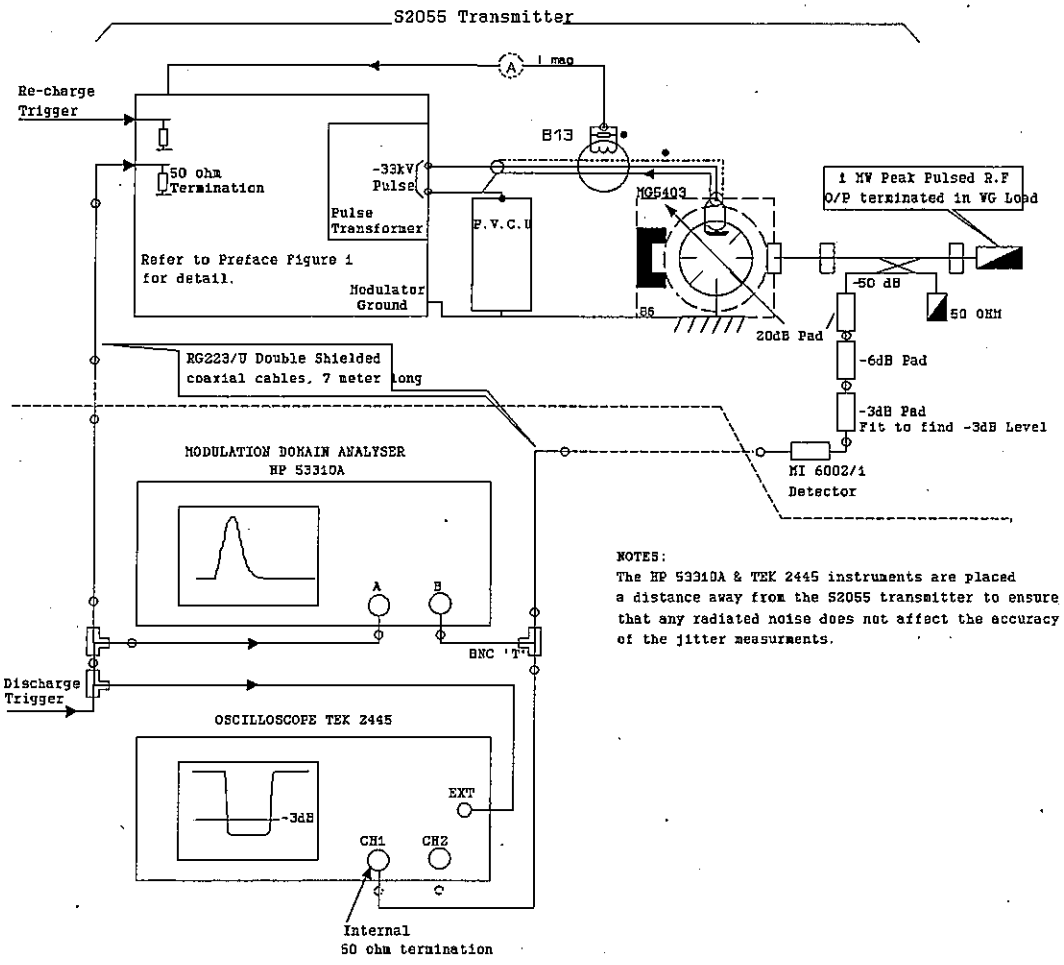


Figure 5.3.1

5.3.1 Measurement of the time variation or jitter between the front edge of the Discharge Trigger from the Signal Processor and the front edge of the transmitter pulsed RF output pulse is carried out using the test connections and equipment as shown above.

5.3.2 Initially the RF pulse, detected envelope is monitored on the oscilloscope , using a micro wave detector crystal.

In order to use the detector to provide a timing reference at the -3dB half power level or to measure the -3dB pulse width for power measurements, it is essential that the detector is operated within the 'square law' part of its characteristic and not over driven. The pulse is displayed initially with the 3dB Pad removed and the pulse height measured using the cursors:

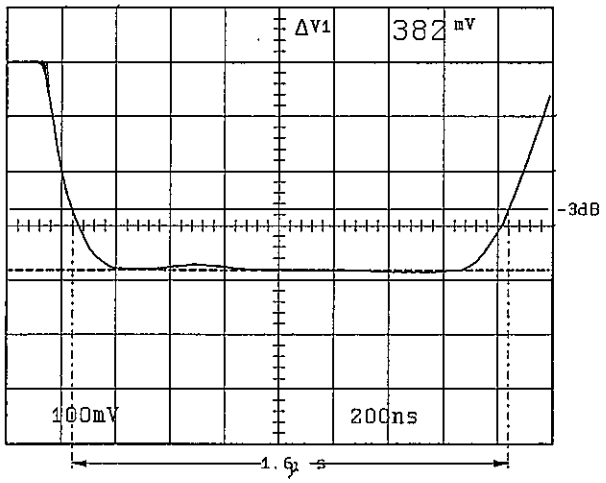


Figure 5.3.2 : CH1 set to 100mV/div,DC coupled,50 ohm terminated.

5.3.3 Level proportional to RF peak power $= V^2/R_{term}$

$(382.10^{-3})^2/50$

$= \underline{2.918 .10^{-3}}$

Half RF peak power level $= 2.918 .10^{-3}/2$

$= \underline{1.459 .10^{-3}}$

The voltage level at the -3dB power level:

$V = (1.459 .10^{-3} \times 50)^{1/2}$

$V = \underline{270 \text{ mV}}$

The lower cursor is then set at the 270 mV level.

The -3dB power level may then be checked by inserting the 3dB pad in series with the 20 and 6 dB pads. The displayed pulse level should reduce to the 270 mV level.

The 3 dB pad is then removed, with the cursor set at the -3dB level.

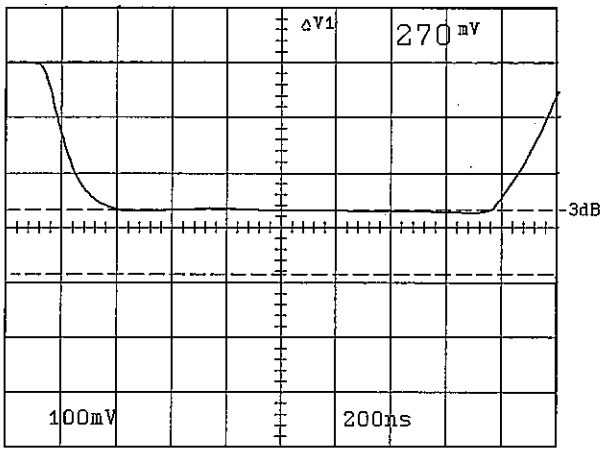


Figure 5.3.3

5.3.4 The oscilloscope is set to trigger on the rising edge of the Discharge trigger, therefore any jitter may be observed on the front edge of the pulse. Using the delayed timebase facility on the oscilloscope the front edge may be observed with the timebase at 20ns/cm.

The jitter performance improves as the magnetron reaches full operating temperature, after approximately 45 minutes.

5.3.5 Using an oscilloscope to measure jitter in the order of 2ns standard deviation (10ns peak) is subjective and visual estimation of the peak variation depends on factors such as persistence of the oscilloscope screen and ones eyesight. It is also not possible to see how the jitter,time variation is distributed.

5.3.6 The most suitable instrument to evaluate the jitter performance of transmitters is to use a 'Modulation Domain Analyzer HP 53310A.

The analyzer is configured to capture 1000 time intervals between a 'start'(rising edge of Discharge Trigger) and 'stop'(-3dB threshold level of the front edge of the RF pulse) events. It is very important that the trigger threshold of the B channel is set to the voltage proportional to the -3dB level, in this case -270mV. The trigger level of the A input (Discharge Trigger) is set to 50% of the peak trigger pulse voltage.

The analyzer stores all the time intervals, indicates the Pk to Pk and also calculates the Standard Deviation. The screen display presents the time intervals in a histogram form which allows the distribution to be seen.

5.3.7 The instrument triggers on a continuous basis, and therefore showing latest jitter performance. Facility is provided to print out the screen display showing the jitter results .

The screen display is as shown in Figure 5.3.4:

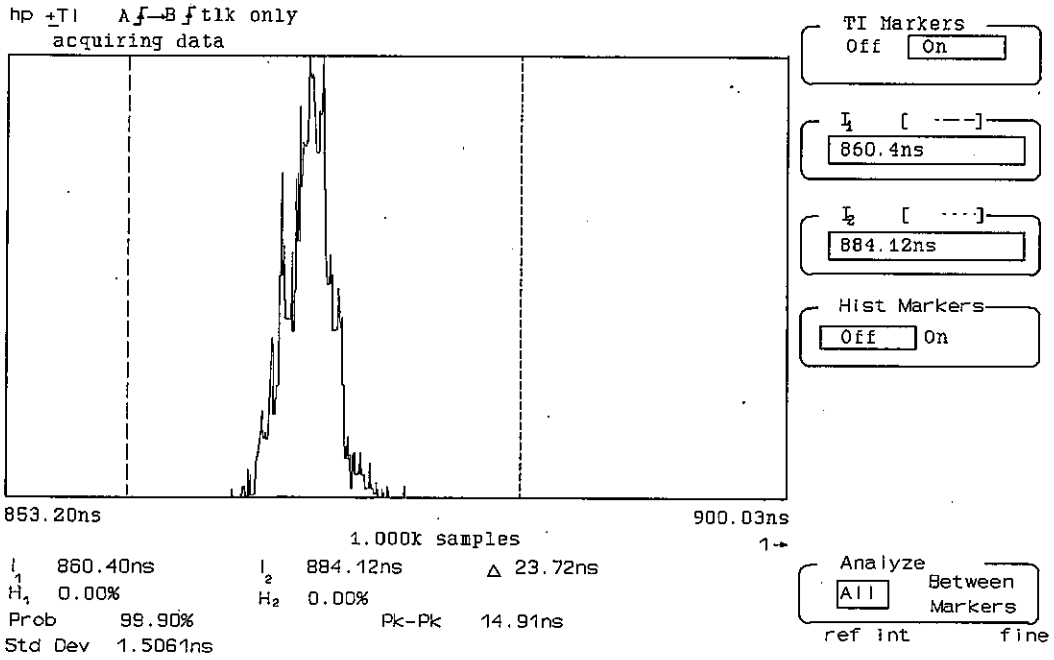
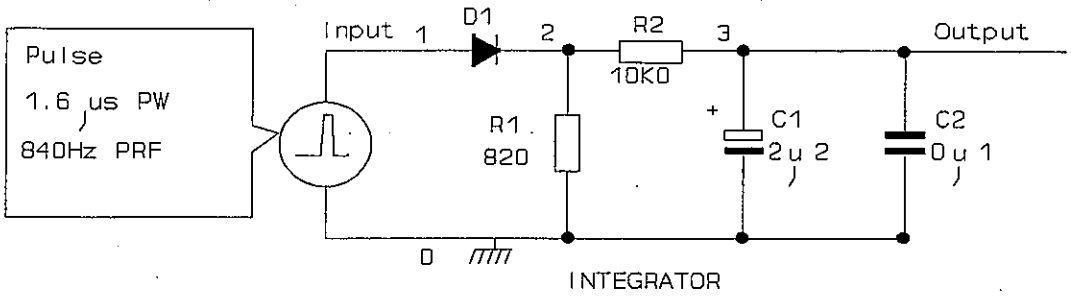
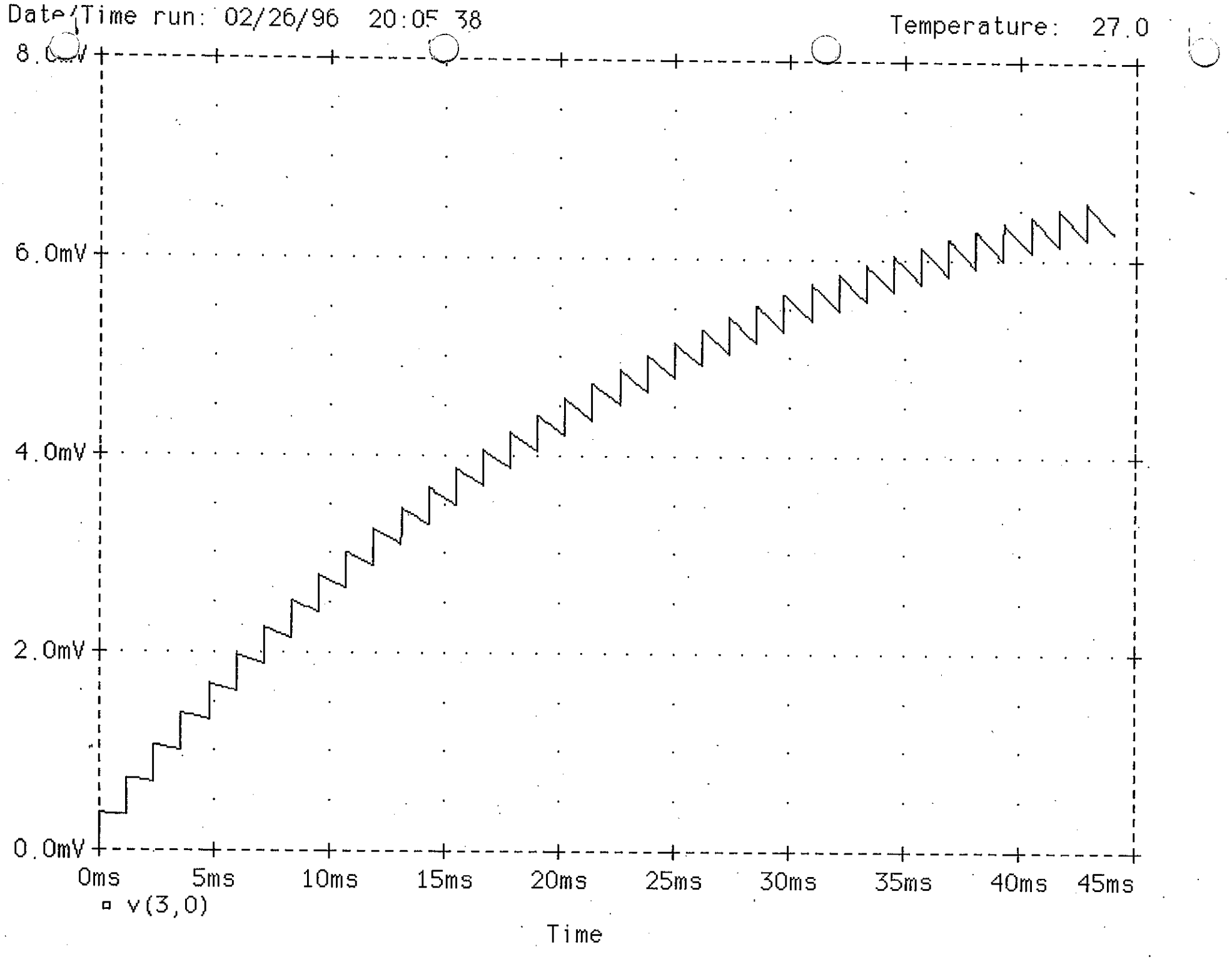

hp ±TI A∫→B∫ tlk only
acquiring data
TI Markers
Off On
I1 [---]
860.4ns
I2 [---]
884.12ns
Hist Markers
Off On
853.20ns
900.03ns
1.000k samples
I1 860.40ns
I2 884.12ns
Δ 23.72ns
H1 0.00%
H2 0.00%
Prob 99.90%
Pk-Pk 14.91ns
Std Dev 1.5061ns
Analyze
All
Between Markers
ref int
fine

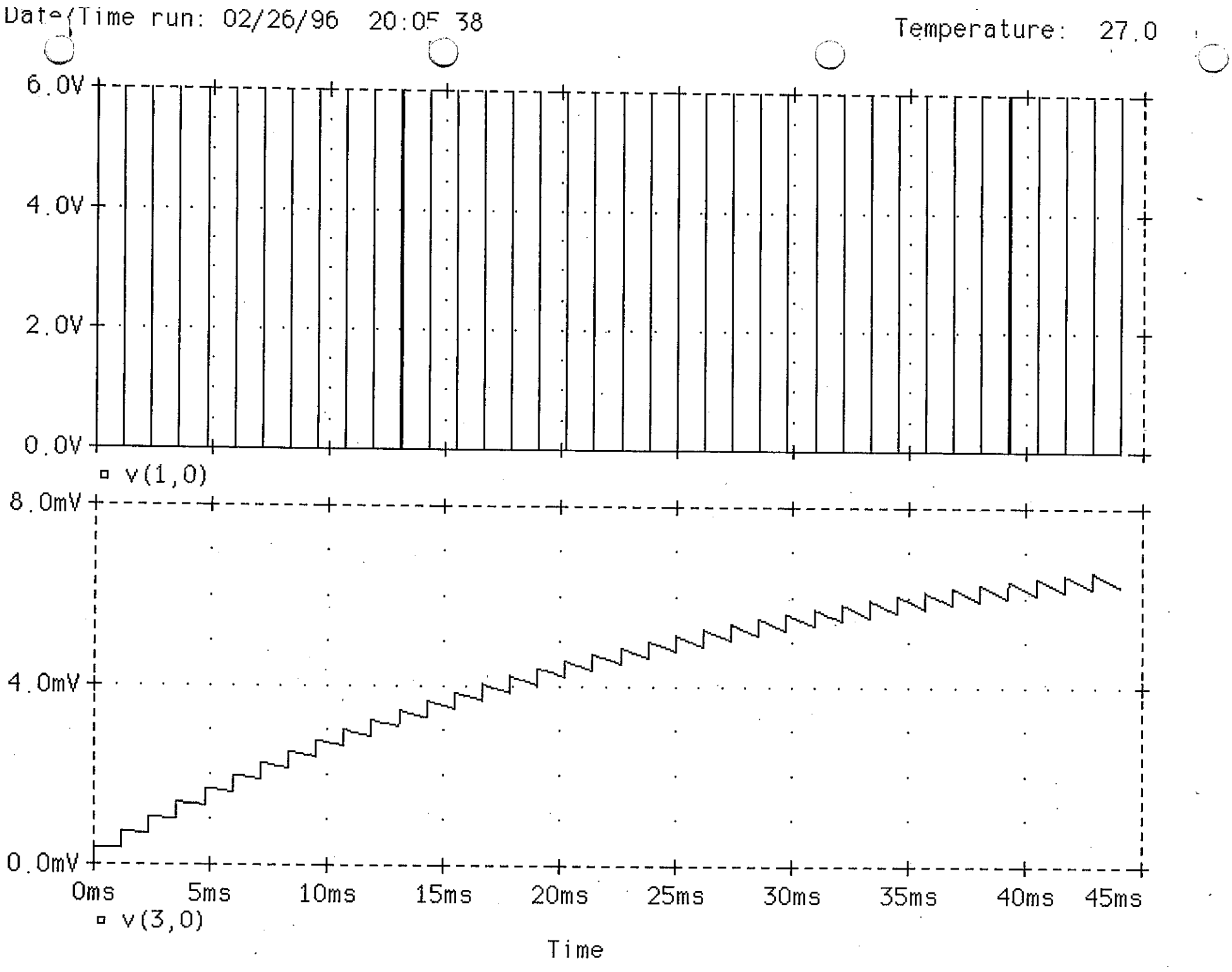
Figure 5.3.4

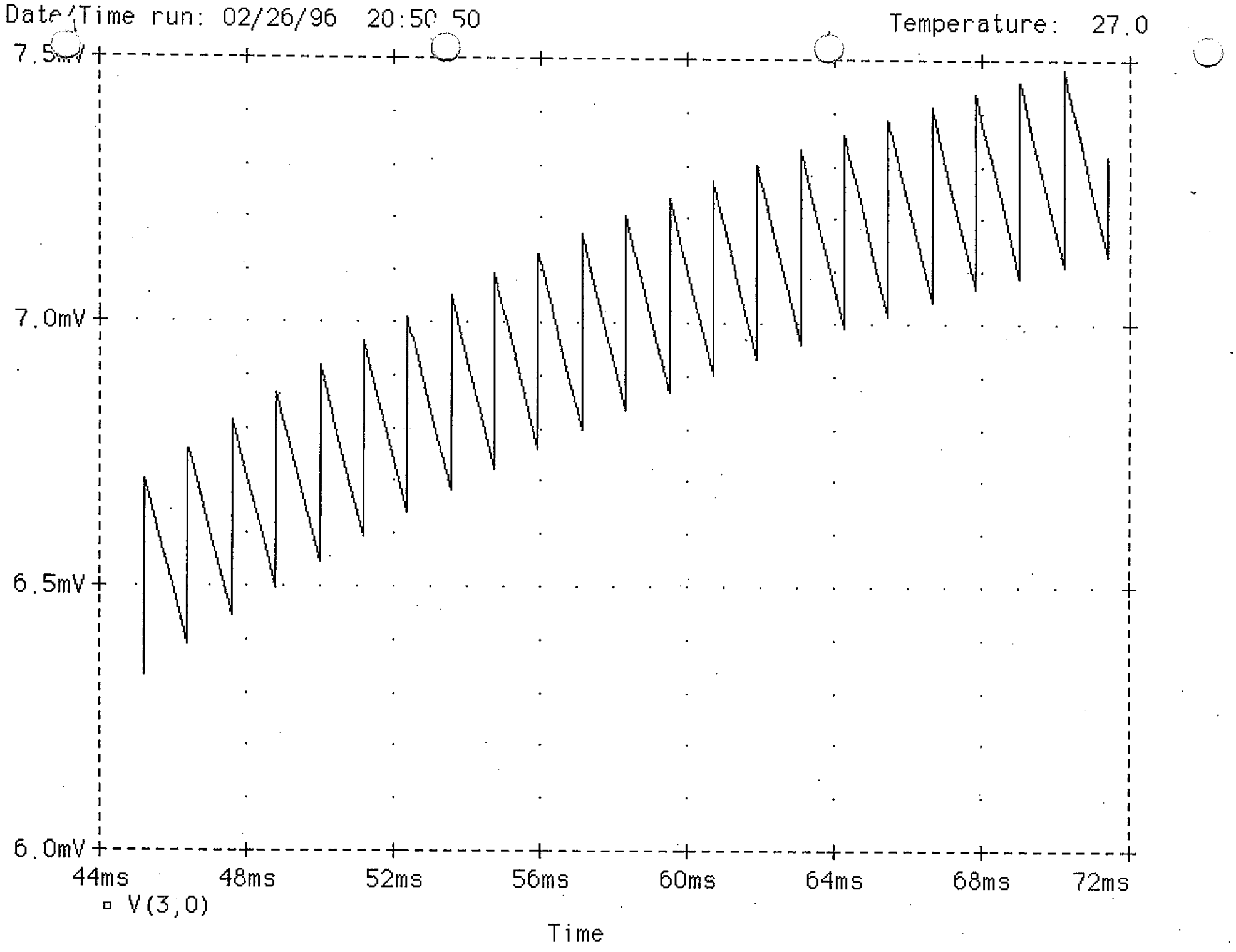
5.4 Appendix 4 Integrator, PSPICE Results

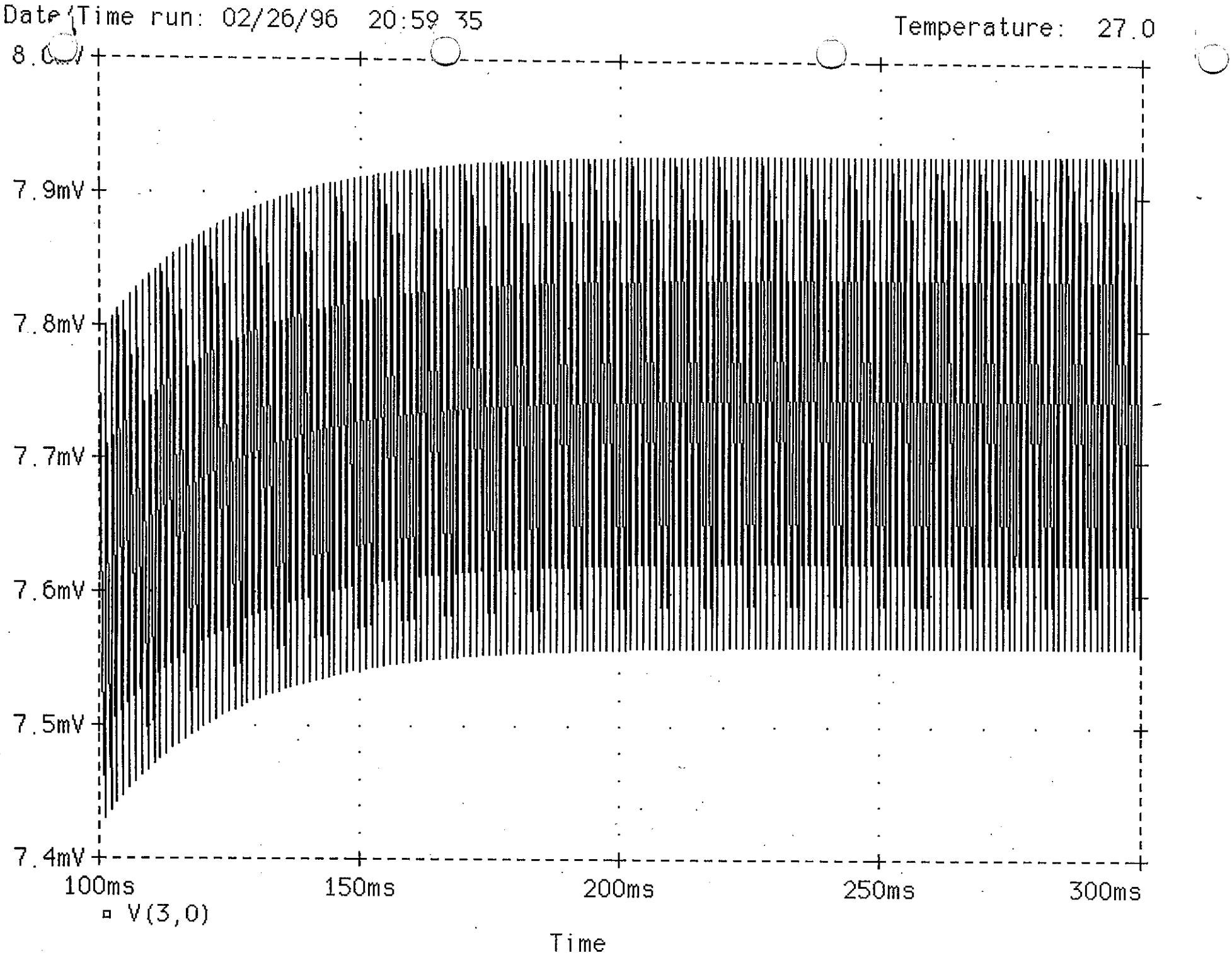



```
* Integrator
.OPTION RELTOL = 0.01  ITL5 = 0
* Input pulse simulating a 6v pulse at 840 Hz
* having a pulse width of 1.6 microseconds,tr & tf=10ns.
VPULSE 1  0  PULSE (0  6  0NS  10NS  10NS 1.6E-6  1.19E-3)
D1     1  2  D1N4149
R1     2  0  820
R2     2  3  10E3
C1     3  0  2.2E-6
C2     3  0  0.1E-6
.LIB   C:\SPICE\DNOM.LIB
.TRAN  50E-6   100MS
.PROBE
.END
```


Date/Time run: 02/26/96 20:05:38
Temperature: 27.0
8.0mV
6.0mV
4.0mV
2.0mV
0.0mV
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
v(3,0)
Time


Date/Time run: 02/26/96 20:05:38
Temperature: 27.0
6.0V
4.0V
2.0V
0.0V
V(1,0)
8.0mV
4.0mV
0.0mV
0ms
5ms
10ms
15ms
20ms
25ms
30ms
35ms
40ms
45ms
V(3,0)
Time


Date/Time run: 02/26/96 20:50:50
Temperature: 27.0
7.5mV
7.0mV
6.5mV
6.0mV
44ms
48ms
52ms
56ms
60ms
64ms
68ms
72ms
V(3,0)
Time


Date/Time run: 02/26/96 20:59:35
Temperature: 27.0
8.0mV
7.9mV
7.8mV
7.7mV
7.6mV
7.5mV
7.4mV
100ms
150ms
200ms
250ms
300ms
V(3,0)
Time

5.5 Appendix 5 Code Page Selection IC35 (GAL 22V10)

```
ABEL Source File:
module MPXDEC;
flag '-r3';
Title 'SBMS-6027-A-JDC-R001
IC35 on S-81-5062-01
Copyright GEC-MARCONI LTD 1993
First used on SS-42141-024 dated 13/11/92';
"declarations
                mpxdec device 'p22v10';
"Inputs
        SELV1       pin 1; "select V1, low active
        SELV2       pin 2; "select V2, low active
        SELV3       pin 3; "select V3, low active

        A3          pin 4; "\
        A2          pin 5; " |-> Low active HEX
        A1          pin 6; " |   nibble from S1
        A0          pin 7; "/    (code page select V1)

        B3          pin 8; "\
        B2          pin 9; " |-> Low active HEX
        B1          pin 10;" |   nibble from S2
        B0          pin 11;"/    (code page select V2)

        D3          pin 13;"\
        D2          pin 14;" |-> Low active HEX
        D1          pin 15;" |   nibble from S3
        D0          pin 16;"/    (code page select V3)

"Outputs
        Q0          pin 17;"code page select     LSB
        Q1          pin 18;
        Q2          pin 19;
        Q3          pin 20;"                     MSB

        ERR         pin 21;
        VCC         pin 24;
        GND         pin 12;

        TRUE, FALSE     =     1,0;
        H,L             =     1,0;
        X,Z,C           =     .X.,.Z.,.C.;
Equations
        [Q0] .oe = TRUE;
        [Q1] .oe = TRUE;
        [Q2] .oe = TRUE;
        [Q3] .oe = TRUE;
```

```
ABEL Source File continued:
        [ERR] .oe = TRUE;
Q0      = !A0 & !SELV1 & SELV2 & SELV3
        # !B0 & SELV1 & !SELV2 & SELV3
        # !D0 & SELV1 & SELV2 & !SELV3;

Q1      = !A1 & !SELV1 & SELV2 & SELV3
        # !B1 & SELV1 & !SELV2 & SELV3
        # !D1 & SELV1 & SELV2 & !SELV3;

Q2      = !A2 & !SELV1 & SELV2 & SELV3
        # !B2 & SELV1 & !SELV2 & SELV3
        # !D2 & SELV1 & SELV2 & !SELV3;

Q3      = !A3 & !SELV1 & SELV2 & SELV3
        # !B3 & SELV1 & !SELV2 & SELV3
        # !D3 & SELV1 & SELV2 & !SELV3;

!ERR    = !SELV1 & SELV2 & SELV3  "O/P signal ERR is only
        # SELV1 & !SELV2 & SELV3  " low when a valid selection
        # SELV1 & SELV2 & !SELV3; " is made.

test_vectors
([SELV1,SELV2,SELV3,A3,A2,A1,A0] -> [Q3,Q2,Q1,Q0])
 [ L  , H  , H  , H, H, H, H] -> [ L, L, L, L];
 [ L  , H  , H  , H, H, H, L] -> [ L, L, L, H];
 [ L  , H  , H  , H, H, L, H] -> [ L, L, H, L];
 [ L  , H  , H  , H, H, L, L] -> [ L, L, H, H];
 [ H  , H  , H  , H, H, L, L] -> [ L, L, L, L];
 [ L  , H  , H  , H, L, H, H] -> [ L, H, L, L];

test_vectors
([SELV1,SELV2,SELV3,B3,B2,B1,B0] -> [Q3,Q2,Q1,Q0])
 [ H  , L  , H  , H, H, H, H] -> [ L, L, L, L];
 [ H  , L  , H  , H, L, H, H] -> [ L, H, L, L];
test_vectors
([SELV1,SELV2,SELV3,D3,D2,D1,D0] -> [Q3,Q2,Q1,Q0])
 [ H  , H  , L  , H, H, H, H] -> [ L, L, L, L]
 [ H  , H  , L  , H, L, H, H] -> [ L, H, L, H];
test_vectors
([SELV1,SELV2,SELV3] -> [ERR])
 [ L  , H  , H  ] -> [ L ];
 [ H  , L  , H  ] -> [ L ];
 [ H  , H  , L  ] -> [ L ];
 [ H  , H  , H  ] -> [ H ];
 [ L  , L  , H  ] -> [ H ];
 [ L  , L  , L  ] -> [ H ];
end MPXDEC;
```

5.6 Appendix 6 Modulator HT Stability Measurements

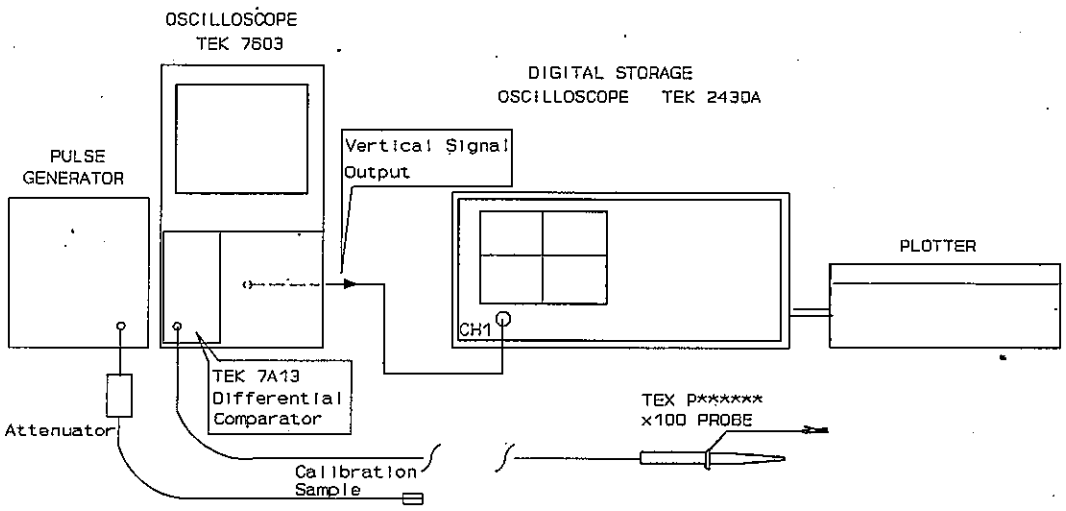


Figure 5.6.1

5.6.1 Measurement of the modulator HT stability is carried out using the equipment shown in Figure 5.6.1 above. In order to observe and record modulator H.T variations of typically 10mV on a DC level of typically -350v, over groups of 4 modulator charge & discharge cycles required the use of a Differential Comparator/Offset unit. The TEK 7A13 & associated oscilloscope frame allowed the adding of a DC (nominally 3.5 volts) level to compensate for the nominal -350v DC modulator HT level, and therefore enabling a Digital Storage Oscilloscope to monitor and record the small variations in HT level.

5.6.2 The timebase of the DSO is set to 500μs and to trigger on a negative falling edge of a pulse. The sensitivity controls of CH1 on the DSO are adjusted such that the the overall sensitivity of the complete measurement setup is 100mV/cm.

To check and adjust the sensitivity if required, the measurement setup is first calibrated, using a Pulse Generator and another calibrated reference oscilloscope.

5.6.3 The Pulse Generator is set up to produce a train of -ve pulses, at a PRF of 840 Hz and a pulse width of 200μs, to simulate the signal to be observed when the modulator HT is monitored. The peak -ve pulse level is set in turn to levels between 100mV and 20mV, level checked using an independent calibrated oscilloscope. The x100 probe is used to monitor the pulses at each level, and the sensitivity controls on the DSO adjusted to calibrate.

5.6.4 The x100 oscilloscope probe is then connected to a -HT point on one of the modules in the modulator. The transmitter is then operated, and allowed to warm up.

The DC Offset control on the differential comparator module is then trimmed such that a train of negative charge pulses are displayed on both oscilloscopes.

The DSO is then set to capture a sample sequence of 4 pulses, and the plotter used to take a hard copy. A number of samples may be taken to find a worse case variation. Figure 5.6.2 shows a typical plot of 4 charge/discharge cycles. The points on the plot of consequence are the lower right hand corners of the pulses, the instant of modulator discharge. To assess the variation accurately, the space between each horizontal graticule line, either side of the -ve peak levels, may be divided into 5 sub divisions, ie, 20mV/sub division.

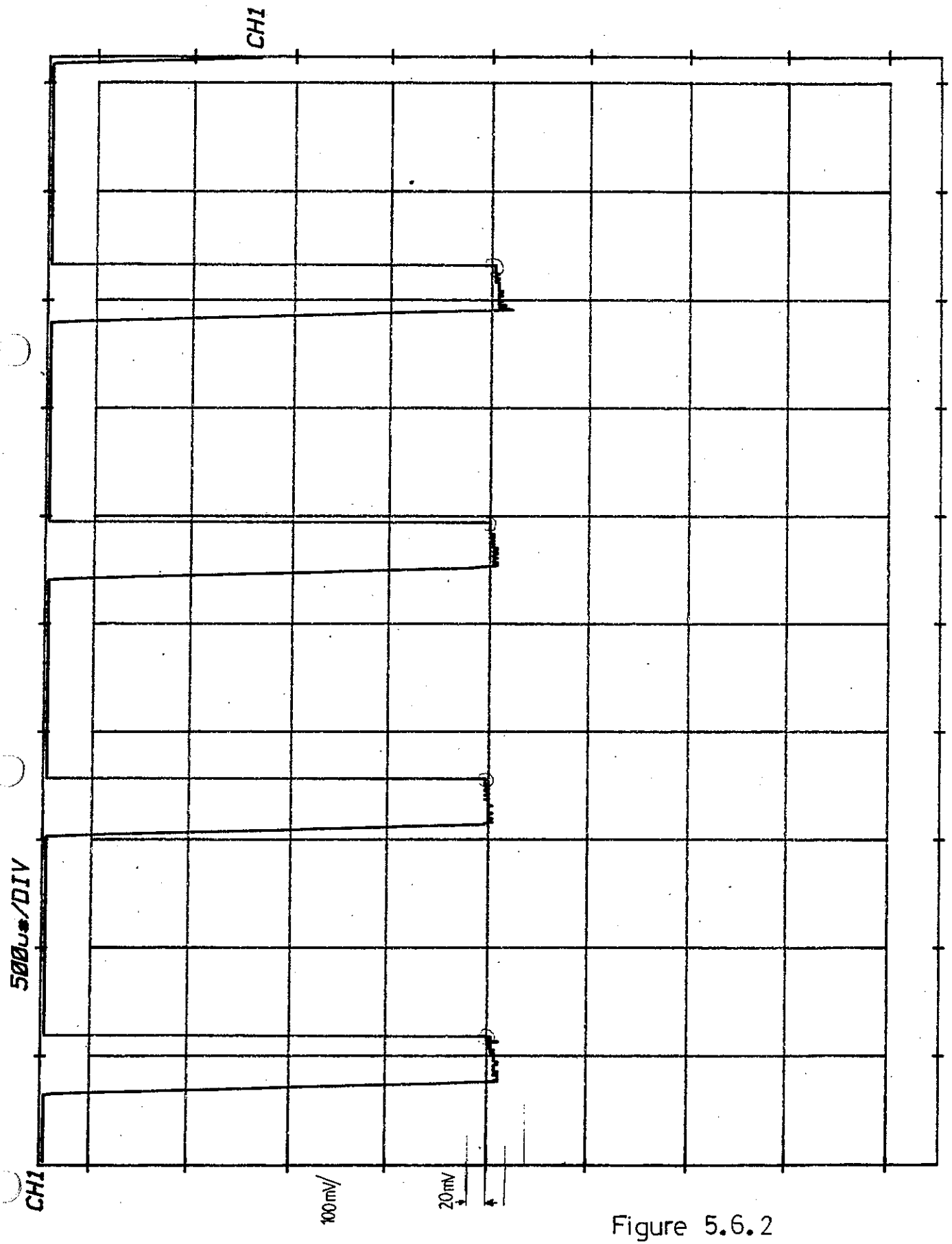


Figure 5.6.2

5.7 Appendix 7

S511H SYSTEM IMPROVEMENT FACTOR NOTE 5

DR. D J Heath

Future Systems (Radar)

MARCONI RADAR SYSTEMS

Technical Note
SG557-6160-DJH-DHWP15

File : IMPFAC1

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S511H SYSTEM IMPROVEMENT FACTOR NOTE 5

1 SUMMARY

It has been demonstrated that the S511H radar gives an improvement factor of approximately 50 dB against a stationary clutter source. Some adjustments to the system setup were necessary to make it possible to measure such a high figure on a 10 bit system.

2 SYSTEM MODIFICATIONS

2.1 System Noise Level

The usual definition of dynamic range is the ratio of the maximum signal which is representable, without distortion, in a system, to the rms noise level.

To use the dynamic range of the A/D fully, the peak to peak signal bipolar voltage at the input to the A/Ds should be 3.8 V. (This value is taken from the system set up instructions). This is equivalent to a peak voltage of 1.9 V and an rms value of $1.9/\sqrt{2} = 1.34$ V. In the normal system set up, the 'shoulder noise' should be set to 20 mV. If it is assumed that the observed 'shoulder noise' is equal to twice the rms noise (the shoulder noise is ± the rms noise) then this represents a dynamic range of:- $20 \times \log(1.34/0.01) = 42.5$ dB.

Another way of looking at this is to determine the dynamic range of the A/D converter in terms of the setting of the rms noise level. If it is assumed that 3.8 V is the largest non-saturated voltage into the 10 bit A/D, (i.e. ±1.9 volts into a processor with 10 bits including sign) then 1 bit is equivalent to $3.8/2^{10}$V = 3.7 mV.

Skolnik (Radar Handbook 2nd edition, page 3.40) gives the dynamic range of the A/D as:-

$$\text{Dynamic range (dB)} = 6N - 9 - 20\log(\sigma/\text{lsb})$$

where
- N is the number of bits including the sign
- σ is the rms noise in phase or quad channels
- lsb is the least significant bit voltage

The first part of this can be thought of as 6x(N-1) - 3, which is equivalent to $20\log(2^{(N-1)})$ with a 3 dB decrease due to the fact that each component contains half the noise power but may have to contain 100% of the signal power.

Using the values in the standard set-up instructions, σ = 10 mV, N is 10, and the lsb voltage has been derived as 3.7 mV. This formula then gives a dynamic range of 60 - 9 - 20log(10/3.7) = 42.4 dB.

Radar folklore often states that the setting of the rms noise level into an A/D converter is '2 bits' or '6 dB above a bit' and it can be seen that in this case the set-up instructions allow a slightly greater value than this. The value should be set as a trade off between system sensitivity and dynamic range. The dynamic range obviously increases as the rms noise level is decreased on the A/D scale. The system sensitivity however increases as the rms noise level is set to a higher level on the scale. This is because at higher levels the steps in the digital log levels are closer, and the CFAR mechanism can more accurately set the threshold level for the required false alarm rate.

As an aside, the dynamic range of the baseband mixer is approximately 50 dB and its value should not limit the dynamic range presented to the A/D.

The value of dynamic range given above demonstrate the difficulty of attempting to measure 50 dB system improvement factor. As a result it was decided, for this measurement, to decrease the rms noise level at the A/D input to 10 mV shoulder noise (5 mV rms noise), which allows a dynamic range of 48.4 dB. Even with this value, the clutter residue would have to be cancelled to below rms noise to show an improvement factor of 50 dB.

3 OTHER SYSTEM CONSIDERATIONS

In Note 4 of this series (SG557-6117-DJH) it was shown that the AFC was not controlling to the 'best' frequency. It was found that the acceptance window had been increased from ± 100 kHz to ± 300 kHz. This has been set back to its normal operational value.

The most important proviso of the following set of measurements is that even with this narrow acceptance window, the control of the frequency is not sufficient to show an improvement factor of 50 dB.

Only when the AFC is switched off and the magnetron frequency tuned by hand for minimum residue were improvement factors around 50 dB consistently demonstrated.

This was illustrated at the start of the day in which these results were taken. On switch on, no clutter residue could be seen. As time went by, the clutter residue actually grew (although it is known that the stability of the tube improves with time). This effect was due to the fact that on switch on the magnetron must have been close to the correct frequency (i.e. Fstalo - Fcoho). As the valve warmed up, the frequency drifted off- but not enough to cause the AFC to operate, i.e. still within the 100 kHz window.

At this time it is not known how accurately the frequency has to be controlled to give the required improvement factor. A useful measurement would be the calibration of the discriminator voltage with frequency.

Another factor which was important was the setting of the RF attenuator after the LNA. If the attenuator setting is set too low then the clutter saturates and an unrepresentative result may be obtained. If the attenuator setting is set too high then the clutter residue is so small compared to noise that there is a large error in the improvement factor measurement. In this latter case it is quite possible to obtain a situation where noise + clutter residue is less than noise because of the fluctuations in the noise value. This happened for the three reading when the attenuation was set to 40 dB. It was demonstrated that the return was just out of saturation with 30 dB attenuation.

4 RESULTS

Although the technique used for the improvement factor measurements can estimate clutter residue when it is below noise there is a smaller error in the measurement when the noise level is small compared to the residue. On the day of the measurements there was intermittent rain and at some times the background level was rain as well as noise. This had the effect of increasing the errors in the improvement factor as well as presumably giving a poorer value due to uncancelled rain residue.

4.1 Results Set 1

The first three results were taken with 30 dB RF attenuation after retuning the magnetron for minimum residue. Although 'minimum residue' is stated, in fact the residue disappears into noise which makes the absolute minimum difficult to identify. There was no rain over the permanent echo.

Run #	<..Non coherent channel.> rms values		<.....MTI channel.....> rms values		<Improvement> < Factor >
	Noise cell	Clutter cell	Noise cell	Clutter cell	(dB)
066	1.2	378.0	5.2	7.8	48.9
067	1.2	368.1	5.1	7.6	49.0
068	1.2	380.4	5.1	6.6	51.6

4.2 Results Set 2

The next set of results were taken some 45 minutes later, in the same conditions, without any manual retuning of the magnetron. It was quite clear from the display of linear unprocessed video that the magnetron frequency had drifted off, as clutter residue was clearly seen above the noise.

Run #	<..Non coherent channel.> rms values		<.....MTI channel.....> rms values		<Improvement> < Factor > (dB)
	Noise cell	Clutter cell	Noise cell	Clutter cell	
069	1.2	373.5	5.2	8.7	47.7
070	1.2	362.0	5.5	10.5	45.1
071	1.2	362.0	5.7	11.1	44.8

4.3 Results Set 3

The third set of results were taken with the rms noise reduced to a minimum value, which, in fact, is only just below the 10 mV shoulder noise set for the first two sets of results. However by this time there was a large rain cloud over the clutter cell and as a result the values were much more variable.

Run #	<..Non coherent channel.> rms values		<.....MTI channel.....> rms values		<Improvement> < Factor > (dB)
	Noise cell	Clutter cell	Noise cell	Clutter cell	
071	1.0	311.0	4.8	8.3	46.6
072	1.0	304.4	4.9	5.8	53.5
073	1.1	277.3	4.7	7.2	47.2
074	1.1	304.4	5.0	5.4	56.1

4.4 Results Set 4

The following four results, 76 to 79 inclusive, were taken with 40 dB attenuation. As a result, the residue would have been very small. In addition, the rain was still present over the clutter and these gave nonsensical values as the clutter residue plus noise was less than noise.

4.5 Results Set 5

Finally, the last two measurements were with the RF attenuation reset to 30 dB. The rms noise level was slightly higher than in the earlier runs (compare NCC noise level in 80 and 81 with the values in 66 to 71). The display indicated that the range cells with the noise sample and the clutter sample in them had only a small amount of rain clutter.

Run #	<..Non coherent channel.> rms values		<.....MTI channel.....> rms values		<Improvement> < Factor > (dB)
	Noise cell	Clutter cell	Noise cell	Clutter cell	
080	1.6	378.1	6.2	8.0	49.3
081	1.6	394.8	6.1	8.0	49.2

5 COMMENTS

It has been decided to average the dB values of these results. This is because a single high dB value unduly weights a linear average to a high value. For example, the 'linear average' of 60 db (1000 voltage ratio) and 40 dB (100 voltage ratio) is 550x or 54.8 dB, whereas an average of the dB values is 50 dB. The clutter residue is determined from the difference of the squares of the MTI channel clutter and noise cell results. The clutter residue is usually smaller than the noise and as a result, normal statistical variations in noise make large variations in the improvement factor. As shown above, a single high value biasses the result more than a single low result. However it is more a 'feeling in the water' rather than a certainty that this is the correct averaging process. For comparison the linear averaged result is also given.

The averages are taken over all results where the magnetron was tuned to 'minimum' residue. The runs in set 2 were not used as it was clear that the magnetron was off tune for this set.

Run #	Improvement Factor (dB)
66	48.9
67	49.0
68	51.6
71	46.6
72	53.5
73	47.2
74	56.1
80	49.3
81	49.2

Mean Improvement Factor = 50.2 dB (dB average) (The average of the linear values is 51.2 dB)

6 CONCLUSIONS

The results show that the whole system improvement factor capability is approximately 50 dB. Whether this capability can be realised in practice depends on whether the AFC can control the magnetron frequency to the required tolerance. At this time, the tolerance required is not known, except that it must be significantly less than ±100 kHz. This tolerance could be quantified by

a) calibration of the discriminator voltage versus frequency difference and

b) taking measurements of improvement factor versus discriminator voltage for a manually tuned magnetron,

c) hopefully (for greatest accuracy) when it is not raining!

5.8 Appendix 8

RF Pulse Jitter

5.8 Appendix 8 RF Pulse Jitter

Jitter may be defined as the variation in time delay between the front edge of the input trigger from the Signal Processor, and the front edge of the pulsed RF output of the magnetron.

Jitter degrades the overall MTI I/F of a radar as detailed in Appendix 2.

Front edge jitter on the S2055 TX pulse is primarily due to start up of oscillation in the magnetron, the back edge is relatively stable. Jitter due to the modulator triggering and signal processor pulse timing is negligible.

During development, jitter was measured using the test apparatus as detailed in Appendix 3.

Jitter in the Coaxial Magnetron

The source of the oscillating RF power in the coaxial magnetron takes the form of a closed loop (re-entrant) slow wave structure, consisting of a cylindrical array of 22 vanes (quarter wave resonant vanes) as shown in Figure 5.8.1.

The array is equivalent to a ring of coupled quarter wave transformers, providing a high impedance at the vane edges and a low impedance at the cylinder wall.

RF energy is transferred from the slow wave structure to an external coaxial resonator via coupling slots in the side wall, placed between every other pair of vanes to produce in phase oscillations. The alternate slot arrangement performs a similar function to vane straps used in a conventional magnetron. Coupling is such that the outer coaxial cavity resonant frequency stabilises and determines the frequency of oscillation. The most efficient mode of oscillation in the structure is where there is 180 deg phase difference in the voltages on adjacent vane edges, this mode is referred to as the pi(π) mode.

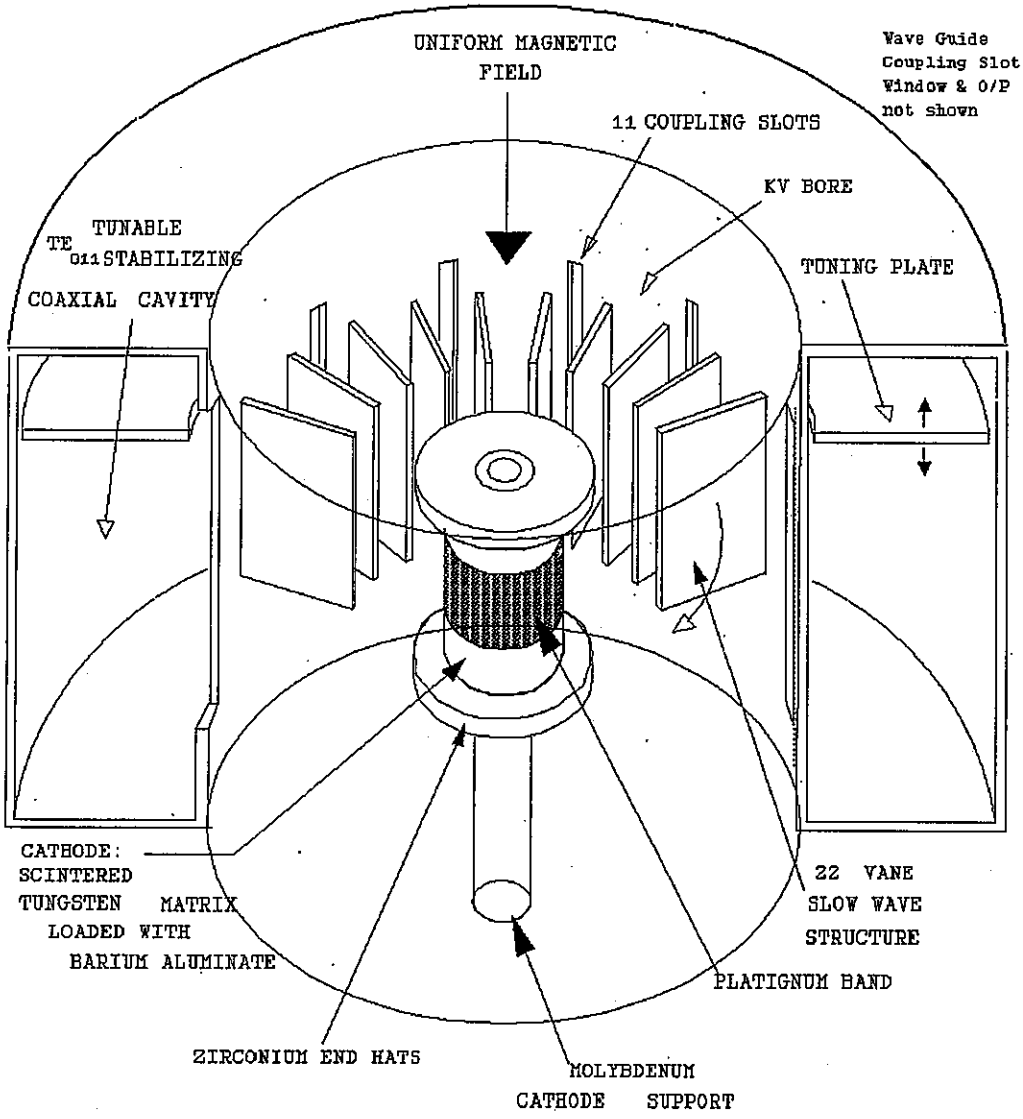

Figure 5.8.1

The energy used to induce the oscillations in the slow wave structure is derived from a rotating space charge of electrons in the space between the cathode surface and the anode vane edges. The circumferential space charge does not instantaneously rotate at the synchronous velocity relating to the π mode. As the cathode voltage falls from 0v towards -34 KV (nom), the electrons accelerate from the cathode surface and pass through a number of velocities which induce oscillations at a number of unwanted mode frequencies.

Spokes (bunches of electrons) are formed on the outer surface of the cylindrical space charge due to the acceleration & deceleration of the electrons caused by the oscillating electric fields on the vane edges. The rotating circumferential space charge caused by the perpendicular nature of the magnetic field upon the electric field does not have outward spokes initially. The formation of the final spoked rotating space charge is a gradual process, delayed by the undesirable interaction of electric fields on the vane edges at non π mode frequencies.

The variable nature in which energy is transferred to non π mode resonant parts of the structure causes the variable delay (jitter) in the build up of oscillations in the π mode.

To reduce the jitter as described above, the electrons need to be accelerated as quickly as possible, without causing arcs between cathode and anode through the velocities associated with lower order un-desirable mode frequencies, to minimise the amount of energy transferred. At approximately 70% of the peak cathode voltage amplitude, a voltage is reached, known as the "Hartree Voltage[2]" where the electron velocities are approaching that required to induce electric field fluctuations at the required π mode frequency. At the Hartree Voltage the acceleration needs to be reduced, to allow time for energy to be transferred from the rotating space charge into the resonant slow wave structure and closely coupled coaxial cavity.

The manufacturer of the valve always recommends approximate rates of rise, however rate of rise adjustments are necessary in order to achieve good jitter performance, with a particular type of modulator.

Rate of Rise profiling is performed by the Pulse Voltage Control Unit detailed in Chapter 3.

The rate of rise profile of the cathode voltage and magnetron current pulse (monitored by B13 as detailed in Chapter 1) is illustrated in Figure 5.8.2:-

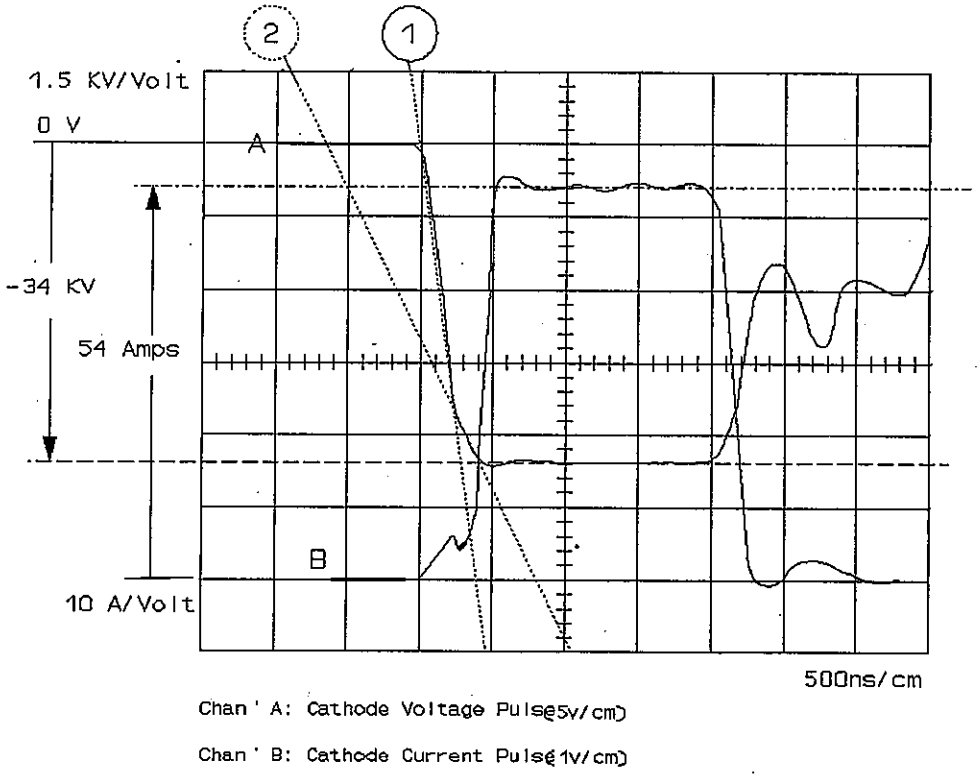

Figure 5.8.2

The above waveforms are precise copies from S2055 photographs, not idealised. The Cathode Voltage pulse was monitored using a Capacitor Divider type potentiometer, its fast response allows the rates of rise 1 & 2 to be measured. Note the smooth transition as the rate of rise changes.

Fine tuning of the rate of rise control and cathode temperature profiling was achieved by observing the distribution of jitter, in terms of Standard Deviation (Ref: Appendix 3).

Other factors affecting jitter and frequency stability

a, The cathode temperature and the subsequent volume of electrons available to form the space charge is critical with respect to obtaining best jitter performance.

b, Corona activity on any of the electrical connections at the magnetron cathode.

c, The quality of the impedance match (VSWR) presented at the output coupling slot from the coaxial cavity also affects jitter and frequency stability of the transmitted RF pulse.

Frequency pulling effect due to varying VSWR as the antenna rotates is minimised by the use of a Non-reciprocal differential phase-shift ferrite duplexer[1,2].The 'Magic T' in the duplexer provides isolation from reflected power due to VSWR variations.

d, Electron emission from other component surfaces other than the cathode.

e, Power level at which the valve is operated.

Operating the valve at a lower power level than maximum for the design improves jitter performance.

f, Use of Resonant Absorbers

Resonant absorber components are placed inside various parts of the magnetron to absorb and attenuate RF oscillations at non π mode frequencies (frequency selective loss).

They are made out of a dissipative material such as Beryllium/Silicon Carbide. Some of the mode frequencies are such that they will couple into the outer resonant cavity via the coupling slots, and so absorbers are placed under the tuning plate in the coaxial cavity. The positioning of the absorbers have a significant effect on jitter performance and reduce the efficiency of the valve.

6 Acknowledgments

† The general idea for the HT Stabilizer was suggested by Mr R. Richardson MIEE C Eng, consultant to the transmitter group at the time.

¶ The proto-type charging inductor was designed by Mr Simon Giles, GEC-Marconi Radar & Defence Systems LTD.

‡ The basic circuit architecture of the PVCU was derived with the assistance of the valve manufacturers GEC EEV LTD, Waterhouse Lane, Chelmsford.
Since the development, a similar basic circuit was found in a book[3].

§ The Solid State Modulator was designed by Mr Simon Giles, GEC-Marconi Radar & Defence Systems LTD.

7 Bibliography

1 Skolnik, M.I., *Introduction to Radar Systems*. New York: McGraw-Hill International Students Edition.Second Edition. 1983.

2 Collins, G.B., *Microwave Magnetrons*, New York: McGraw-Hill, First Edition. 1948. Page 30.

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