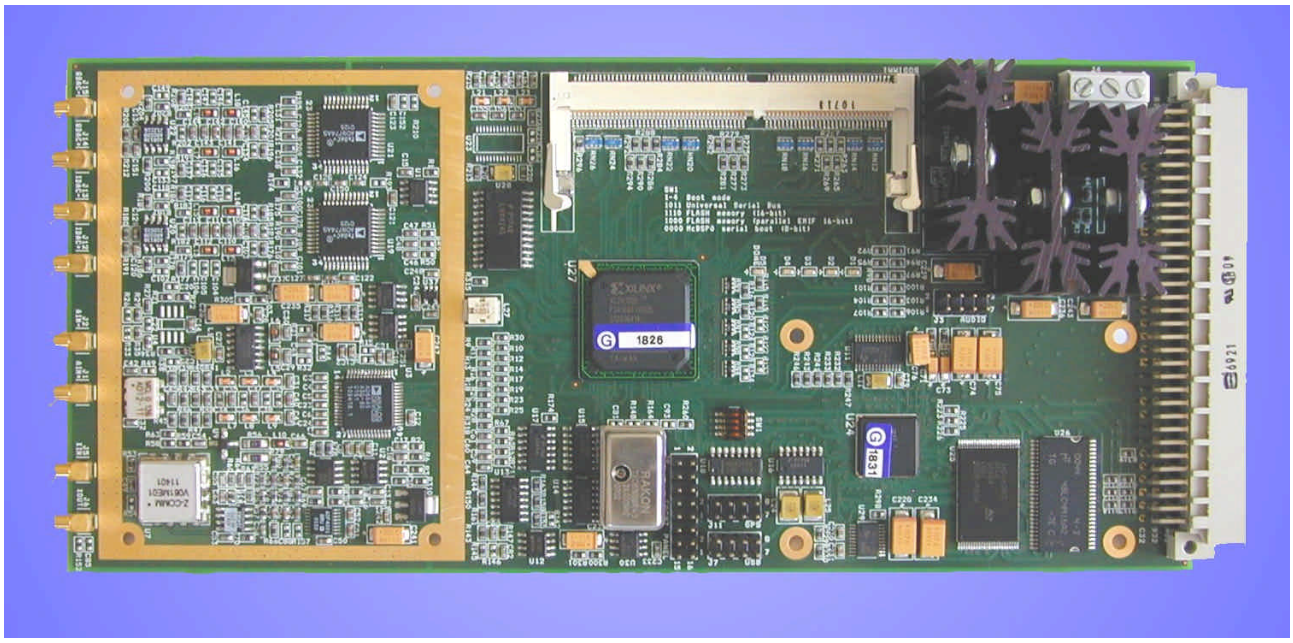
ASPE-1000
Advanced Signal Processing Engine

MULTIPLE ACCESS COMMUNICATIONS LIMITED



Features

- Input frequencies up to 200 MHz
- Up to 80 MSample/s sampling rate
- Variable analogue input gain
- Up to 1 million programmable FPGA gates
- Onboard signal processing
- USB interface for control and data transfer
- Internal or external clock
- Quadrature baseband outputs
- GPS module
- Expandable memory
- PC-controlled/standalone operation

Applications

- Configurable IF filtering
- Digital down-converters
- Programmable arbitrary waveform synthesis
- RF measurement equipment
- High speed data capture
- Drive testing cellular networks

Overview

The core of the advanced signal processing engine (ASPE) is a field programmable gate array (FGPA) connected to a digital signal processor (DSP), with a universal serial bus (USB) link providing a high-speed control and data interface. This combination of FPGA programmability and DSP processing power makes for a flexible platform suitable for many tasks.

The ASPE can be used as a signal source, sink or converter. Using the analogue-to-digital converter (ADC) and associated circuitry, the ASPE can be used for high-speed data capture or signal analysis. Using the digital-to-analogue converters (DACs), it can be used as a programmable arbitrary waveform synthesiser. Using both the ADC and the DACs, the ASPE can capture intermediate frequency (IF) signals and output processed baseband data. A stereo audio DAC is provided, for example for broadcast reception applications.

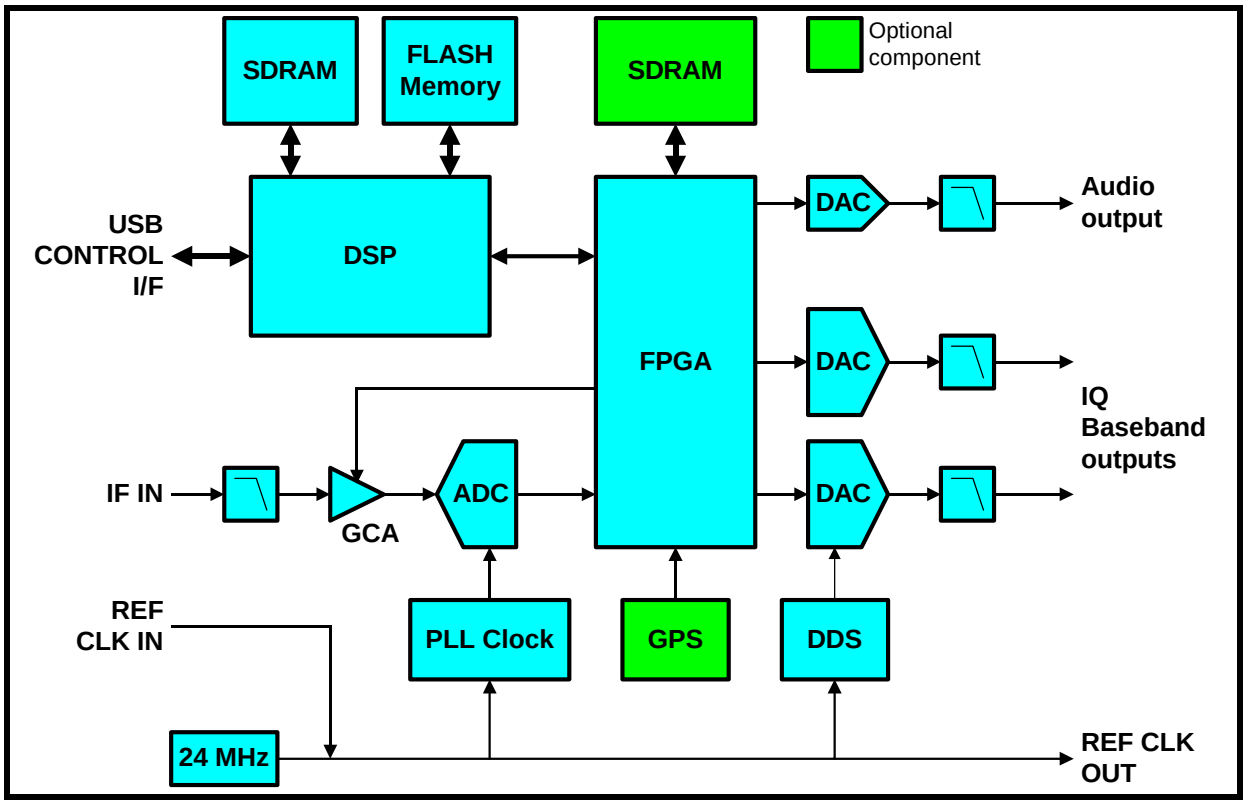
For applications requiring data storage, the FPGA can be partially configured as random access memory (RAM). If this is not sufficient for a given application, synchronous dynamic RAM (SDRAM) can be added, using standard SODIMM modules, to give up to 512 MBytes extra RAM. In addition the DSP has 128 Kwords of internal memory and 4 MBytes of external SDRAM and 2 Mbytes of FLASH for memory-intensive processing applications.

The ASPE can be booted from a PC over the USB, but for standalone applications a FLASH memory can be used to store the FPGA configuration and the DSP code.

A global positioning system (GPS) module can be added when geographical or time information is needed. An example would be drive testing of cellular networks, when the ASPE could capture radio frequency (RF) data which are uploaded along with positional information to a personal computer (PC) for later analysis.

Individual ASPE applications may need different form factors, and so the ASPE is offered as a fully verified circuit design that MAC Ltd will customise to your specific needs.

ASPE Block Diagram



System Components

FPGA
The FPGA is a 1,000,000 gate device from the Xilinx Virtex II family. The user can implement FPGA designs or use predefined personality modules. Each module has its own data sheet. FPGA configuration data can be downloaded from a PC or stored in a FLASH attached to the DSP.

DSP
The DSP is a Texas Instruments TMS320C5509 device that can run at 200 MHz. It has 128 Kwords of onboard RAM, a real-time clock, a watchdog timer, six DMA channels, three serial ports and a USB port. This port is used as the ASPE USB controller, and is fully compliant with the USB v1.1 (12 Mbit/s) specifications. It includes support for isochronous transfers.

ADC
The ADC is a 14-bit device (AD6645) that can sample at up to 80 MSample/s. It has a spurious free dynamic range of 100 dB, and a typical signal-to-noise ratio of 74 dB. Analogue input gain control has been provided on the ASPE to optimise the level of the ADC input signal. Input signals are in differential format.

DACs
The DACs are four times oversampling 14-bit devices (AD9774) that can accept data at up to 32 MSample/s and have an output rate of up to 128 MSample/s. They have a typical spurious free dynamic range of 79 dB and a typical signal-to-noise ratio of 76 dB. Two DACs are provided so that baseband (I and Q) outputs are available. The outputs are in differential format.

Direct Digital Synthesiser (DDS)
The DDS is used to supply a clock for the DACs. In this capacity it can generate clock frequencies up to 32 MHz with a resolution of better than 1 Hz.

FLASH
The FLASH is used to hold the FPGA configuration and DSP code for standalone ASPE applications. It can be up to a 16-Mbit device with access times of 90 ns.

SDRAM (DSP)
The DSP SDRAM is a PC100/PC133-compliant device containing up to 4 MByte of memory.

System Components (cont)

SDRAM (FPGA)

The optional FPGA SDRAM is a SODIMM device of the type used in laptop PCs. It is a PC133 device with a 64-bit data bus, and can contain up to 512 MBytes of memory.

GPS

The optional GPS module can track up to 12 satellites, and updates once per second. The acquisition time ranges from 15 s for a warm start with known data to five minutes when no satellite data are known. The positional accuracy is 5 m RMS.

Audio DAC

The audio DAC is a stereo device that can sample at up to 96 kHz, supports a variety of word sizes and has digital gain control with a range of 79 dB range.

Form Factor

The ASPE is supplied as an extended single Eurocard board (100 mm by 220 mm) suitable for use in rack-mounted systems. Power connections are supplied on a 96-way DIN41612 Type C backplane connector. The ASPE can be supplied in other form factors by arrangement.

Operating Conditions

The ASPE requires two input voltages, one at a nominal voltage of 5.5V, and the other at a nominal voltage of 15V. The operating temperature range is from 0ºC to 50ºC.

Development Tools

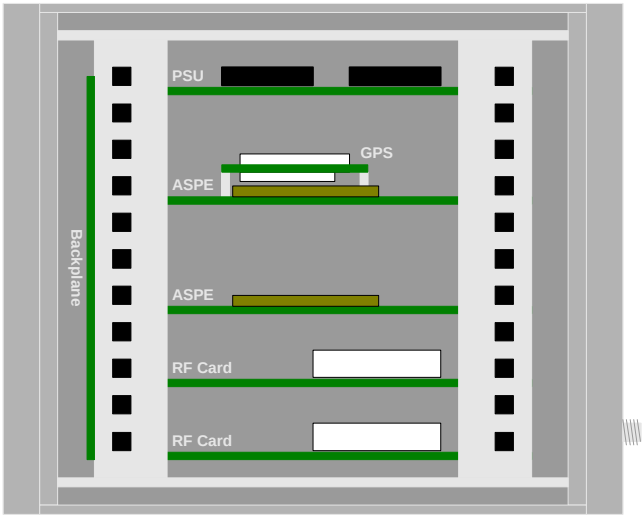
Several tools are required to program and use the ASPE. Xilinx Foundation Series FPGA tools are needed to construct FPGA designs, while Code Composer is required to write DSP software. A PC used for communications with the ASPE must have a USB port, and must use the MAC-supplied ASPE USB driver. It will need a serial port for GPS communications, and if any PC software is to be developed for a given application, either Microsoft Visual C++ or Borland Builder will be required.

Related Products

The ASPE is a central component within MAC Ltd's CatchAll Receiver platform, an open architecture platform permitting users to rapidly assemble customised receiver solutions. The CatchAll platform is based around a half-width 19" rack case, and can accommodate two ASPEs, two RF cards and a power supply card. The application of the CatchAll platform is defined entirely by the FPGA configuration and DSP software. Since these can both be changed at run-time, the CatchAll is a true software defined radio.

The specifications of available RF cards are subject to change, and customised versions can be supplied. Interested parties are asked to contact Multiple Access Communications Ltd directly for the latest information.

CatchAll Receiver Platform



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