CI9080ia – Universal I/Q IF Rx Interface for Wireless Communications

FEATURES

- **2.7V to 3.6V single supply operation**
- **1 MHz Signal bandwidth**
- **50 MHz baseband sampling frequency**
- **200 MHz maximum IF carrier frequency**
- **Programmable bandwidth with consumption control**
- **At least 70 dB SFDR for all standards**
- **Programmable full-scale input signal**
- **Built-in current consumption control for alternative operation modes (analog + digital)**
- **Flexible power down modes**
- **Built-in self-calibration of baseband offset**
- **20 mA typical current consumption**
- **Compact analog core area: 4.3 mm^2**

APPLICATIONS

Portable wireless units supporting combinations of multiple standards:

- **DECT, CDMA**
- **GSM, DCS 1800, PCS 1900**
- **PDC, AMPS, Tetrapol**

OVERVIEW

This low-power IF receive interface Macrocell is designed in 0.35µm CMOS technology.

Each channel includes the functions of IF to base-band mixing, anti-aliasing filtering combined with offset calibration, programmable gain amplification, A/D conversion and base-band digital filtering.

A/D conversion uses a 3rd order delta-sigma modulator with 3-bit quantizer. Feedback multibit D/A conversion is implemented with capacitor arrays linearized with a data-weighted averaging algorithm. The SFDR range achieves at least 70 dB for all the standards.

The high-speed bitstream is decimated by a SINC4 filter, followed by baseband FIR filters, tailor designed for CDMA and GSM.

Offset is cancelled with a self-calibration cycle.

All biasing and reference voltages are generated from an external bandgap circuit. Built-in bias control keeps current consumption at the minimum appropriate for the bandwidth actually being used.

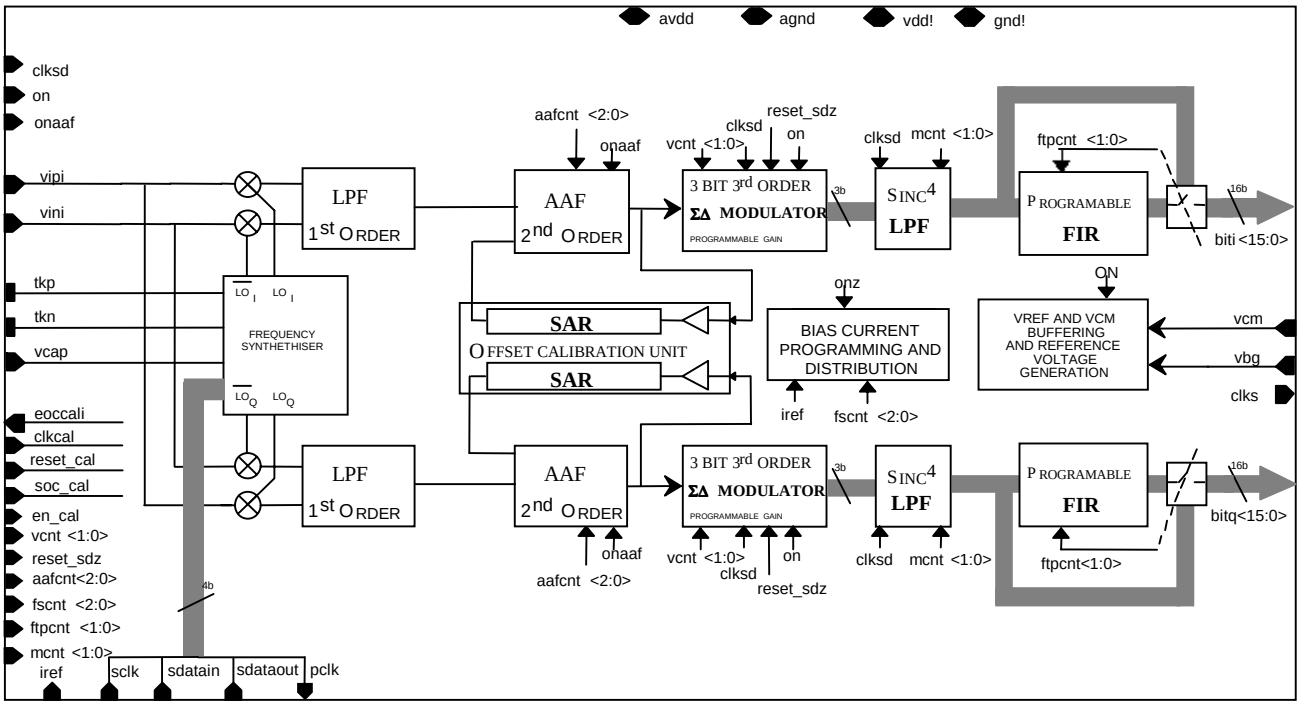
A power-down mode is included with less than 1 µA of standby current.

The Synthesizer is based on a PLL, using VCO with an external resonator tank, which is tuned to a fixed frequency in the specified range.

The Synthesizer uses internal programmable integer modulo dividers for the input reference signal (M divider) and for the feedback divider (N divider) generating waves in quadrature for the internal IF mixer.

TECHNOLOGY: Instantiated in 0.35µm CMOS with single-poly; retargetable towards any sub-micron CMOS technology with 2.5V/3V/5V supply.

FUNCTIONAL DIAGRAM



TAGUSPARK Edifício Inovação IV, Sala 733
2780-920 Porto Salvo **PORTUGAL**
TEL: (+351) 21 033 63 00 **E-mail:** chipidea@chipidea.com
FAX: (+351) 21 033 63 96 **URL:** http://www.chipidea.com