Features

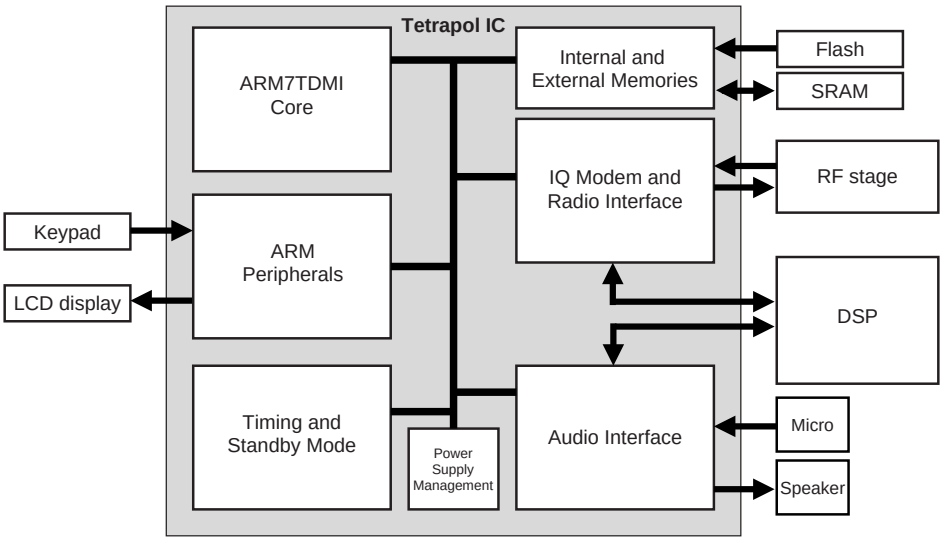
- **Atmel Voice CODEC**
  - **Digitizes and Encodes Speech Signals from the Microphone**
  - **Transforms into Analog Format Speech Signals for the Speaker**
  - **Based on State-of-the-Art Analog-to-Digital Conversion Techniques**
  - **Direct Interface to Off-Chip DSP for Compression/Decompression and Treatment of the Signal Stream**
- **Atmel IQ Modem**
  - **Modulates/Demodulates Compressed Digital Speech Signal Stream for Transmission/Reception by the RF Interface**
  - **Interface to DSP**
- **ARM7TDMI™ ARM® Thumb® Processor**
  - **High-Performance 32-bit RISC Architecture**
  - **High-Density 16-bit Instruction Set**
  - **Leader in MIPS/Watt**
  - **Embedded ICE (In Circuit Emulation)**
- **ARM7TDMI Peripherals, Including a Keypad Interface and LCD Display Driver**
- **Analog-to-Digital (ADC) and Digital-to-Analog (DAC) Converters as Part of the Microcontroller Interface**
- **State-of-the-Art Sigma-Delta DACs for Offset and Frequency Control of the RF Interface**
- **DACs for Ramp-up and Ramp-down Control**
- **On-chip RAM and ROM for Use by the ARM7TDMI Core**
- **Phase-Locked Loop (PLL) Cells for Stable Clock Sources**
- **Power Management Circuitry to Optimize Power Consumption**
- **Test Circuitry, Including JTAG Boundary Scan Cells**

Description

The Atmel Tetrapol baseband integrated circuit integrates, on a single chip, all the functions of the Tetrapol digital radio handset. It picks up the outgoing voice signal stream from the microphone, digitizes, compresses and modulates it, before sending it to the RF interface for transmission. The incoming radio signal stream is demodulated, uncompressed and transformed into analog format for the speaker. Control instructions are accepted from the keypad, and status information is displayed on the LCD screen. An off-chip DSP performs the compression/decompression steps.

The chip conforms to the Tetrapol standard, a European-wide standard for secure digital police mobile radio networks. It has already been adopted by a number of police forces and security agencies.

Figure 1. Tetrapol IC System Block Diagram



Tetrapol Baseband Integrated Circuit

Preliminary

Rev. 1269A–01/99

Pin Configuration

Figure 2. Tetrapol IC Pinout in BGA256 Package

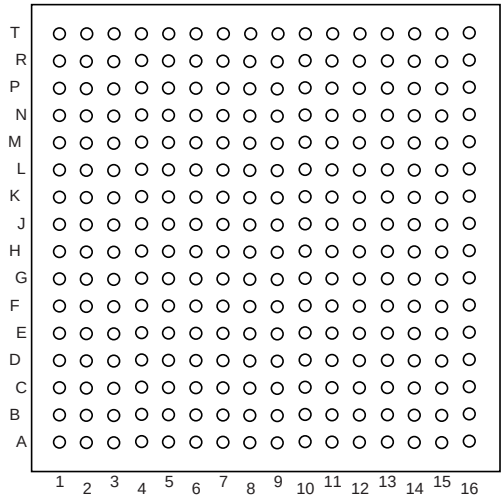


Table 1. Tetrapol IC Pin Description

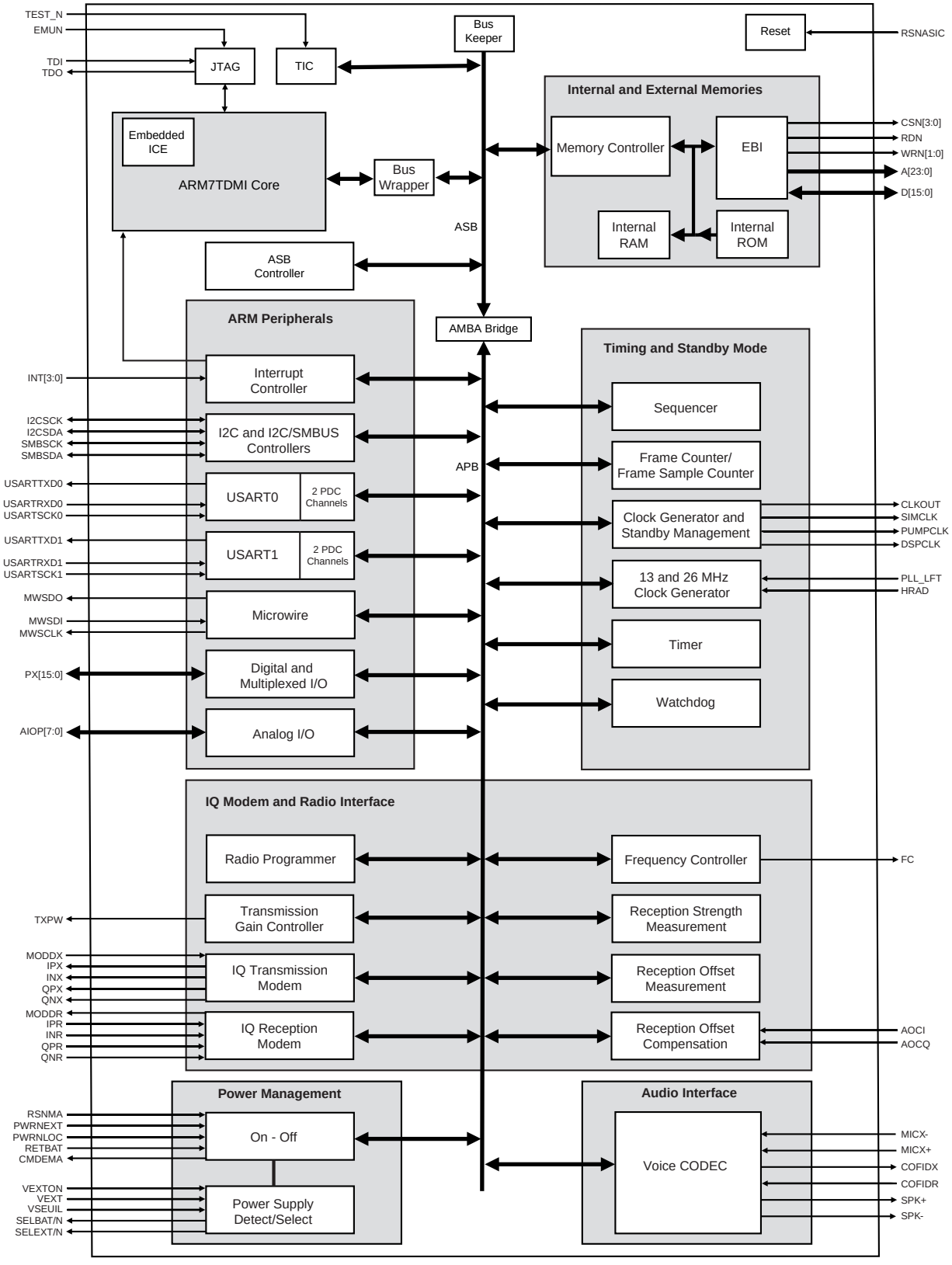
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	VCMIN	C1	AIP3	E1	RSNASIC	G1	RCT
A2	VCMOUT	C2	AIP7	E2	RSNMA	G2	SELBATN
A3	INX	C3	AIP6	E3	CMDEMA	G3	SELBAT
A4	IPX	C4	MODREF	E4	IOGNDR	G4	V3P
A5	IPR	C5	P5.6	E5	P4.15	G5	P3.2
A6	INR	C6	P5.1	E6	P4.12	G6	P3.0
A7	VCMPAD	C7	P5.3	E7	P4.11	G7	P3.6
A8	QNR	C8	P5.8	E8	P4.9	G8	P3.12
A9	QPR	C9	P5.5	E9	P4.7	G9	P3.10
A10	RADREF	C10	P5.9	E10	P4.4	G10	P3.4
A11	TXPW	C11	P5.7	E11	P4.2	G11	P3.7
A12	AOCQ	C12	P5.10	E12	P4.0	G12	P3.15
A13	AOCI	C13	RADGNDR	E13	GNDL	G13	GNDL
A14	D15	C14	D9	E14	D0	G14	A21
A15	D14	C15	D8	E15	WRN0	G15	A19
A16	D13	C16	D7	E16	RDN	G16	A20
B1	AIP4	D1	AIP0	F1	PWRNLOC	H1	VSEUIL
B2	AIP5	D2	AIP2	F2	RETBAT	H2	VEXTON
B3	QNX	D3	AIP1	F3	PWRNEXT	H3	GNDP
B4	QPX	D4	IOVREF	F4	IOV3A	H4	V3PA
B5	P5.4	D5	IOGNDA	F5	P4.14	H5	P3.3
B6	P5.0	D6	GNDL	F6	P4.13	H6	P3.1
B7	P5.2	D7	MODGNDA	F7	P4.10	H7	P3.5
B8	P5.14	D8	MODV3A	F8	P4.8	H8	P3.8
B9	P5.13	D9	VCC	F9	P4.6	H9	P3.14
B10	P5.12	D10	RADGNDA	F10	P4.5	H10	P3.13
B11	P5.15	D11	RADV3A	F11	P4.3	H11	P3.9
B12	P5.11	D12	FCGND	F12	P4.1	H12	P3.11
B13	FC	D13	FCVREF	F13	VCC	H13	VCC
B14	D12	D14	D5	F14	A23	H14	A17
B15	D11	D15	D3	F15	GCSN2	H15	A16
B16	D10	D16	D4	F16	GCSN0	H16	A15

Table 1. Tetrapol IC Pin Description (Continued)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
J1	SELEXTN	L1	TCK	N1	VDAC	R1	MIC2+
J2	VEXT	L2	TMS	N2	EAIN	R2	MIC1-
J3	SELEXT	L3	EMUN	N3	MIC0-	R3	MIC1+
J4	VCC	L4	GNDL	N4	GNDL	R4	COUT
J5	P2.6	L5	P1.2	N5	COFIV3A	R5	MODCLKX
J6	P2.5	L6	P1.1	N6	COFIGNDA	R6	USART1SCK1
J7	P2.9	L7	P1.5	N7	PAGNDA	R7	COFOFSR
J8	P2.12	L8	P1.3	N8	PAV3A	R8	MODDX
J9	P2.14	L9	P1.11	N9	VCC	R9	MODCLKR
J10	P2.4	L10	P1.10	N10	GNDL	R10	CLKOUT
J11	P2.2	L11	P1.12	N11	HRADVCCA	R11	PLL_LFT
J12	P2.0	L12	P1.15	N12	HRADGNDA	R12	GCSN3
J13	GNDL	L13	VCC	N13	VCC	R13	ROMN
J14	A8	L14	A2	N14	INT0	R14	GCSN1
J15	A10	L15	A4	N15	INT2	R15	A13
J16	A11	L16	A3	N16	INT1	R16	A9
K1	TDO	M1	CONS1	P1	VMID	T1	MIC2-
K2	TDI	M2	CONS0	P2	VCM	T2	VBG
K3	TRSTN	M3	NC	P3	MIC0+	T3	SPK-
K4	VCC	M4	VCC	P4	USART1TXD2	T4	SPK+
K5	P2.10	M5	P1.6	P5	COFIDX	T5	MODFSR
K6	P2.7	M6	P1.7	P6	DSPCLK	T6	COFIFSX
K7	P2.8	M7	P1.0	P7	MODFSX	T7	COFIFSXR
K8	P2.11	M8	P1.4	P8	COFIDR	T8	MODDR
K9	P2.13	M9	P1.8	P9	DSPCLKR	T9	USART1RXD1
K10	P2.15	M10	P1.9	P10	COPCLK	T10	PUMPCLK
K11	P2.3	M11	P1.13	P11	TESTN	T11	HRAD
K12	P2.1	M12	P1.14	P12	PLL_TEST	T12	D1
K13	GNDL	M13	GNDL	P13	D2	T13	D6
K14	A5	M14	A0	P14	A12	T14	WR1N
K15	A7	M15	INT3	P15	A22	T15	NC
K16	A6	M16	A1	P16	A14	T16	A18

Block Diagram

Figure 3. Tetrapol IC Block Diagram



Architectural Overview

ARM7TDMI Microcontroller Core

The ARM7TDMI processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications.

JTAG and Test Interface Controller

The ARM7TDMI uses the serial JTAG port for processor emulation. The parallel TIC, multiplexed with the chip address and data buses, enables access to internal registers while bypassing the processor.

Additional test interfaces are:

- Boundary Scan Interface
- Device-specific test interface
- Atmel-specific test configuration

AMBA Bus and Bridge

The system architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). The ASB is designed for maximum performance. It interfaces the processor with the on-chip 32-bit memories and the external memories and devices by means of the External Bus Interface (EBI). The APB is designed for accesses to on-chip peripherals and is optimized for low power consumption. The AMBA Bridge provides the interface between the ASB and the APB.

Internal and External Memories

Memory Controller

The memory controller manages internal and external memory access. It is connected to the internal and external memory blocks by means of the ASB and the External Bus Interface.

Internal RAM and ROM

The internal RAM is a memory of 512 x 32 bits which can be used for either instructions or data. It is accessible in 16- and 32-bit modes.

The internal ROM is a memory of 256 x 32 bits. It contains the boot program.

External Bus Interface

The EBI provides fast, flexible access to 8- or 16-bit external memory blocks or compatible devices. It is fully programmable and can address up to 64M bytes.

Timing and Standby Mode

Sequencer

The sequencer is a finite-state machine which triggers actions at precise time intervals.

Frame and Frame Sample Counters

These are programmable counters - modulo 200 for the frame counter and modulo 320 for the frame sample counter.

Clock Generation and Standby Management/ 13 and 26 MHz Clock Generation

The clock generation function generates and controls the permanent 26 MHz clock, from which the permanent 13 MHz clock is generated.

Timer

The timer block is made up of three 16-bit programmable timers.

Watchdog

A watchdog timer prevents system lock-up in the case of entry into an endless loop.

ARM Peripherals

Interrupt Controller

The device incorporates an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines.

I^2C and I^2C/SMBUS Controllers

The device contains two serial interfaces managed by two independent I^2C controllers. The standard I^2C interface enables exchanges with I^2C-type accessories, whether master or slave. It is multiplexed with the digital I/O ports which permits the connection of parallel access accessories on the same wires.

The SMBUS interface is dedicated to exchanges between the battery and the charger.

The two interfaces are independent of each other.

USART

The chip provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are each connected to a Peripheral Data Controller. This configuration allows data to be transferred with minimal processor intervention.

Microwire®

The Microwire is a serial interface between external peripherals and the ARM7TDMI microcontroller.

Digital and Multiplexed I/O
The chip contains 5 bidirectional I/O ports of 16 parallel bits. Some of these are multiplexed with functional I/Os.

Analog I/O
Eight analog inputs are available. They permit the measurement and comparison of minimum levels. Maximum levels can be measured with an interrupt trigger. Four of the eight inputs are multiplexed with the analog outputs. 8-bit low-power analog-to-digital and digital-to-analog converters are used. The DACs are buffered to drive external resistive-capacitive loads.

IQ Modem and Radio Interface

Radio Programmer
This block creates the serial interface between the internal bus and external radio circuits. It can program up to 8 radio circuits and transmit data packets of up to 56 bits. Programming is done by the ARM core.

Frequency Controller
The Frequency Controller produces an analog signal proportional to the required radio frequency. The signal is derived from digital data via a compact single-bit sigma-delta DAC with 10-bit resolution.

Transmission Gain Controller (Ramp-up, Ramp-down)
Transmitted signal power, as well as ramping up and ramping down at the beginning or end of a transmit burst, are controlled by low-power 8-bit Nyquist data converters. They are buffered to drive external resistive-capacitive loads.

Reception Strength Measurement
This block measures the average strength of received signals sampled during a given interval.

Reception Offset Measurement
This module measures the offset of received samples at given intervals.

Reception Offset Compensation
This block provides the necessary correction to compensate the natural offset of demodulated signals. Fine control steps are achieved by using oversampled multibit DACs with 14-bit resolution.

IQ Transmission and Reception Modem
The Baseband Modem (CODEC) performs A/D and D/A conversion of the I and Q waveforms according to the GMSK standard.

For the best dynamic performance in terms of SNR and THD, both transmission and reception chains are based on noise-shaped oversampled architectures. Each transmit channel includes:

- $Sinc^3$ interpolator
- Drop compensator
- 10-bit current-steering DAC
- Second-order continous time filter with buffer

The differential offset for both I and Q can be reduced to 1 mV after performing a calibration cycle.

The I/Q receiver employs a delta-sigma ADC for each channel, the bitstream of which is decimated by a $sinc^3$ digital filter. A Parks McClellan FIR filter is included to assure rejection of out-of-band components.

Power Management

On - Off
The on-off function controls power up and power down and ensures power up in a correctly initialized state.

Power Supply Detect/Select
The power supply function detects the presence of an external power supply and selects the power source from the battery or the external supply.

Audio Interface

Voice CODEC
The Atmel Voice CODEC contains seperate reception and transmission channels. The transmission channel filters the incoming microphone signals, converts them to digital signals, filters and then transmits the resulting data serially.

The reception channel filters the incoming serial digital signal, converts it to an analog signal and then amplifies/attenuates and transmits the signal to a speaker.

Digital signals interface directly with the off-chip DSP.

Sigma-delta conversion is used in both transmit and receive. The powerdown scheme allows only the transmit or receive section to be powered up. A control register programs all voice CODEC functions: multiplexing the three microphone inputs, bypass of the microphone amplifier, selection of auxiliary input, setting of TX and RX PGA gains, and loopback test mode.

Electrical Characteristics

V_{DD} = 2.4V to 3.6V, T_A = -40°C to 85°C (worst case of process)

Table 2. Device Characteristics

Symbol	Parameter	Description/Conditions	Min	Typ	Max	Units
V_{EXT}	External Voltage	Dynamic	0		3.3	V
V_{SEUIL}	Threshold Voltage	Dynamic	0		3.3	V
$SEL_{XXX(X)}$	TTL I/O Current Levels	Low Level Current Load			4	mA
		High Level Current Load			0.5	mA
	Static Power Consumption	Excluding load and V_{CC} = 0		TBD	25	µA

Table 3. Voiceband CODEC Characteristics

Symbol	Parameter	Description/Conditions	Min	Typ	Max	Units
ADC Channel						
G_{XAL}	Gain Tracking Error	ref @-10 dB, 3 dBm0 to -40 dBm0	-0.5		0.5	dB
THD	Total Harmonic Distortion	0 to -6 dBm0		-65	-48	dB
	Idle Channel Noise				-67	dBm0p
DAC Channel						
R_{XAL}	Gain Tracking Error	ref @-10 dB, 3 dBm0 to -40 dBm0	-0.5		0.5	dB
THD	Total Harmonic Distortion	0 to -6 dBm0			-48	dB
	Idle Channel Noise				-74	dBm0p

Table 4. IQ Baseband Modem (CODEC) Characteristics

Symbol	Parameter	Description/Conditions	Min	Typ	Max	Units
Transmit DAC						
N	Resolution			10		bits
BW	Signal Bandwidth		12.5			kHz
f_S	Sampling Rate			40		kHz
THD	Total Harmonic Distortion	$V_{IN} = 2V_{PP}$, F_{IN} = 2 khZ, BW = 0 to 8 kHz			-56	dB
V_{OFF}	Differential Offset, post cal		-1		1	mV
Receive ADC						
N	Resolution		12			bits
BW	Signal Bandwidth		5			kHz
	Gain Flatness	BW = DC to 5 kHz	-0.1		0.1	dB
	Out-of-Band Attenuation	f > 6 kHz	-55			dB
f_S	Sampling Rate			2		MHz
THD	Total Harmonic Distortion	$V_{IN} = 1V_{PP}$, F_{IN} = 2 kHz, BW = 0 to 8 kHz			-50	dB
SNR	Signal-to-Noise Ratio	$V_{IN} = 2V_{PP}$, F_{IN} = 2 kHz, BW = 0 to 8 kHz	72			dB

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