EXHIBIT # 10

FCC Requirements CRF 47 Part 2.1033,c (10)

Frequency, Spurious and Power Control

JXBLMDSXP4-DS3

EXHIBIT 10 Frequency Control for 28 to 31 GHZ LMDS Radio

The transmit frequency is controlled by a DDS modulator device (AD7008) made by Analog devices. The AD7008 direct digital synthesis (DDS) chip is a numerically controlled oscillator employing a 32-bit phase accumulator.

$$\text{DDS(frequency)} = \frac{TX_{FREQUENCY}(Hz)}{4096} \text{ X } 214.7483648$$

To arrive at a program value for the DDS the ODU microprocessor takes the desired Transmit frequency in Hertz and divides by 4096 then multiplies by 2^32 / 20,000,000

AD7008 Theory of operation

The internal circuit of the AD7008 consists of four main sections. These are:

Numerical Controlled Oscillator (NCO) + Phase Modulator
SIN and Cosine LOOK UP tables
In Phase and Quadrature modulators
Digital to Analog Converter

The first section consists of two frequency select registers, a phase accumulator and a phase offset register. The main component of the NCO is a 32 bit phase accumulator which accumulates a phase step on every clock cycle. The value of the phase step determines how many clocks cycles are required for the phase accumulator to count 2π radians (i.e., one cycle of the output frequency). the output frequency, f_{OUT} , is given by:

$$f_{OUT} = \frac{Phase\_Step}{2\pi} f_{CLOCK} = \frac{\Delta Phase}{2^{32}} f_{CLOCK}$$

$$0 \leq \Delta \text{ Phase} \leq 2^{32} - 1$$

The input to the phase accumulator (i.e., the phase step) can be selected either from the FREQ0 Register or FREQ1 Register and this is controlled by the FSELECT pin. The XP-4 design uses the FREQ0 Register only and the serial assembly mode. The transfer control pins are hardwired (see table).

This allows binary frequency shift keying to be easily implemented. The two FSK frequencies can be loaded into FREQ0 and FREQ1 and selected using the FSELECT pin. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies. More complex frequency modulation schemes, such as GMSK, can be implemented by updating the contents of these registers.

Following the NCO, a phase offset can be added to perform phase modulation using the 12 bit PHASE Register. The content of this register are added to the most significant bits of the NCO.

	TC1	TC0	Destination Register
XP4 hardwired register selection	0	0	FREQ0 Register
	0	1	FREQ1 Register
	1	0	PHASE Register
	1	1	IQMOD Register

Table 1 - AD7008 Destination Register selection

	TC3	TC2	Destination Register
	0	0	Parallel Assembly Register
	0	1	Not used
	1	0	Parallel Assembly Register
XP4 hardwired register selection	1	1	Serial Assembly Register

Table 2 - AD7008 Source Register selection

The output of the phase accumulator is converted to an amplitude signal by means of an Sine/Cosine ROM look up table. Although the NCO contains a 32 bit accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is both impractical and unnecessary as this would require a look up table of 2^{32} entries. It is necessary only to have sufficient phase resolution in the look up tables such that the dc error of the output waveform is dominated by the quantization error in the DAC. this requires the look up tables to have two or more bits of phase resolution than the 0 bit DAC.

Because no amplitude modulation is required, the IQ multipliers are bypassed. The sine output is directly sent to the 10 bits DAC. This device includes a high impedance source 10 bit DAC, capable of driving wide range of loads at different speeds. Full scale output current can be adjusted, for optimum power and external load requirements, through the use of a single external resistor.

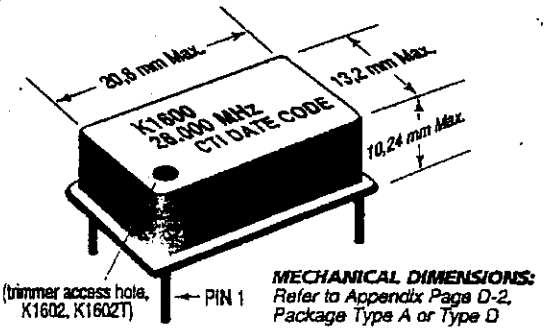
The DAC can be configured for single or differential ended operation. A single ended mode is used in the XP-4 radio. The negative output is tied directly to ground. In the XP-4 radio the frequency is programmed from the following equation.

$$f_{OUT} = \frac{Phase\_Step}{2\pi} f_{CLOCK} = \frac{PROGRAM\_value}{2^{32}} * 20Mhz$$

One AD7008 DDS is used for the transmitter and another for the receiver. They are controlled through the QSM in the MC68332 microprocessor.

CHAMPION
K1600 SERIES

- ▲ **APPLICATIONS** Reference Clock; Phase-Locked Loops (PLL's); Signal Tracking; Clocking "Sync" to NTSC Video Standards
- ▲ 2.0 to 30.0 MHz Frequency Range
- ▲ ±2.0ppm Frequency Stability
- ▲ ±1.0ppm Available (K1601 Series)
- ▲ -40°C to +85°C Operating Temperature
- ▲ +0.5V to +4.5V Control Voltage
- ▲ Manual Frequency Adjustment Capability Option
- ▲ Hermetically Sealed Package Options
- ▲ TTL/CMOS and Sinewave Outputs



MECHANICAL DIMENSIONS: *Refer to Appendix Page D-2, Package Type A or Type D*

ELECTRICAL SPECIFICATIONS

MODEL	K1602	K1602TE	K1602T	K1603T
Frequency Range (MHz)	16 to 30	2 to 30	2 to 30	2 to 30
Package Type (Page D)	Type D	Type A (TC)VCXO	Type D	Type A
Frequency Stability (ppm)				
Overall	Inclusive of temperature, voltage, load.			
25° Calibration	±1.5			Inclusive
Aging (10 years)	<±2ppm			Inclusive
0°C to 55°C	±1.0			
-40°C to +85°C	±2.0			±4.6
Frequency Control Function:				Not Available
Voltage Control	Included		Not Available	
Minimum Deviation (ppm)	±28	±28 ("TEW" = ±40ppm)		
Min. Deviation Sensitivity (ppm/V)	+14			
Nominal Control Voltage (V)	2.5			
Control Voltage Range (V)	0.5 to 4.5			
Linearity	10%			
Manual Adjustment	Included	Not Available	Included	
Minimum Adjustment (ppm)	±5		±5	
Output	1.0V p-p min.	Refer to Page B, Table 2		
	"Clipped" Sinewave			
	10 Kohms/10pF			
Symmetry (%) CMOS/TTL	-	45/55 <14 MHz; 40/60 ≥14 MHz		
Input Current (mA)	<2.0	<20		
Supply Voltage (V)	+5.0 ±5%			
Temperature Range (°C)				
Operable	-40°C to +85°C			
Storage	-40°C to +85°C			
Start Up Time (ms)	<5	<20	<10	
Test Circuit Diagram	Refer to Page B, Figure 3 (K1600T) or Figure 4 (K1600).			

Typical Phase Noise (dBc/Hz)	
Offset from Carrier	
10 Hz	-70
100 Hz	-95
1 KHz	-120
10 KHz	-140
100 KHz	-150

ORDERING INFORMATION

K160XX- Specify Frequency

- "Blank" = Sinewave output
- "T" = TTL/CMOS output
- "TE" = TTL/CMOS output, hermetic package
- "TEW" = "TE" version with ±40 ppm min. deviation

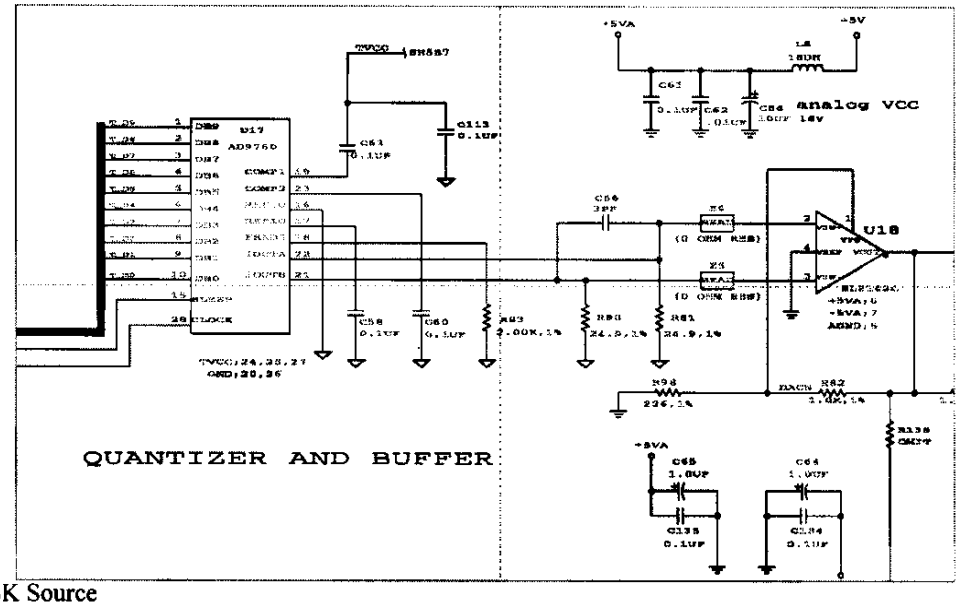
- "1" = 0°C to 55° Operating Temp., ±1ppm
- "2" = -40°C to 85°C Operating Temp., ±2ppm
- "3" = -40°C to 85°C Operating Temp., ±4.6ppm, inclusive, hermetic package

innova
3325 S. 116TH ST BLDG 2 SEATTLE, WA 98168
(206) 439-9121 (206) 439-2700 FAX

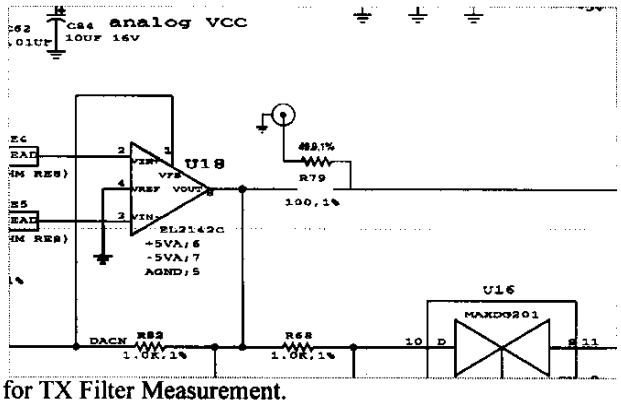
SIZE	DWG NO.	REV
A	394-000001-000	C
	CAD FILE: 39400001.SCD	SHEET: 3

Transmitter Spurious and Modulation Control

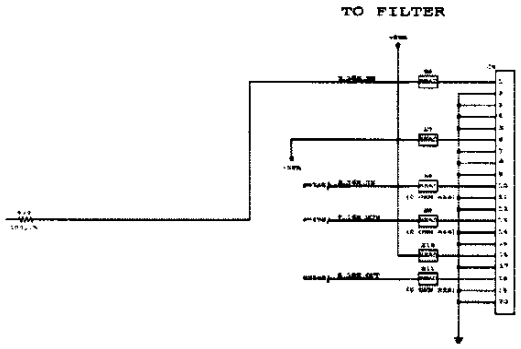
1. Introduction
   1.1. This document describes expected and measured transmit filter on DS-3 4FSK Signal Processor Printed Circuit Assembly (SigProc).



   1.2. Fig. 1 4FSK Source
      1.2.1. The 4FSK waveform is sourced by a 10-Bit Video DAC AD9760-50. At present the DAC only outputs one of four levels, and all filtering is performed by the analog transmit filters.
      1.2.2. The differential output of the DAC is amplified by an analog differential amplifier EL2142C; this has the effect of carrying a terminated differential signal across a noisy digital groundplane to become a single-sided waveform on a quiet groundplane.
      1.2.3. The output of this amplifier is designed to not limit for the maximum DAC output excursion

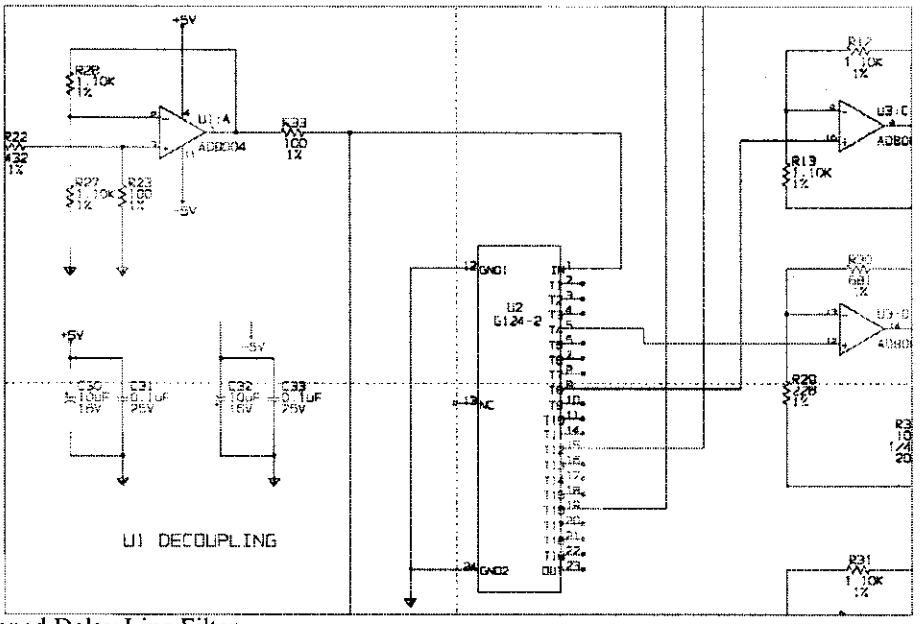


   1.3. Fig. 2 Test Connection for TX Filter Measurement.

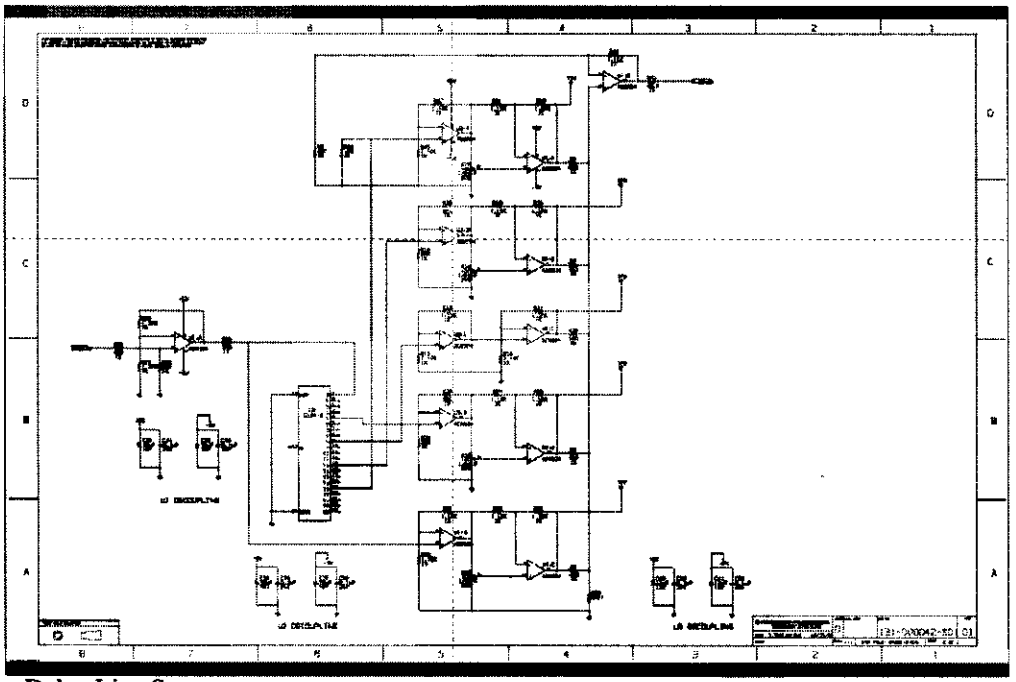


   1.4. Fig. 3 SigProc Filter Daughter Card Interface

1.4.1. The SigProc Filter Daughter Card TX section is a five-tap analog delay line equalizer with each tap amplitude adjustable within a specified range using a potentiometer. Taps are spaced at intervals of about one symbol time (40.6ns).



1.5. Fig. 4 Tapped Delay Line Filter



1.6. Fig. 5 Delay Line Summer

1.6.1. Unfiltered four-level waveforms spaced at about 1 symbol interval are scaled, possibly inverted and added in the tapped delay line filter

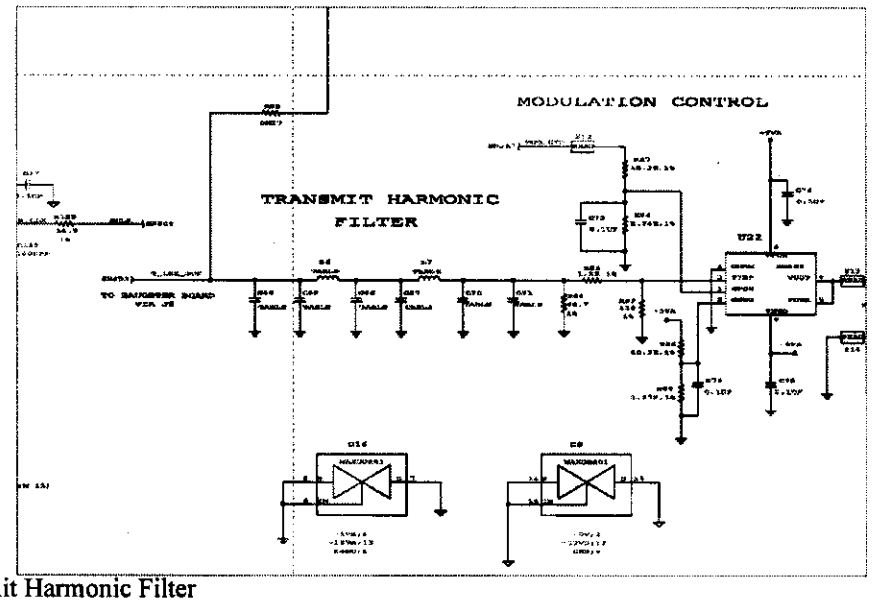
1.6.2. The center tap is fixed: all other taps are adjustable

1.6.3. The center tap has a fixed gain of 1

1.6.4. The two taps immediately adjacent to the center tap have a maximum gain of ± .4129

1.6.5. The two end taps have a maximum gain of ± .1000

1.6.6. This equalizer is used to cancel a major part of the linear part of the intersymbol interference that the subsequent radio creates.



1.7. **Fig. 6** Transmit Harmonic Filter

1.7.1. The equalized output is filtered using a Chebyshev 5th-order filter with 66 ohm source and load impedance. The filter output is matched using a pi-pad into the 100-ohm input impedance of the voltage-controlled amplifier.

1.7.2. The filter ratio of CIN to C1 is 127/220 or .5772 (.1dB ripple Chebyshev filter is .5807 ratio)

1.7.3. Inductors are wound toroids (9 turns of 30AWG enameled wire wound in a single layer on MICROMETALS T25-2 ferrite core, .446uH 5% adjusted and set by manufacturer using Q-Dope adhesive, marked with yellow dot on red wire) with design Q exceeding 140 for frequencies between 4.0MHz and 15 MHz.

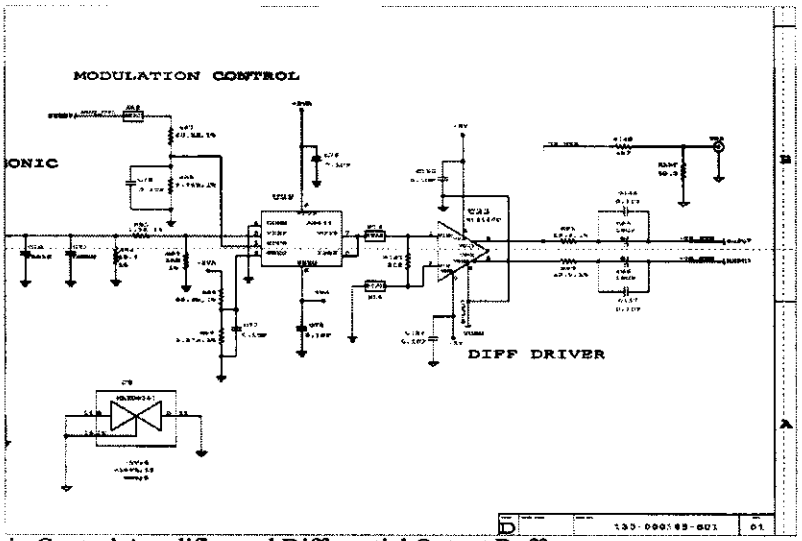
1.7.4. The prototype filter inductance is .28665 uH

1.7.5. The prototype filter capacitance is 98.1661pF

1.7.6. The prototype filter resistance is 54 ohms

1.7.7. The prototype filter frequency is 30MHz

1.7.8. The actual filter load is 47 ohms. The actual filter source is 50 ohms.



1.8. **Fig. 7** Transmit Gain Control Amplifier and Differential Output Buffer

1.8.1. The filter output is into an adjustable-gain amplifier with 100 ohms input impedance through a matching pad. This amplifier is used during system adjustment test to set the FM modulation index. The adjustment range is ± 6dB adjustable in .05dB increments.

1.8.2. The eye waveform is examined at TP2 during module test to verify the eye pattern closely matches a pictured eye pattern in terms of eye shape and closure and amplitude. The transmit RF spectrum is verified against a mask during Factory Acceptance Testing, as is the system BER performance versus RF level over temperature.

1.8.3. The Gain Control Amplifier output drives a differential amplifier (which bridges from the relatively-quiet PCA to the noisy backplane/receiver).

2. Measured Transmitter Filter

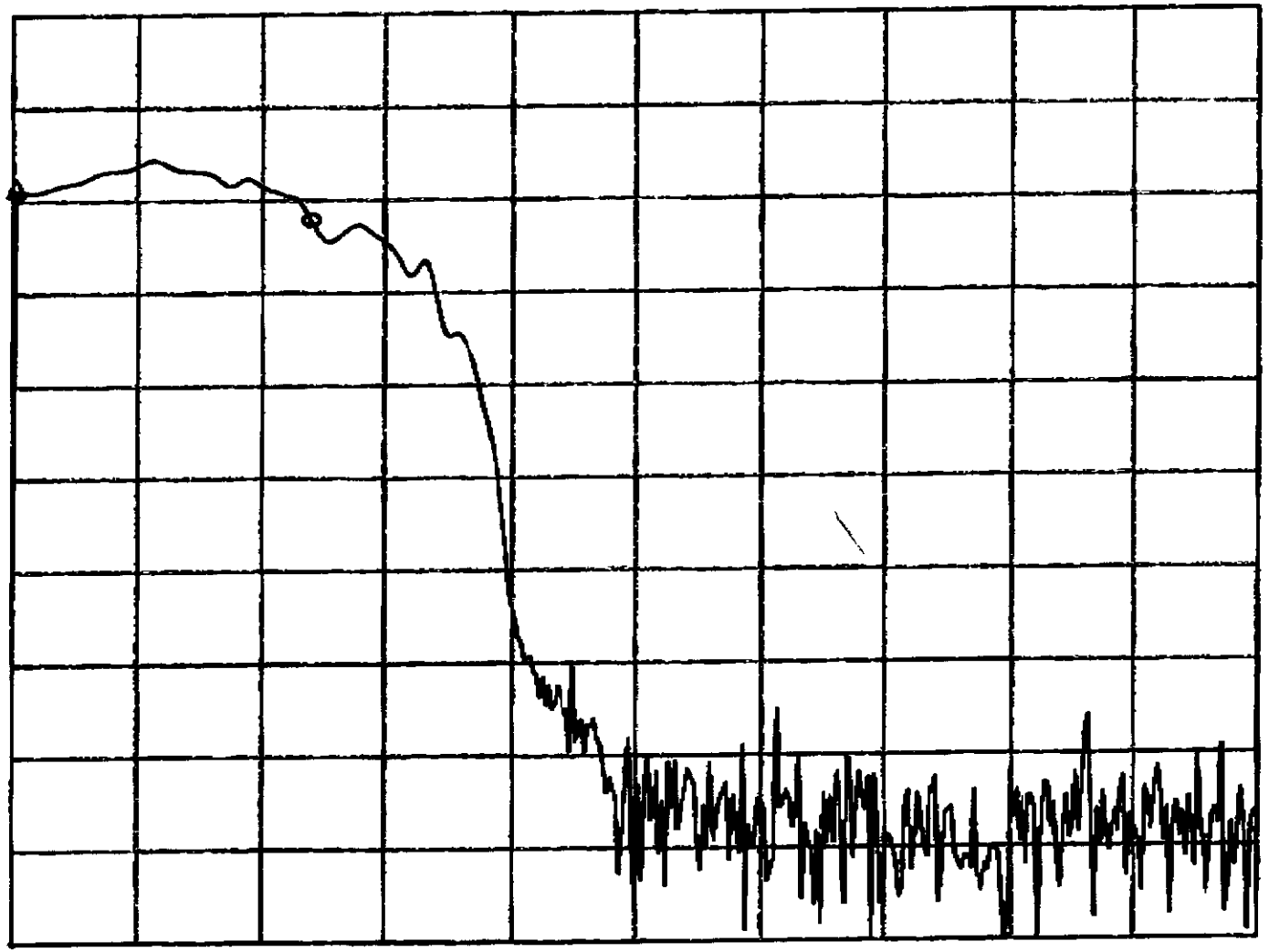
2.1. An HP3577B Network Analyzer (5Hz – 200MHz) is connected to the UUT, which has been mounted in a standard DMC Link Simulator Test Fixture.

2.2. R79 100 1% is removed. The resistor is replaced by the B (output) port of the Network Analyzer and a 50 ohm 1% resistor (return loss is not measured).

2.3. The PWB TX-EYE output is measured at the Link Simulator TX EYE output, which is connected directly to the A (input) Port of the Network Analyzer. This output is one-half of the normal differential SigProc output

2.4. The gain and group delay of the connection are scanned and plotted.

REF LEVEL /DIV OFFSET 23 750 000.000Hz
-10.000dBm 10.000dB MAG (A) -3.158dB



START 0.000Hz STOP 100 000 000.000Hz
AMPTD -10.0dBm

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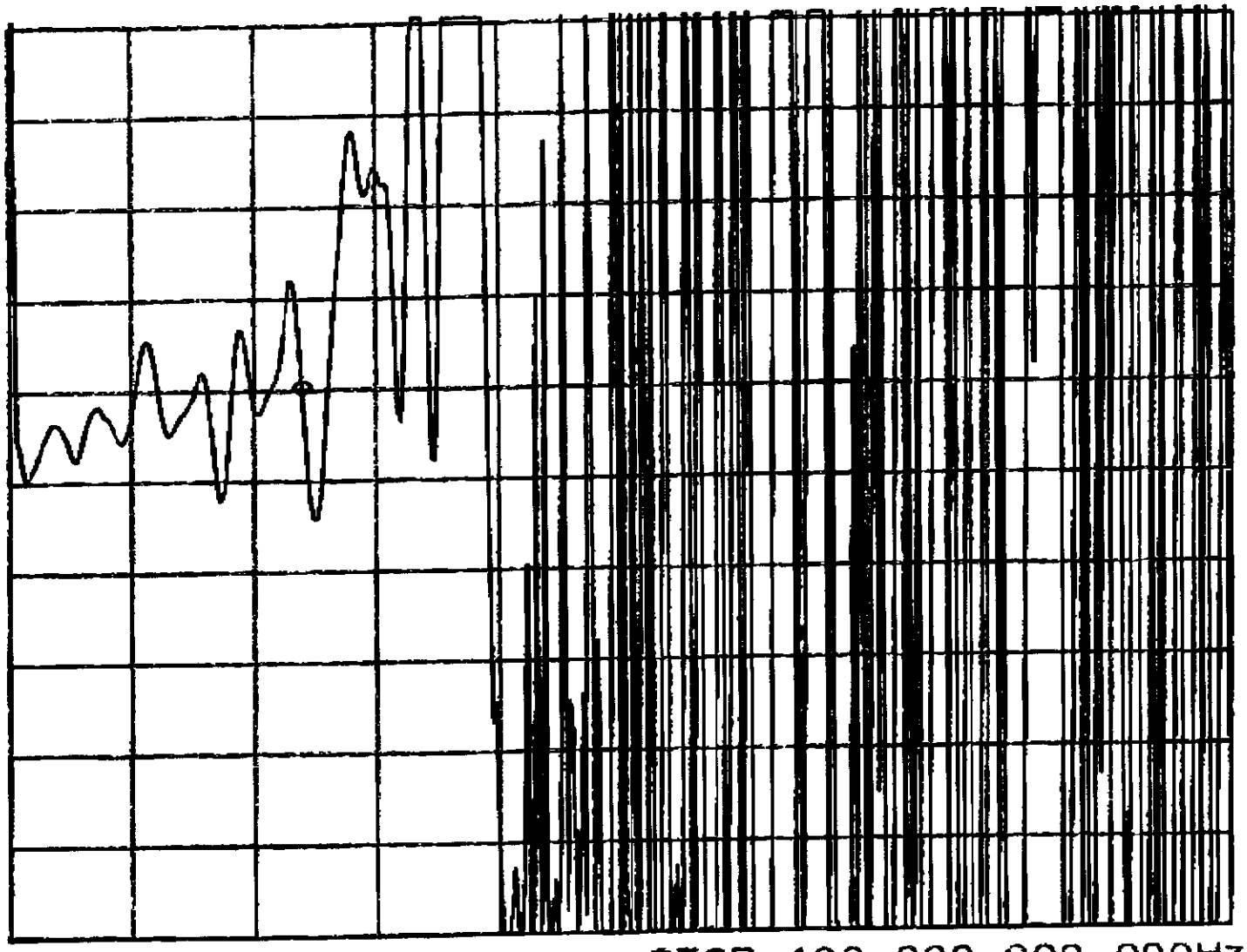
PLOTS: R BINNING
Single-Sided DS-3
Transmit FILTER
and EQUALIZER
AMPLITUDE VERSUS FREQ.



MAY 26, 1999
PETER J. CASTAGNA
PLOTS: R BIANNINI

Single-Sided DS-3
Transmit Filter and
Equalizer

GROUP DELAY VERSUS
FREQUENCY

CFR 47 part 2.1055 / 101.107 (IO) Frequency setting and stabilization:

Frequency Stability is a function of the Reference clock as shown in the specification sheet by Champion part number K 1 600. The requirement for the LMDS application (CFR 47 part 101.107) is +/- .00 1 %. This radio will provide stability of better than +/- .0005 %. The following drawing shows the arrangement of the various frequency determining elements for the XP4 radio. Additionally, the process which the computer controls the setting for the required frequency is also illustrated in this section.

Transmitter Frequency Control Circuit

Transmitter Frequency Control Circuit