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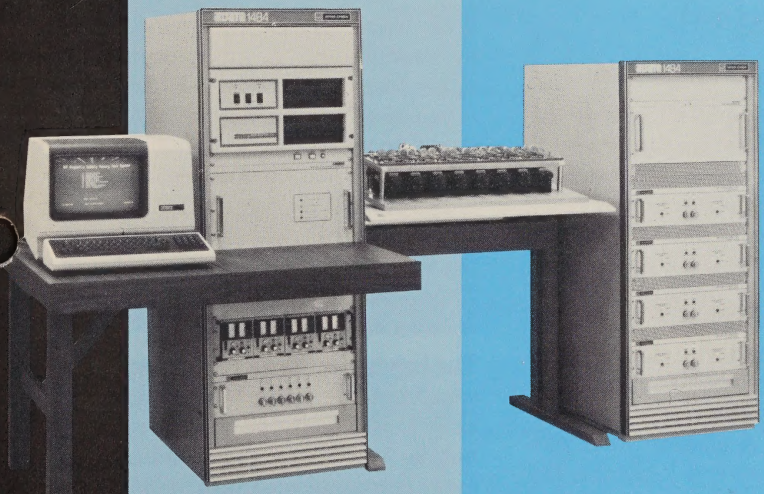
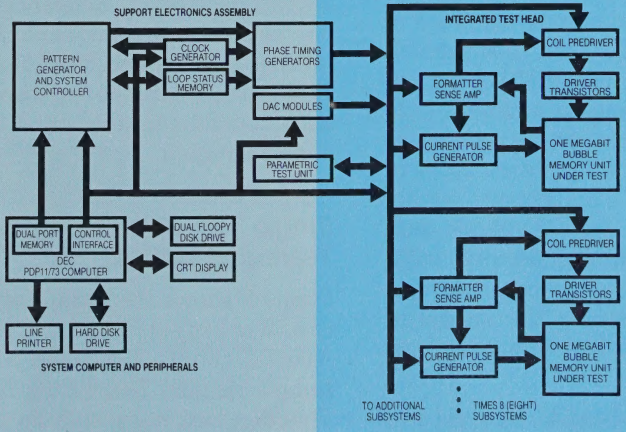
Parallel Testing of Magnetic Bubble Memories





WATKINS-JOHNSON COMPANY
Tech-notes

Higher density memory devices and accelerating technology combined with the special challenges of an analog interface and complex architecture present unique challenges to manufacturers of automatic test equipment (ATE) for magnetic bubble memories (MBMs). Testers must keep pace with technology, reduce test costs by reducing test times and provide a testing environment most appropriate for the particular MBM user application. Parallel testing, incorporation of MBM support ICs at test and an augmented test approach provide reduced costs, increased throughput and higher yields for MBM manufacturers.

Magnetic Bubble Memories

The first step in understanding the problems of MBM test is a fundamental knowledge of magnetic bubble memory technology. A magnetic bubble memory is a solid-state device that stores information in the form of cylindrical magnetic domains in a thin-film of magnetic material. These domains are mobile inside of the device along regular permalloy (nickel-iron alloy) patterns which define the device architecture. The presence of a domain at a particular site represents a logic one; the absence of a domain, a logic zero. The domains are moved about the device by means of a rotating magnetic field in the plane of the thin-film garnet. The interface to the MBM component is analog and, being a magnetic technology, all stimulus to the component is accomplished with current sinks or current sources. The primary advantages of MBMs are nonvolatile data storage, high storage density, solid-state operation and low power dissipation. Figure 1 shows the simplified block replicate architecture of the Intel 7110 MBM.

Data in the MBM resides in a series of circular shift registers called *minor loops*. Unlike a RAM, where a particular memory cell is addressed and its data accessed, data (magnetic domains) in the MBM must be moved or "replicated" from the device minor loops to an output track, where it is serially detected. Conversely, for write operations, data is serially written into an input track, where it is transferred or "swapped" in parallel to the minor loops. The data remains circulating in the minor loops until it is to be accessed. When any one bit is moved one site, all bits move one site, thereby requiring more housekeeping than a conventional array-type memory.

A key feature of MBMs is their capacity for redundancy. A given number of minor loops are allowed to be defective. A bad-loop map is generated at test and stored in a dedicated loop called the boot loop. When the MBM component is applied in a memory subsystem, the bad-loop map is read and used to mask out the defective portions of the device. This redundancy technique improves device-yields significantly.

The key implications for testing MBM components — analog interface, extensive housekeeping/timing requirements and internal redundancy — make automatic testing of MBMs quite different than automatic testing of conventional memories. References 1 and 2 provide a more detailed explanation of MBMs. With an understanding of the MBM component, one can then come to understand the existing single testhead implementation.

Single Test-Head Component Testing of MBMs

Figure 2 shows the block diagram for the Watkins-Johnson Company ADATE Single Test-Head Magnetic Bubble Memory Test System (MBMT). This diagram represents the primary approach to MBM testing. Testing is

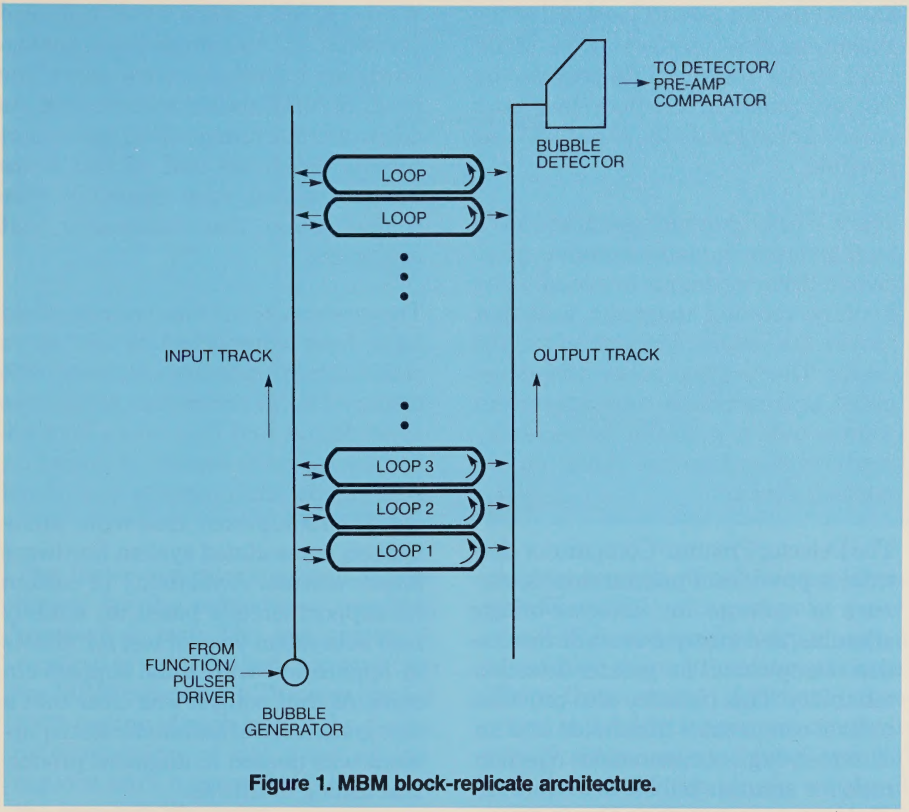


Figure 1. MBM block-replicate architecture.

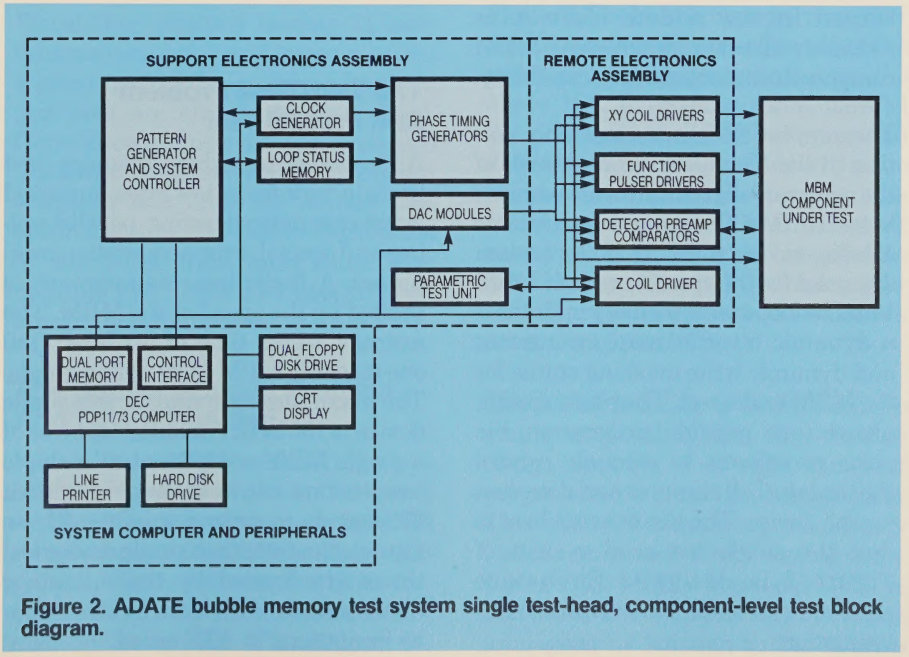


Figure 2. ADATE bubble memory test system single test-head, component-level test block diagram.

done at the component level. All of the custom analog interface to the MBM Unit Under Test (UUT) is provided by the test system in a remote electronics assembly as close to the MBM UUT as possible.

The XY coil drive subsystem utilizes a voltage-programmable commutating-switch drive technique to generate the in-plane rotating magnetic field that moves the bubble domains about the device. The function pulser drivers are gated, programmable constant-current sources used to generate the necessary read/write and control pulses for the memory device.

The Detector Preamp/Comparator electronics provides a programmable current or voltage for detector-bridge stimulus, and incorporates a dc restoration clamp circuit for greater detection reliability. This circuitry also provides bi-level comparator thresholds and an extremely high common-mode rejection ratio for accurate bubble detection. All of the analog interface circuitry contained in the remote electronics assembly allows comprehensive MBM component characterization capability.

The support electronics assembly portion of the test system contains all of the necessary digital hardware required to test MBMs. The pattern generator is a dedicated test microcontroller custom designed for the special needs of MBM test. The loop-status memory maintains a dynamic bit-error map, error count and dynamic write masking status for the MBM under test. The phase-timing generators provide programmable pulse waveforms to precisely control the timing of all stimulus and detection for the device. The key concept here is that the single test-head system of Figure 2 is designed for device characterization and engineering evaluation.

While MBMs were evolving and "growing up," this single-head, analog-hardware intensive system served the needs of MBM manufacturers well. As device architectures evolved, as support circuits developed and as test times became critical, new demands were placed upon the automatic test equipment.

The production test time problem could have been approached in two ways with existing hardware: eliminate 100% testing of MBM parameters, or increase expenditures and floor space for additional test-system capacity. Meanwhile, new device architectures (e.g., Intel IM7114 multiplexed read-write architecture) necessitated system hardware improvements. Availability of custom IC support circuits posed an entirely new subsystem level of test for MBMs in application with these support circuits. At that point it was clear that a new generation of automatic test equipment was needed to augment production testing of MBMs.

The Test-Time Problem And Parallel Test

Approaches to reduce memory test times include faster test rates, improved worst-case pattern testing, parallel testing and special error acceleration techniques. A faster test-rate approach is limited by the speed of the MBM. The average access time of an Intel 7110 one-megabit MBM is 41 milliseconds. The maximum data rate for this single device is 100 kHz. An automatic test of a single MBM component at a single temperature can take anywhere from 30 seconds to several minutes. These figures illustrate that single-device test times are limited by the operating requirements of the device rather than by limitations in ATE speed.

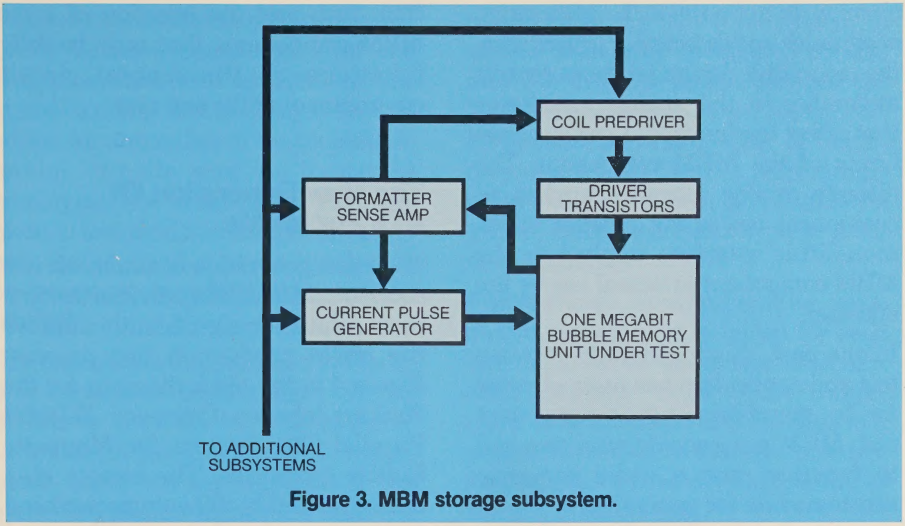


Figure 3. MBM storage subsystem.

The faster test-rate approach is also limited by the redundancy mapping required at test. The test system is required to write the bad-loop map into the MBM component. This requires full 100% testing of each loop in the device, determination of the most advantageous error map, and the writing of the map into the device.

Worst-case pattern testing is continuously evolving and improving, but a great deal of the gains available in this area are already being realized. Generation of a new test pattern is also a software task undertaken by the test engineer, and does not require new generations of hardware. Reductions in test times, then, must come from multiple test heads and special error acceleration techniques.

The Support-Circuit Problem And Guard Banding

Virtually no MBM end-user employs MBM technology without the 4 or 5 support ICs used to integrate the MBM component into an MBM memory subsystem. Figure 3 shows the block diagram for a single-component MBM memory subsystem. The support IC chip set consists of a formatter/sense amplifier (FSA), a current pulse generator (CPG), and a coil predriver with a monolithic driver transistor package. These three support functions correspond to the detector preamp comparators, function pulser drivers and XY coil drivers of the single test-head component test system diagrammed in Figure 2. The bubble memory controller (BMC) support IC generates all of the necessary timing and control for the above ICs. It provides serial/parallel data conversion, FIFO buffering and data-rate coordination. The BMC is the sophisticated interface between the MBM memory subsystem and the next hardware level for which it provides data storage. The BMC is replaced at test by the support electronics assembly of the ATE.

The analog interface to the MBM in the single test-head system is a discrete design capable of a wide range of programmable stimulus and detection. This discrete design also provides very fast, accurate and "clean" analog waveforms to the MBM component UUT. In contrast, the support ICs (though analogous in function to the discrete

circuits) do not provide the wide range of stimulus and detection. Furthermore, the monolithic design produces certain anomalies in the analog waveforms that effect the functional performance limits of the MBM component. The discrete analog interface applied at component test is far superior to the monolithic interface applied to the MBM component in actual use by the end-user.

In the past, this incongruity between test and application has been adjusted for by guard-banding at component test. MBM components were required to function over a wider range to accommodate for anomalies in the IC support circuits. Experience dictates which parameters are most crucial to guard band. The guard-banding technique is nothing new to memory testing. The trade-off is a reduction in yield from test, and the rejection of some MBM components that may be fully functional in the support circuit environment of the end-user.

The New Generation Of ATE For MBMs

The latest generation of automatic test equipment for MBMs provides the optimum solution to significantly improve the MBM production test process. Figure 4 is the block diagram for the Watkins-Johnson Company WJ-1484 Parallel Test System for Magnetic Bubble Memories. The remote electronics assembly of the single test-head system is replaced by an integrated parallel test head (PTH). The PTH utilizes the monolithic support ICs to provide the full analog interface to the MBM under test. This production-

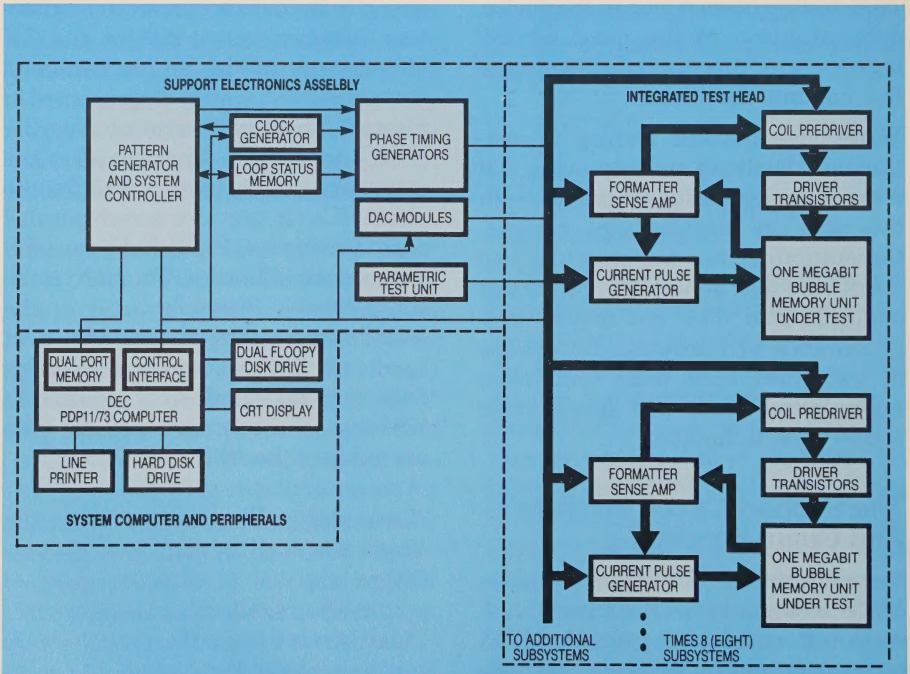


Figure 4. ADATE parallel bubble memory test system block diagram (eight test-head, subsystem).

oriented approach eliminates the incongruity between component-level test and subsystem-level application. The guard-banding test technique used to adjust for anomalies in the monolithic analog circuits need no longer be employed. The result is an improvement in test yield and components that are tested in the same electronic environment in which they will be applied.

The test system diagrammed in Figure 4 is capable of testing eight 1M bit MBMs or four 4M bit MBMs simultaneously in parallel. While all components under test are subjected to the same test-pattern algorithm, separate data masking, loop status and error logging are provided for each individual MBM under test. Special functions have also been added to provide diagnostic capability beyond what the normal support IC application will allow.

Three independently programmable voltage rails provide power to the support ICs. This allows V_{CC} (ICs power) performance limits to be assessed for the MBM in the bubble subsystem. A special "level-shift" circuit incorporated into the detector bridge between the MBM component and the FSA support IC allows programmability of bubble detection levels. Current pulse amplitudes to the MBM are also variable via a DAC-controlled current pulse generator reference.

Furthermore, comprehensive parametric capability is provided for each individual MBM under test. This capability permits "dead" MBM components to be identified and replaced in a matter of seconds so that dynamic test sockets can be used more efficiently to test shippable MBMs.

Augmentation Of The Production Test Process

Figure 5 shows a simplified work-flow diagram that can be implemented for MBM production test. Note that both single test-head and parallel test-head systems are employed.

The single test-head system performs component level test of MBMs. Only

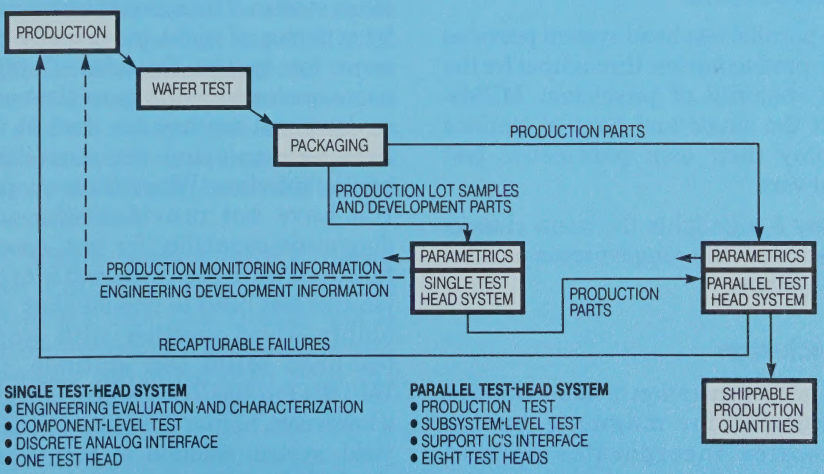


Figure 5. Work-flow diagram MBM production test.

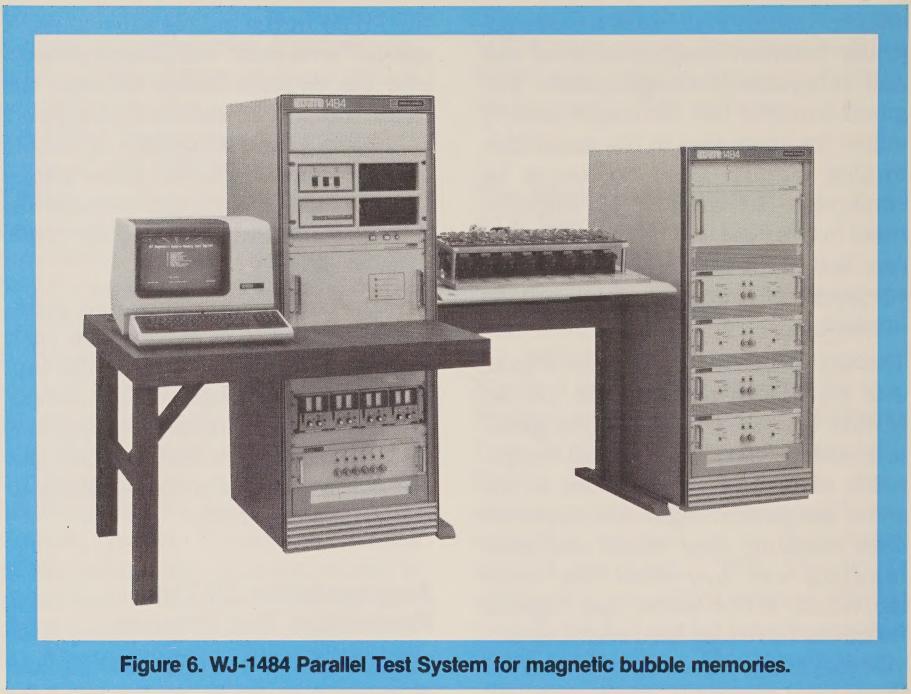


Figure 6. WJ-1484 Parallel Test System for magnetic bubble memories.

sample lots of production parts and new parts requiring characterization and development are passed through this level of test. This component level of test provides valuable engineering information for development parts and valuable quality/yield information for production parts.

The parallel test-head system provides high production test throughput for the vast majority of production MBMs. Both the single and parallel stations employ their own parametric test hardware.

Figure 5 highlights the main characteristics of the single-versus-parallel test systems.

Conclusion

The latest generation of automatic test equipment for magnetic bubble memories incorporates several improvements in hardware and test concept into a single-system solution. The Watkins-Johnson Company WJ-1484 Parallel Test System for Magnetic Bubble Memories is pictured in Figure 6.

Greater expenditures and increased floor space are not required for the latest system. Throughput is increased by a factor of eight in virtually the same test-system footprint. Components are tested in the same electronic environment as they are used in the field by employing the monolithic analog interface. Where these support ICs have not provided adequate diagnostic capability for test, special functions have been designed into the parallel test head to provide that capability. Used together with single test-head MBM test stations, the WJ-1484 Parallel Test System provides a lower cost, higher throughput, higher yield, system solution to comprehensive MBM testing.

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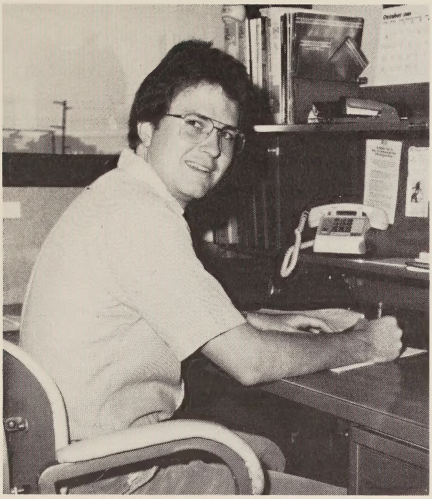

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Mr. Adams is a Member of the Technical Staff in the Test Department and is currently assigned as Acting Head, ATE Sub-Systems Section. He is responsible for the design and development of custom subsystems for ATE products. He has held design, development, field maintenance and overall product responsibility for the ADATE WJ-14XX line of automatic test equipment for magnetic bubble memories. His section is also responsible for a new product line of ADATE ATE for telecommunications transmission systems. Reduction to practice of digital subsystems as well as magnetic bubble memory and rf system integration have been additional responsibilities.

Mr. Adams holds a B.S.E.E. degree from California Polytechnic State University, San Luis Obispo, and is currently pursuing a Masters Degree in Business Administration from the University of Santa Clara.

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