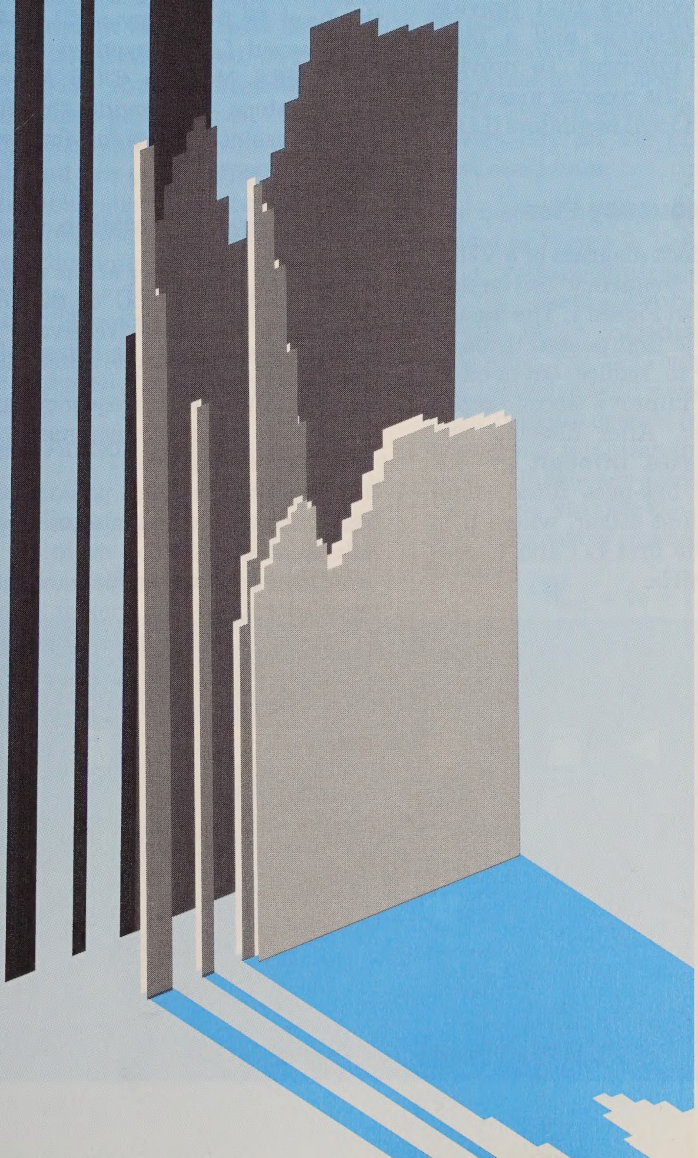
VOL. 18 NO.2 MARCH / APRIL 1991

Design Considerations For Fast Switching PLL Synthesizers



WATKINS-JOHNSON COMPANY

Tech-notes

The requirements placed on surveillance receivers have become more stringent in the past decade. The need for smaller and smaller receivers has been growing because of the task of monitoring more signals from sites with limited space. In addition, due to the dense signal environment, today's receivers must have better selectivity, sensitivity, and dynamic range than those in the past. The recent introduction of frequency-agile communications systems has created the need for surveillance receivers that provide high-speed acquisition and a high probability of intercept. To provide this capability, the receiver must contain high-speed local oscillators (LOs).

Receiver Frequency Plan

A simplified block diagram of a VHF/UHF receiver frequency conversion plan is shown in Figure 1. The incoming spectrum is first passed through a preselector to reduce out-of-band signals and improve second-order intercept point. After filtering, the spectrum passes through an RF amplifier and low-pass filter before entering the first mixer, where it is mixed with the first LO and upconverted to 692 MHz.

The first LO must tune from 694 MHz to 1204 MHz to translate the 2-to-512 MHz spectrum up to the first IF frequency. The first LO must also take steps small enough to keep the input signals and the information they may carry within the first IF bandwidth. A step size of 2 MHz was chosen for the conversion plan shown.

The upconverted IF signal at 692 MHz is then filtered and amplified before entering the second mixer, where it is mixed with the second LO to produce the final IF frequency of 21.4 MHz. The second LO is required to tune from 668.6 MHz to 670.6 MHz in 100-Hz steps to provide the final tuning resolution over full frequency range of operation.

First LO Implementation

Let us first look closer at the requirements for the first LO of this fast-acquisition miniature receiver. The synthesizer's requirements include:

1. 694 to 1204 MHz frequency range
2. 2-MHz frequency increments
3. Fast settling time
4. Low phase noise
5. Low power consumption
6. Small size
7. Good spurious performance

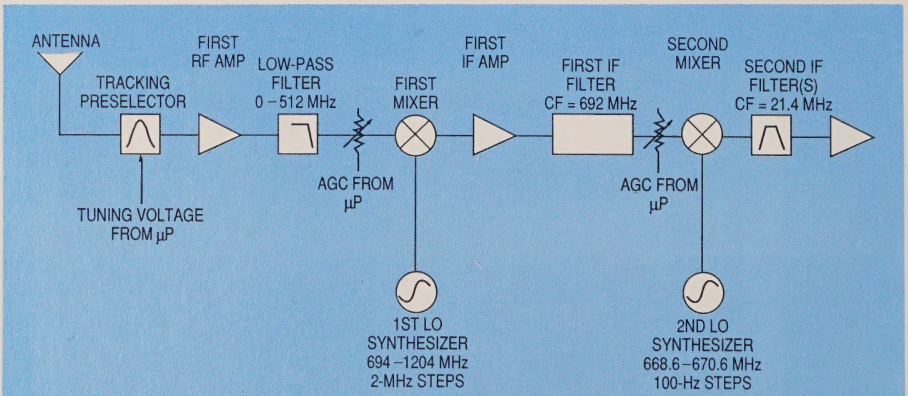


Figure 1. VHF/UHF receiver frequency conversion plan.

The first step in the synthesizer design is to determine which of the three basic synthesis techniques best provides the performance needed: direct digital, direct analog or phase-locked loop.

Direct Digital Synthesis

No other area in frequency synthesis has received more attention in recent years than direct digital synthesis (DDS), nor has any area made as much progress. Direct digital synthesizers produce signals with fine frequency resolution, fast switching speed, good spurious response and phase-noise performance. In VLSI form, these synthesizers are relatively small and low power. The limitation on the technique is that the maximum output frequency obtainable with low power consumption and reasonable spurious performance is about 10 MHz. Therefore, it is not possible to implement the first LO directly with DDS and meet the LO requirements.

Direct Analog Synthesis

Direct analog synthesis refers to the generation of new frequencies from one or more reference frequencies using a combination of multipliers, dividers, mixers, and bandpass filters. Direct analog synthesis can provide fine resolution, fast switching and low-noise synthesizers. However, the hardware requirements make this approach too large and too power-hungry to be of use in a miniature receiver. In addition, because the frequency range of interest is nearly an octave, the spurious performance of this approach would not meet the established specifications.

Indirect Synthesis: The Phase-Locked Loop

No other synthesis approach has been so excessively discussed in print as the phase-locked loop (PLL). Nearly all of today's small, synthesized receivers rely on the PLL to produce local oscillators.

The basic form of the digital PLL is shown in Figure 2. The loop consists of a voltage-controlled oscillator (VCO), variable-ratio frequency divider, phase comparator, and low-pass filter. The VCO output is divided and compared with a stable reference. Error voltages derived from the phase comparator maintain the VCO on frequency. Frequency selection is accomplished by varying the division ratio of the frequency divider. For locking to occur,

$$f_{out} = N \times f_{ref}$$

Equation 1

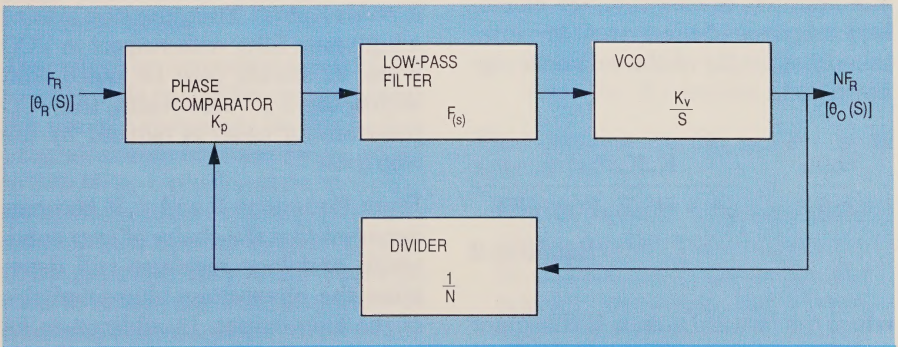


Figure 2. PLL block diagram.

Equation 1 indicates that the smallest frequency increment generated by the loop is equal to the phase comparator frequency (f_{ref}). Also, note that this frequency determines the rate at which frequency corrections are made to the VCO.

The switching speed of the phase-locked loop is a function of the loop bandwidth and closed-loop frequency response. Since the bandwidth is always smaller than f_{ref} to provide a clean correction voltage to the VCO, faster switching speeds require higher reference frequencies.

A properly designed phase-locked loop can provide a low powered, small-sized frequency synthesizer with moderately fast switching speed. This will be the synthesis method chosen for the fast-switching first LO.

PLL Basics

It is customary to use feedback control theory in the analysis of phase-locked loops. Therefore, a quick review of the concepts of feedback control theory as applied to PLLs follows. From Figure 2, in control theory terms, the transfer function from any point in the system to the output is simply the forward gain from that point to the output divided by 1 + (open-loop gain). For example, in this case, the closed-loop response of the system to variations in s(s = jω) of the reference signal θr(s) is:

$$\frac{\theta o(s)}{\theta r(s)} = \frac{K_v K_p F(s)/s}{1 + (K_v K_p F(s)/sN)}$$

Equation 2

where the forward gain is KvKpF(s)/s and the open-loop gain is KvKpF(s)/sN. Re-writing Equation 2 to the form

$$\frac{\theta o(s)}{\theta r(s)} = \frac{N}{1 + s(N/K_v K_p F(s))}$$

Equation 3

yields the transfer function of a low-pass filter whose time constant is N/KvKpF(s). This shows that the loop acts as a low-pass filter with respect to variations in s of the reference signal. It should be noted that the variations in phase at the output are N times greater than those at the input for frequencies within the bandwidth of the loop.

Equation 3 illustrates one of the fundamental characteristics of a PLL. That is, that the phase noise at the output of a PLL, within the loop bandwidth, is equal to the reference noise multiplied by N (assuming the loop gain suppresses VCO noise).

Loop Response to VCO Noise

Referring to Figure 2, the transfer function from the VCO to the output can be written as:

$$\frac{\theta o(s)}{\theta v(s)} = \frac{1}{1 + (K_v K_p F(s)/sN)}$$

Equation 4

Equation 4 is the transfer function of a high-pass filter whose time constant is N/KvKpF(s). Thus, the loop acts as a high-pass filter with respect to VCO noise. It should also be noted that within the 3-dB bandwidth, the VCO free-running noise is reduced by the loop gain.

From Equations 3 and 4, it becomes apparent that the choice of loop bandwidth and loop response will determine the phase-noise characteristics of the loop output. In addition to its importance in determining the loop's phase-noise performance, the loop

bandwidth and response will determine the switching speed of the loop. It has been suggested that with presteering, the settling time of the loop can be approximated by:

$$\text{settling time} = \frac{4 \text{ to } 6}{\text{(closed-loop bandwidth)}}$$

Equation 5

This equation is used only as a rule-of-thumb and does not take into consideration loop-damping factors or loop phase margin. It does, however, suggest that to obtain faster switching speed, you need simply to widen the loop bandwidth. However, the loop bandwidth cannot increase without limit because of sampling-delay phase shifts and the need to filter the reference frequency ripple from the phase detector to prevent sidebands on the LO.

First LO Design Compromises

Let us now attempt to design a PLL to implement the first LO required for the miniature acquisition receiver. From Equation 1, the maximum reference frequency allowed to maintain the desired frequency resolution is 2 MHz. From our discussions on phase noise and tuning speed, it is apparent that the maximum reference frequency will also produce the best noise performance and the fastest switching speed.

To produce an output frequency of 694 to 1204 MHz in 2-MHz steps requires the use of a frequency divider that is programmable over the range of 347 to 602 MHz. Unfortunately, there are no dividers programmable over this range which operate at 1200 MHz. A fixed prescaler (say ÷ 10) could be used to reduce the VCO frequency to that which is acceptable to programmable counters. However, the loop reference frequency would also have to be reduced by the prescaler value to maintain 2-MHz increments at the output. Reducing the reference frequency would increase the division ratio in the loop and require a narrower loop bandwidth resulting in greater reference noise and slower speed.

The alternatives to fixed division are mixing and "dual modulus division." The use of mixers within a loop requires a considerable amount of hardware, and is prone to spurious-signal generation if careful attention is not paid to layout. Although widely used, mixing is certainly more complicated than dual modulus division in terms of realization in a small amount of space with low power consumption.

The principle of dual modulus division centers on a high-frequency divider working in conjunction with lower speed programmable counters. Figure 3 is a block diagram of a dual modulus system. It is composed of the following major blocks:

- A dual modulus prescaler which will divide by one of two numbers, P or P+1 (e.g., 10/11, 128/129, etc.).
- An A counter which is programmable and controls the modulus of the prescaler.
- A programmable N counter which is clocked in parallel with the A counter whose output resets the A counter and itself.

The operation of the system is as follows:

The A counter is programmed with a smaller number than the N counter and, assuming the counters are empty, the system starts with the dual modulus prescaler dividing by P+1. This continues until the A counter reaches

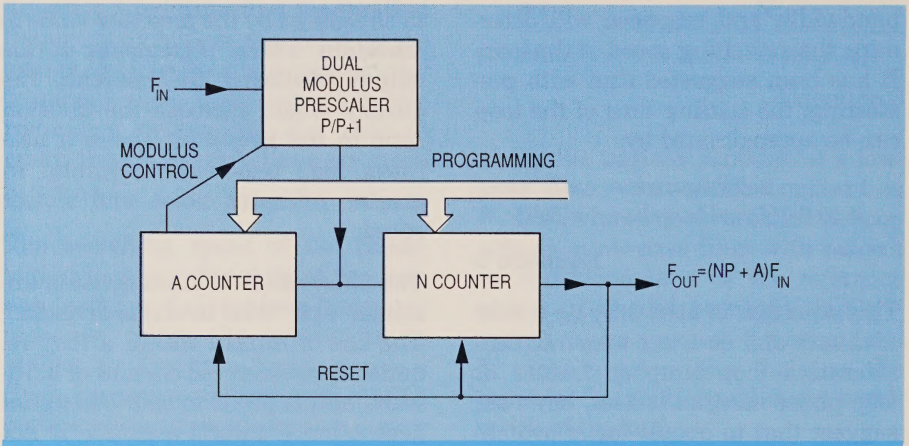


Figure 3. Dual-modulus prescaling.

its programmed value at which time the dual modulus prescaler divides by P until the N counter reaches its programmed value. Since the A and N counters are clocked in parallel, the system will have divided by P+1 for the A counts and by P for the N−A remaining counts. Thus, the total division ratio N_{tot} is given by:

$$N_{tot} = A \times (P+1) + (N-A)P$$
$$= N \times P + A$$

Equation 6

In the example, if a 1204 MHz ÷ 10/11 prescaler were available and the loop required a 2-MHz reference frequency, the required division ratio would be 602. By setting A = 2 and N = 60, the system would divide by 11 for the first two counts and by 10 for the remaining 58 counts. Yielding,

$$N_{tot} = (2 \times 11) + (58 \times 10) = 602.$$

Obviously, for the system to work, A must be less than or equal to N and, therefore, to make every channel available, the minimum division ratio with the loop is:

$$N_{tot}(min) = P(P-1)$$

Equation 7

Loop-Delay Requirements

The operation of the dual modulus system appears simple; however, there is one very important consideration which *cannot* be overlooked. That consideration is loop delay.

Considering the previous example again, where N = 60, A = 2, and the ÷ 10/11 is operating at 1204 MHz. Suppose N and A are downcounters and A has just decremented to 1. After 11 more pulses into the dual modulus divider, the A counter will receive a pulse to decrement to zero and reset the ÷ 10/11 to divide by 10. Consider the counter the instant the 11th pulse appears at the 10/11 input. After some time, tp1 (determined by the ÷ 10/11 propagation delay), the ÷ 10/11 will produce a pulse which clocks the N and A counters; then, after some time, tp2 (determined by the A counter propagation delay), the A counter produces a pulse to set the dual modulus divider ratio to ÷ 10; and after a setup time, tp3, the dual modulus divider will divide by 10. But, if the total delay, tp1 + tp2 + tp3, is greater than ten cycles of the input frequency, the divider will not be set to ÷ 10 until after ten pulses have passed. Hence, the system will fail. Thus,

$$P/fin > \text{total loop delay}$$

Equation 8

An example of some available prescalers from leading manufacturers is shown in Table 1. The table includes important information on the devices including:

- Maximum operating frequency
- Propagation delay and setup time
- Minimum division ratio for continuous coverage
- Power consumption

From the table, it is apparent that the maximum operating frequency of the low-power dividers is 1300 MHz. However, from Equation 3, the maximum reference frequency would be limited to:

$$692\ \text{MHz}/P(P-1)$$
$$= 172\ \text{kHz (using } \div 64/65 \text{ prescaler)}$$

This reference frequency would be much too low to implement a high-speed loop. Since all other prescalers operate below 1100 MHz, a fixed prescaler will be required in the loop between the VCO and dual modulus prescaler. Adding a fixed divide-by-2 in the loop will reduce the maximum reference frequency to 1 MHz and increase the phase noise due to the reference by 6 dB.

Prescaler Listing

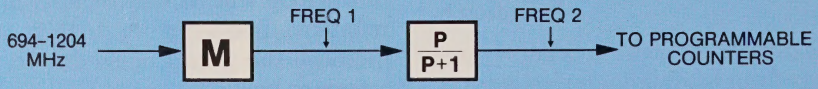
Table 2 lists the possible combinations of fixed and variable dividers and the loop design features of each combination. The choice of the optimum combination was based on achieving the highest reference frequency possible without exceeding the propagation delays or maximum input frequencies of the N and A counters controlling the dividers.

From Table 2 it is apparent that the best choice of prescalers is fixed $\div$ 2, followed by the SP8782 $\div$ 16/17. The SP8782 is a new integrated circuit introduced last year with advanced resynchronizing techniques used to minimize loop-delay effects. Thus, the device adds only 4 nanoseconds to loop delay.

Referring once again to Table 2, it is shown that the N and A counters

MODULUS	INPUT FREQ. (MAX)	MIN. DIVISION RATIO	PROP. DELAY (MAX)	SET UP TIME (MIN)	5V POWER CONSUMPTION (MAX)
5/6	1.5 GHz	20	1.9	690 ps	1.1 W
10/11	1.5 GHz	90	3.0	690 ps	1.1 W
20/21	1.5 GHz	380	4.1	690 ps	1.1 W
40/41	1.5 GHz	1560	5.3	690 ps	1.1 W
64/65, 128/129	1.3 GHz	4032, 16256	Not Specified	25 ns	50 mW
64/65, 128/129	1.1 GHz	4032, 16256	8 ns.	16 ns	50 mW
16/17	1.0 GHz	240	3 ns.	1 ns	200 mW
8/9	500 MHz	56	6 ns.	2.5 ns	300 mW
10/11	500 MHz	90	6 ns.	2.5 ns	300 mW
40/41	520 MHz	1560	28 ns.	10 ns	60 mW
10/11	200 MHz	90	9 ns.	3 ns	100 mW
10/11	225 MHz	90	45 ns.	14 ns	35 mW

Table 1: Dual modulus prescaler availability.



M	FREQ. 1 (MAX)	P/P=1	FREQ. 2 (MAX)	ALLOWABLE LOOP DELAY[1]	REQUIRED "A" COUNTER DELAY[2]	MAXIMUM f_{ref} FOR 2 MHz STEP[3]
Not Used	1204 MHz	64/65	18.8 MHz	53 ns	Not Specified	172 kHz
2	602 MHz	64/65	9.4 MHz	106 ns	Not Specified	86 kHz
2	602 MHz	16/17	37.6 MHz	26.6 ns	22.6 ns	1 kHz
4	301 MHz	8/9	37.6 MHz	26.6 ns	19.6 ns	500 kHz
4	301 MHz	10/11	30.1 MHz	33.2 ns	26.2 ns	500 kHz
4	301 MHz	40/41	7.525 MHz	133 ns	95 ns	110 kHz
8	150.5 MHz	10/11	15 MHz	66.6 ns	54.6 ns	250 kHz
8	150.5 MHz	10/11	15 MHz	66.6 ns	7.6 ns	250 kHz
16	75 MHz	64/10	7.5 MHz	133 ns	74 ns	125 kHz

1. Where Allowable Loop Delay = P/FREQ. 1
2. Where Required A Counter Delay = Allowable Delay − (P/P + 1) delay − (P/P + 1) Set Up Time
3. Where $f_{ref}(max)$ = The smaller of 2 MHz ÷ M or 694 MHz ÷ M ÷ [P(P−1)]

Table 2: 1st LO prescaler options.

must operate at 37 MHz and have a maximum clock-to-output delay of:

26.6 nsec (allowed)
− 4 nsec (SP8782) = 22.6 nsec.

Commercially available LSI Counters cannot meet the speed requirements and, therefore, discrete counters using high-speed logic are required. This will increase the power consumption as only FAST TTL and ECL logic will fulfill the requirements. If low power consumption was the main concern, another combination of dividers could have been chosen which would allow low power C-MOS dividers to control the dual modulus prescalers. For instance, if a fixed ÷ 8 was followed by a ÷ 10/11 prescaler, a 250-kHz loop could be designed which would consume only 20 percent of the power of the selected loop. However, the speed would be limited to several milliseconds.

First LO Design

A block diagram of the first LO design is shown in Figure 4. The first LO is comprised of four VCOs (used to keep VCO sensitivity low), a fixed ÷ 2 prescaler, ÷ 16/17 dual modulus divider, programmable N and A counters, phase detector, and loop filter. The phase detector used within the loop is a discrete phase/frequency detector and charge pump which is shown in Figure 5. Using the loop filter shown in Figure 5 creates a second-order type-2 loop expressed by:

$$\frac{\theta o(s)}{\theta r(s)} = \frac{2sD\omega_n+1}{s^2 + 2sD\omega_n+1}$$

Equation 9

where $\theta o(s)$ and $\theta r(s)$ are output and input phase and ω_n and D are the closed loop natural frequency and damping factor given by

$$\omega n = \sqrt{\frac{K_v K_p}{NC}}$$

Equation 10

$$D = \frac{RC\omega_n}{2}$$

Equation 11

and

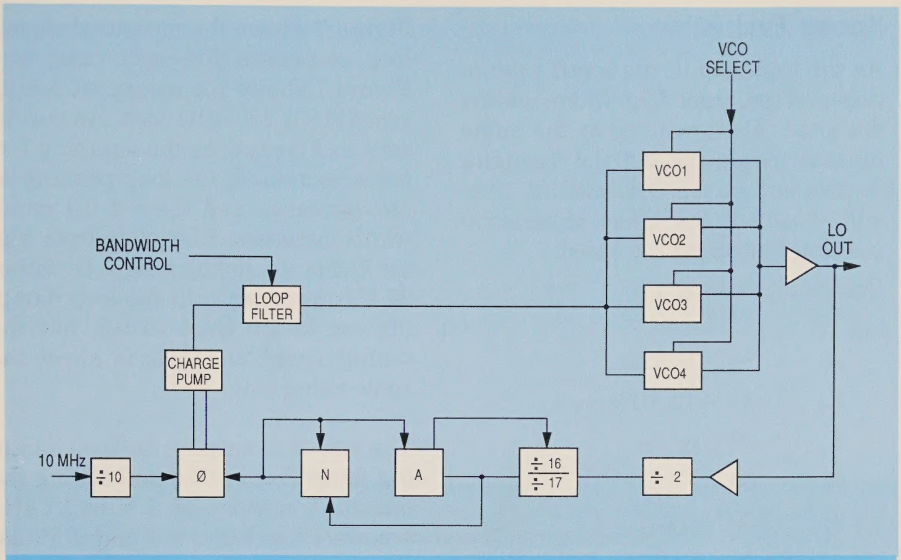


Figure 4. First LO block diagram.

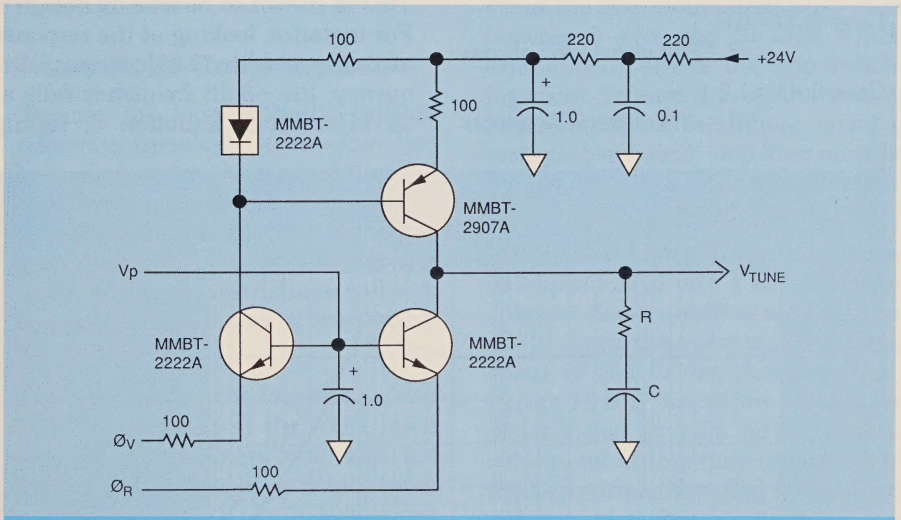


Figure 5. Phase-detector charge pump.

$$BW3dB = \frac{\omega_n}{2\pi}\left(2D^2 + 1 + \sqrt{(2D^2+1)^2 + 1}\right)^{1/2}$$

Equation 12

is the 3-dB bandwidth of the loop in Hz.

Speed Evaluation

As the first step in the speed evaluation process, three loop filters will be designed. Each will have the same natural frequency, but the damping factors will be 0.5, 0.8, and 1.0. This will illustrate the effect closed-loop peaking has on tuning speed.

Design Equations

Let

$\omega_n = 2\pi \times 10$ kHz

$K_v = 2\pi \times 12$ MHz/volt

$K_p = 18$ mA/2π

$N = 800$

fo = 800 MHz

$C = K_v K_p / N\omega_n^2 = 0.06\ \mu F\ (0.068\ \mu F)$

Case 1: D = 0.5

$R = 2D/\omega_n C = 234$ ohms (220 ohms)

Case 2: D = 0.8

R = 374 ohms (365 ohms)

Case 3: D = 1.0

R = 468 ohms (475 ohms)

Figure 6 shows the measured closed-loop responses for each case, and Figure 7 shows the measured tuning speed for a 125-MHz step. As can be seen in Figure 6, as the damping factor is increased, the loop peaking at ωn decreases and the −3 dB bandwidth increases. Also, note from Figure 7, that the tuning time to be within 20 kHz is faster with the loop damping set to 1.0 than to 0.5, but the tuning speed to 1 kHz is about the same either way.

The effects of keeping the loop damping factor fixed at 0.8 and setting the natural frequency at 4, 8 or 15 kHz are shown in Figures 8 and 9. Equation 11 predicts that when D = 0.8, the loop −3 dB frequency will be approximately twice the natural frequency. This is shown to be true in Figure 8. For instance, looking at the response of the loop with 15-kHz natural frequency, the −3 dB frequency falls at 34 kHz. From Equation 5, tuning

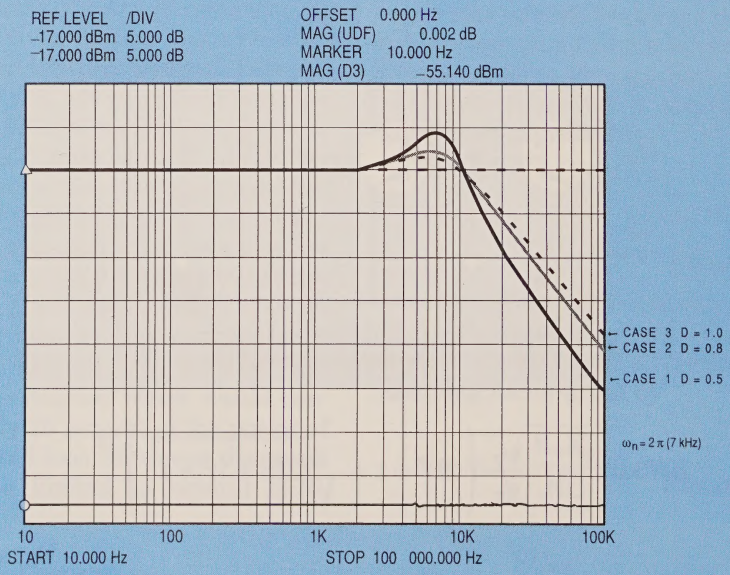


Figure 6. Closed-loop response versus damping factor.

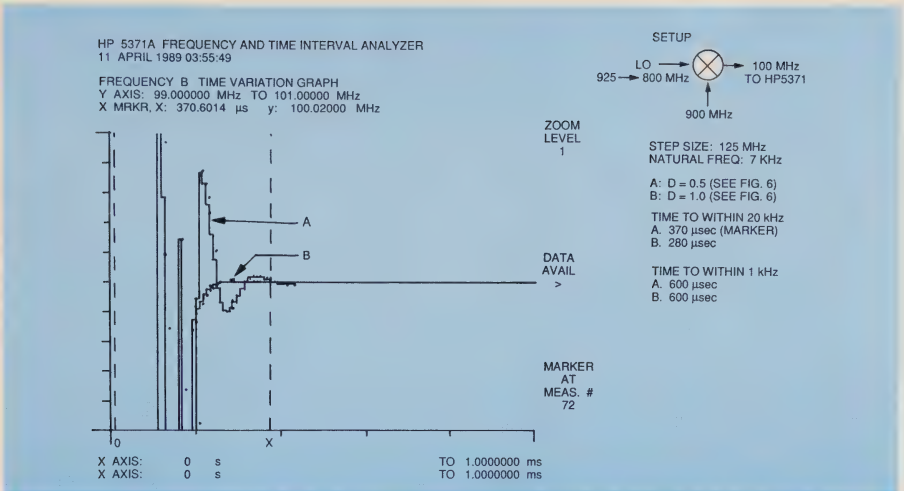


Figure 7. Step response versus damping factor.

speed is predicted to be approximately 100 to 200 microseconds, as shown in Figure 9.

Phase-Noise Considerations

Because the loop with the highest reference frequency achievable has been chosen, we are assured that the noise within the loop bandwidth due to the multiplied reference noise has been minimized. But how low is this noise, and what restrictions will this impose on the choice of loop bandwidth?

The noise within the loop bandwidth will be composed of the VCO noise reduced by the loop gain and the divider and reference oscillator noise multiplied by N_{tot}. At 10-kHz offset from the carrier, the noise floor of the divider/phase detector has been measured at −155 dBc/Hz. Therefore, the phase noise at a final output frequency of 1204 MHz will be:

$$20 \log (1204)\ \text{dB} - 155\ \text{dBc/Hz} = -93.4\ \text{dBc/Hz at 10-kHz offset.}$$

To meet the phase noise specification of −95 dBc/Hz at 20-kHz offset will require that the loop response provide 3 dB of attenuation at 20 kHz. This forces the loop natural frequency to be between 5 kHz and 10 kHz, which dramatically affects the loop switching speed. To meet the requirements of switching speed and phase noise, a multiple bandwidth loop filter must be designed which is wide during switching and narrowed after settling.

This type of filter is being designed to be implemented into a new Watkins-Johnson fast-acquisition receiver. Figure 10 shows the worst-case switching speed of the LO at this time, and Figure 11 is a plot of the closed-loop phase noise at 1200 MHz. Work is continuing at this time to implement the loop without the need for the fixed ÷ 2 prescaler. Present designs center on the use of high-speed programmable array logic (PAL) in conjunction with SP8782 (÷ 16/17). Eliminating the ÷ 2 will reduce phase noise 6 dB and allow for a wider loop bandwidth with a simpler design.

First LO Summary

Some of the compromises in implementing a fast switching PLL have

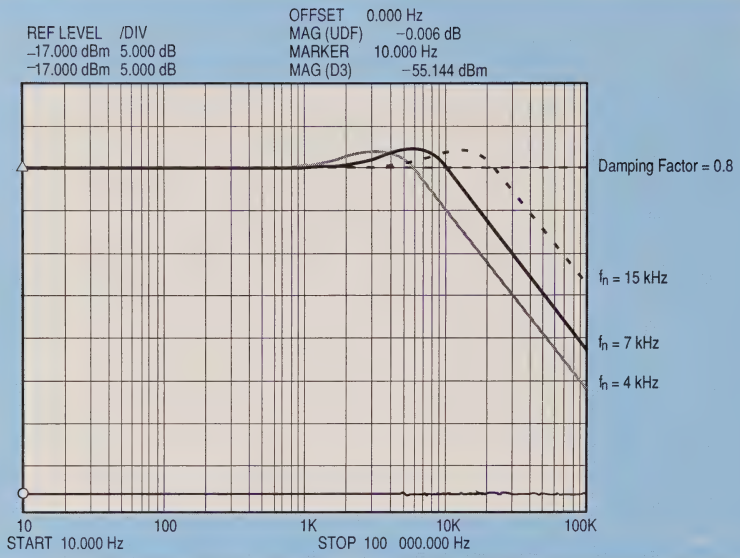


Figure 8. Closed-loop response for various natural frequencies.

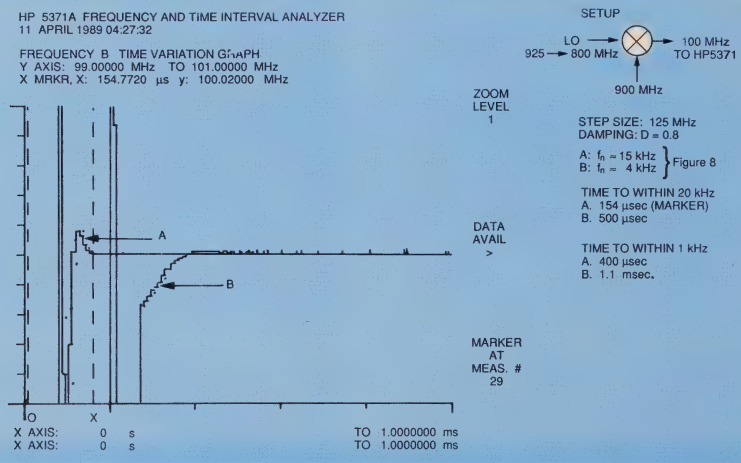


Figure 9. Step response versus natural frequency.

been presented. The actual design process for the PLL loop filter is much more detailed than the simplified examples presented here. The final loop filter is of much higher order to reduce reference sidebands and provide a greater attenuation slope. The intent of the discussion has not been to cover the details of higher order PLL design, but to examine the trade-offs and limitations imposed by the circuitry required to build the loop to meet specific performance goals.

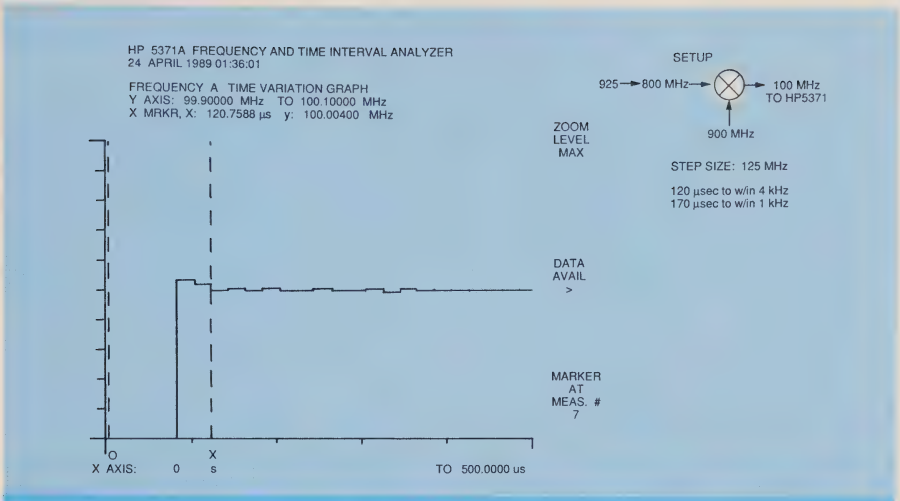


Figure 10. First LO switching speed.

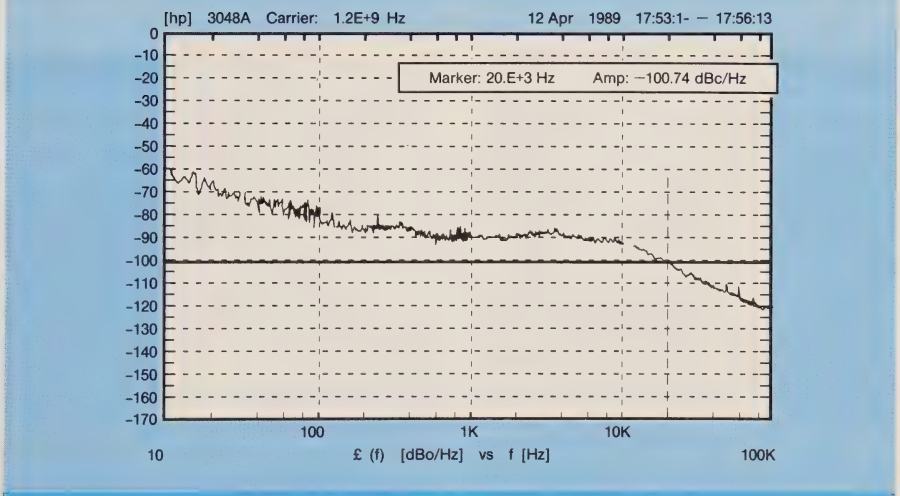


Figure 11. First LO phase noise at 1200 MHz.

Design Considerations For Fast Switching Speed And Fine Tuning Resolution

Thus far, only methods of achieving fast tuning with relatively large step sizes have been discussed. Generally, fast tuning is easier with larger steps due to the ability to use a higher reference frequency and a correspondingly wider loop bandwidth. The problem of fast tuning, while maintaining fine frequency resolution, has long been a problem of modern synthesized receivers.

In a typical receiver conversion plan, fine tuning resolution is accomplished in the second local oscillator synthesizer. Figure 12 shows the second LO

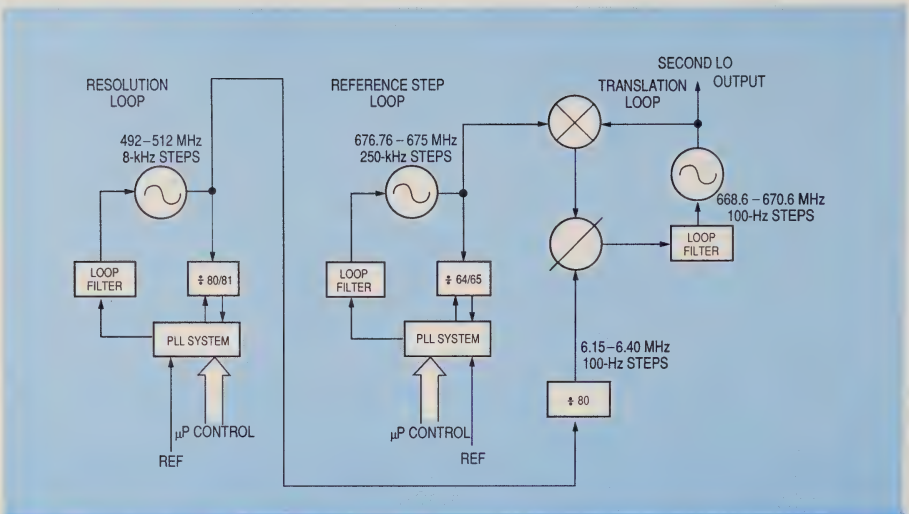


Figure 12. WJ-8607 Miniceptor second LO block diagram.

block diagram for the WJ-8607 Miniceptor Receiver. This synthesizer tunes from 668.6 MHz to 670.6 MHz in 100-Hz steps, and is a three-loop design employing a reference step loop, a resolution loop, and an output translation loop. The reference step loop tunes from 676.75 MHz to 675.00 MHz in 250-kHz steps, while the resolution loop tunes from 492 MHz to 512 MHz in 8-kHz steps. The output of the resolution loop is divided by 80, and the final output tunes from 6.15 MHz to 6.40 MHz. When these two loops are summed together in the output translation loop, the result is a fine-tuning synthesizer capable of 100-Hz resolution.

There are several advantages to this type of fine-tuning synthesizer design:

1. *Simplicity*—This type of synthesizer can be easily implemented with readily available integrated circuits (IC). The digital control is accomplished with relatively simple interface circuitry to a microprocessor controller. The bulk of the circuitry is contained on a few multifunction synthesizer IC chips. All of the digital dividers and prescalers are now commercially available on LSI chips. Surface-mount versions of the ICs are also available for high-density packaging designs.

2. *Low Power Consumption*—Due to the availability of high-speed CMOS synthesizer ICs, the power consumption of this type of synthesizer is typically only 300 milliwatts.

3. *Good Phase-Noise Performance*—Due to the high reference frequency of the reference step loop and the long division factor in the output of the resolution loop, the phase noise of the design is acceptable for general-purpose communications receivers. Figure 13 shows the phase-noise performance of the design.

The main disadvantage to this type of design is the limited tuning speed due to the resolution loop synthesizer. As previously discussed, there are two reasons for the slow tuning of the resolution loop. First, the low reference

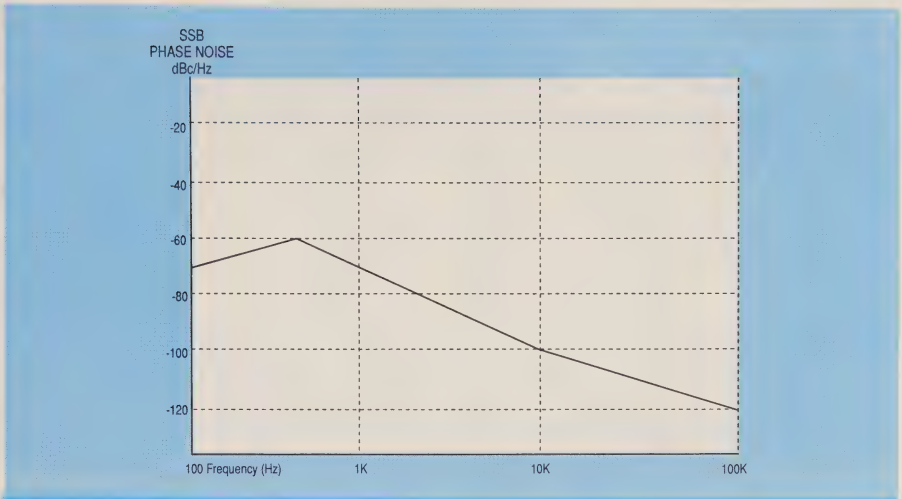


Figure 13. Second LO phase noise.

frequency of 8 kHz limits the number of error pulses the phase detector can generate for loop correction during tuning; second, the loop bandwidth must be kept narrow, typically 1 kHz, in order to attenuate the reference pulses that feed through the loop filter. The time required to tune this loop across the full tuning range is typically 8 milliseconds.

Direct Digital Synthesis

In order to decrease the time required to tune the second LO synthesizer, we must increase the speed of the resolution loop. In so doing, we do not want to sacrifice any of the important performance specifications, such as the phase noise, signal purity, or tuning resolution. One method of increasing the tuning speed would be to replace the resolution loop with a direct digital synthesizer. As mentioned earlier, direct digital synthesis has generated a great deal of interest in the past several years because of the tremendous improvements in performance that can be obtained with careful application of the technology. Direct digital synthesis offers improved tuning time, phase coherent switching, improved tuning resolution, and superior phase noise. Since a direct digital synthesizer can typically switch in much less than a microsecond, the overall tuning time of the second local oscillator would be limited only by the tuning time of the translation loop. Substituting a direct digital synthesizer for the resolution loop would require slight modification of the reference step loop. The reference source would become a fixed, non-tuning signal and, therefore, would not limit the tuning time.

Before discussing the new design for the second local oscillator, the design considerations for a phase-locked loop employing a direct digital synthesizer as a resolution source should be briefly discussed. Several excellent references are available for a complete discussion of direct digital synthesis; however, all of the theory will not be explored in this paper. A block diagram of the typical direct digital synthesizer is shown in Figure 14.

In general, direct digital synthesizers employ a phase accumulator that con-

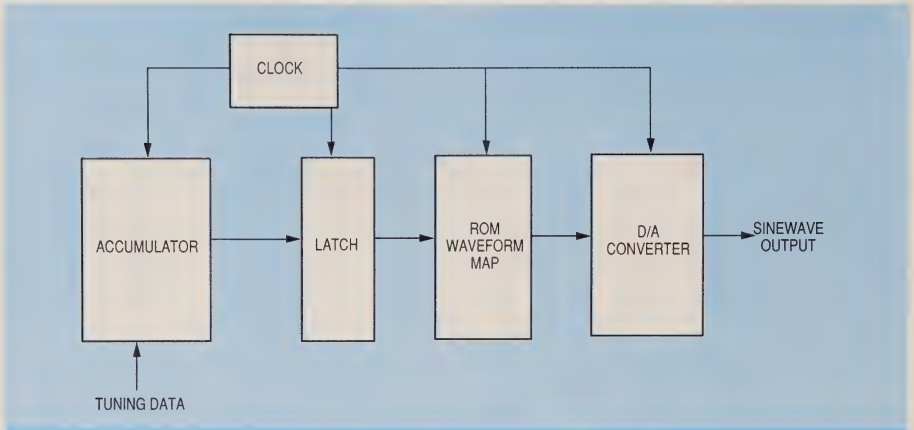


Figure 14. Direct digital synthesizer block diagram.

tains a number (P) representing the current phase of the output waveform. P is then used to obtain the corresponding value of the output waveform from the waveform map, which is stored in EPROM memory. The analog value of the output waveform is then generated by the digital-to-analog (D/A) converter. The output frequency of the synthesizer is given by the following equation:

$$F_{out} = \frac{F_{clk}}{2^N} \cdot M$$

Equation 13

where F_{clk} is the frequency of the clock, N is the number of accumulator bits, and M is the tuning number.

Using this equation, the smallest frequency step possible for a 24-bit accumulator and 20-MHz clock is 1.192 Hz, which is more than adequate for most applications.

The Digital RF Solutions DRFS-2250 Accumulator was chosen for this direct-digital synthesizer design because of the 100-milliwatt power consumption and the ease of chip interface. Several alternative interfaces are also available. For this application, the parallel 24-bit tuning bus was chosen. Digital RF Solutions also provides the waveform map, leaving the designer to select a suitable D/A converter. The TDC 1012 DAC was selected as one of the fastest 12-bit digital-to-analog converters available.

Local Oscillator Design Employing the DRFS-2250

Although there are many advantages to using direct digital synthesis, there are three practical limitations that must be considered. First, the spurious outputs of most direct digital synthesizers are limited by the performance of the digital-to-analog converters. Most current digital synthesizers will contain spurious outputs only 70 dB below the carrier. In modern receiver design, spurious outputs on the local oscillator signal mean unwanted spurious responses in the receiver. The key to understanding the impact of these spurs on receiver performance lies in predicting precisely where the spurs fall relative to the carrier of the local oscillator source. Spurs that are 70-dB down at an offset of 1 kHz from the carrier are not of major consequence in a VHF/UHF receiver where the operating bandwidths are typically tens of kilo-

hertz. However, the same spurious response moved out to a separation of 300 kHz will seriously limit the reciprocal mix performance of a receiver. When a strong out-of-band signal is input to the receiver with a frequency offset equal to the offset of the local oscillator spurious signal, the spur will be reciprocally mixed into the receiver IF passband. The undesired spurious response will degrade the signal-to-noise ratio of the desired signal in the passband. Proper filtering must be employed at the output of the digital synthesizer, as well as in the final output-loop translation to remove the undesired spurious signals.

Figure 15 shows the spurious outputs from the digital synthesizer. With the synthesizer tuned to 4.4 MHz, several large spectral lines are visible at 15.6 MHz and 20 MHz. These are typically the largest of the spurious outputs, and are caused by the 20-MHz clock and the difference between the clock frequency and the output frequency. Both of these unwanted spectral lines must be filtered before the signal is injected as the resolution reference. Figure 16 shows the output from the digital synthesizer after bandpass filtering and amplification. The bandpass filter that was used is a simple five-pole, 0.1-dB ripple Chebyshev filter, centered at 4.4 MHz. Note that the level of the 20-MHz and 15.6-MHz spurious outputs are attenuated by more than 80 dB.The increase in harmonic content of the signal is due to the limiting action of the amplifier following the bandpass filter.

There are also several spurious outputs that cross through the main output carrier at various points in the tuning range. Figure 17 shows the level of the crossover spurs that occur when the synthesizer is tuned to 1/4 of the 20-MHz clock frequency. Since these spurs cross through the carrier, filtering at the output of the digital synthesizer cannot remove the spur. However, as long as the spurs are no larger than about −70 dBc, acceptable performance can be attained by careful design of the translation loop filter. As the crossover spur tunes through the carrier, the loop filter will begin

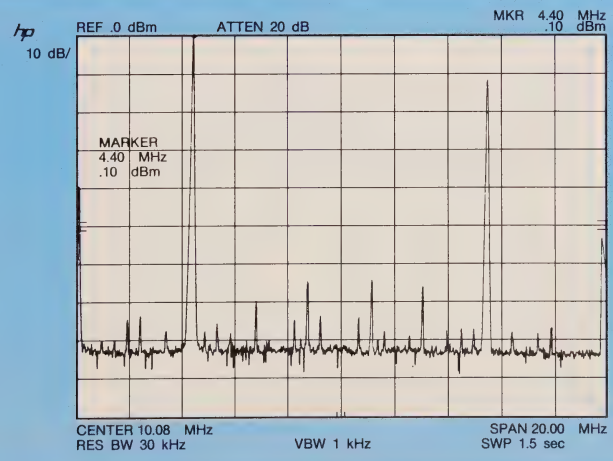


Figure 15. Spurious outputs.

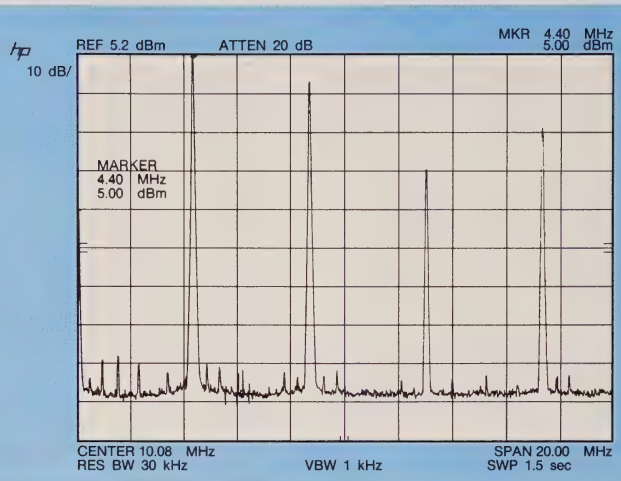


Figure 16. Spurious outputs after bandpass filtering.

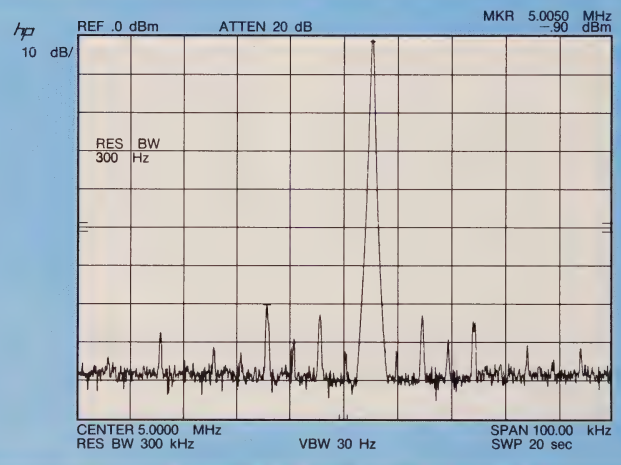


Figure 17. Spurious outputs close to carrier.

attenuating the spur as it crosses the loop bandwidth. Fortunately, all of the tune-through spurs are easily predicted. The largest two of these spurs are located at 1/3 and 1/4 of the clock frequency. In this case, for a clock frequency of 20 MHz, the tune-through spurs will be located at 5 MHz and 6.666 . . . MHz. By designing the synthesizer such that the tuning range of the digital synthesizer is 3.4 to 5.4 MHz, we will avoid the crossover spur at 6.666 . . . MHz.

The second limitation of digital synthesis that must be considered is the operating frequency. To date, the maximum output frequency of a low-powered digital synthesizer is limited to about 10 MHz. There are several sources of higher frequency digital synthesizers, but as a general rule,

power consumption and spurious outputs are both higher. The source of this limitation is primarily due to the speed of the D/A converters and the access time of the memory map used to generate the output waveform. Since the resolution loop of the synthesizer is required to tune over a maximum span of 2 MHz, it is well within the capabilities of the DRFS-2250.

The third limitation that must be considered is the difficulty in maintaining phase coherency with other synthesized sources. Because the accumulator is implemented in a binary format, the output frequency is always related to the inverse of a power of 2. As shown by Equation 13, one way to avoid this problem would be to use a clock frequency that is a power of 2. For example, a clock frequency of 2^{24} (16.777216 MHz) would yield exactly 1-Hz tuning resolution. A phase-locked loop could be built that locks a 16.777216 MHz crystal source to a 1-MHz precision reference by dividing both signals down to a common frequency of 64 Hz. Although this is a bit awkward and requires an extremely narrow loop bandwidth, it is possible. Eventually, digital synthesizer designers will develop accumulators that operate in BCD format which will yield decade tuning resolution with decade clock frequencies. Several manufacturers have begun to introduce such devices.

Figure 18 shows the block diagram of the second local oscillator with the direct digital loop substituted in place of the resolution loop. The reference step loop is now fixed at 674 MHz, allowing the digital synthesizer to tune the entire 2-MHz span from 3.4 to 5.4 MHz. The translated output follows the digital synthesizer and tunes the required range from 668.6 to 670.6 MHz. It is important to note that the translation loop VCO must be temperature-compensated such that the drift in frequency never crosses over the 674-MHz reference loop. The mixing product caused by the translation oscillator mixing on the high side of the 674-MHz reference could cause the loop to generate an error voltage that would force the translation oscillator to drift still further from the

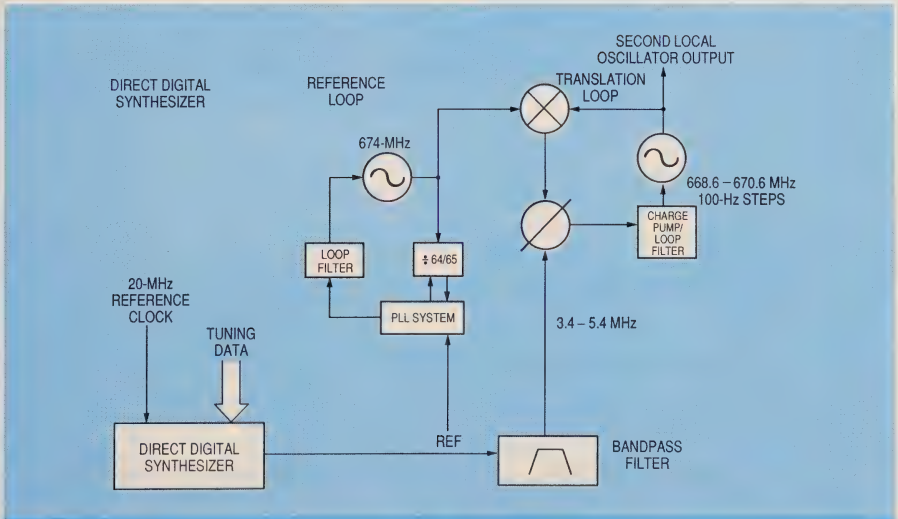


Figure 18. Second local oscillator with direct digital synthesizer block diagram.

correct frequency. A higher intermediate frequency of the loop could have been chosen which would help the image lock problem, but then the spurious products that occur at F_{clk} and $F_{out} - F_{clk}$ would be all the more difficult to filter out, since they would be closer to the desired carrier signal.

Phase-Noise Considerations

If possible, the design of the new second local oscillator would ideally have phase-noise performance at least as good as the original design. The phase-noise performance can be predicted easily if the phase noise of the reference loop and digital loop are known. Figure 19 shows the phase noise of the reference loop together with the phase noise of the digital synthesizer. Since the noise performance of the digital synthesizer is predominated by the clock used, excellent performance is obtained by using a good-quality crystal-clock oscillator. Since there is no digital divider in this loop, the final output phase noise is determined by the sum of the 674-MHz loop phase noise and the phase noise of the digital synthesizer. The noise contribution of the digital synthesizer is small in comparison to the 674-MHz loop, and it can be ignored. Therefore, the final output phase noise from the translation loop is set by the noise of the 674-MHz reference loop for offset frequencies that are less than the translation-loop bandwidth. For offsets greater than the translation-loop bandwidth, the translation-loop VCO sets the phase-noise performance.

Figure 19 also shows the additional improvement in the phase-noise performance if the 674-MHz reference loop VCO is redesigned to incorporate a surface-acoustic-wave resonator. As can be seen from the graph, a 20-dB reduction in the phase noise can be achieved at 1-kHz offset from the carrier. The 674-MHz resonator is a component readily available from several manufacturers and is used in commercial CATV applications. In this instance, the phase noise is set predominantly by the 674-MHz SAWR VCO out to about 20 kHz, where the phase noise of the direct digital synthesizer begins to contribute to the total noise.

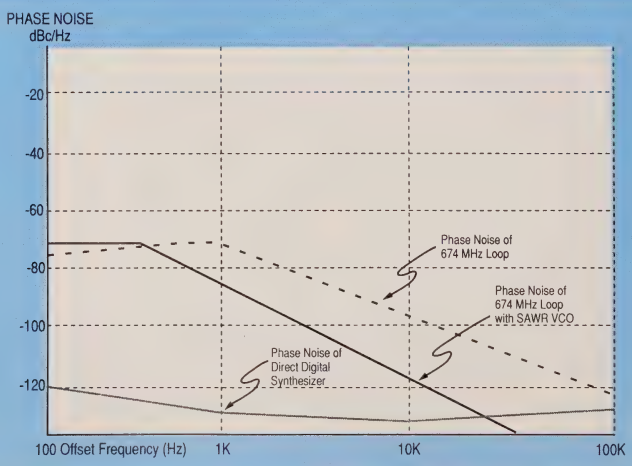


Figure 19. Phase noise of 674-MHz reference loop and DDFS.

Loop-Bandwidth Considerations

The optimum point for setting the translation loop bandwidth is based on the desired tuning time and the rejection of spurious responses caused by the direct digital synthesizer. In this design, we wish to minimize the tuning time while simultaneously maximizing attenuation to crossover spurious signals. We must consider how the spurious outputs of the digital synthesizer will affect the overall receiver performance. In a typical high-performance receiver, we would want to suppress spurious outputs to at least −80 dBc at an offset of 100 kHz. With spurious outputs only −70 dBc out of the digital synthesizer, we would be required to set the loop bandwidth at roughly 25 kHz in order to realize 12 dB of attenuation with a second-order loop—assuming our loop is critically damped. Depending on the individual application, the loop bandwidth can be moved closer or further out, and the damping factor can be adjusted to achieve a good tradeoff between speed and spurious performance. Once the optimum loop bandwidth is determined, Equations 10, 11 and 12 can be used to arrive at values for the loop filter components. For this design, we would like to have 10 dB of attenuation at 100 kHz, as well as having the bandwidth as wide as possible. The following parameters are given:

K_v = 2 MHz/volt
K_p = 1.8 mA/2π
N = 1

ωn = 1.89 E + 5 Radians
D = 0.53
BW = 55.8 E + 3 Hertz

For R = 56 ohms
and C = 0.1 μFarad

The values chosen for R and C were adjusted iteratively with a programmable calculator to yield standard value components that satisfy the design.

Figure 20 shows the closed-loop response of the translation-loop synthesizer. With the damping set at 0.53, the attenuation at 100 kHz falls right on our goal of 10 dB. The 3-dB bandwidth is also very close to the calculated value.

Tuning Time

Based on the earlier discussions of tuning time and bandwidth, it should be apparent that the tuning time of this loop will be relatively fast. Figure 21 shows the actual measured settling time of the synthesizer for a full 2-MHz frequency step. The upper trace shows the tuning command occurring at t = 50 microseconds. The lower trace is the output of an FM discriminator which is calibrated to 10 kHz per division. The markers show the elapsed time from the tuning command to settling of the synthesizer to within 10 kHz to be 128 microseconds. Settling to within 2 kHz requires approximately 150 microseconds, and 1-kHz settling requires 175 microseconds.

The overall tuning time of the synthesizer can be custom tailored for each application based on the required spurious rejection. Tuning times as fast as 25 microseconds are easily achieved by moving the loop bandwidth out to several megahertz.

Second LO Summary

We have shown one possible application of direct digital synthesis in increasing the tuning speed of a phase-locked loop while maintaining fine frequency resolution. As the state-of-the-art in direct digital synthesis

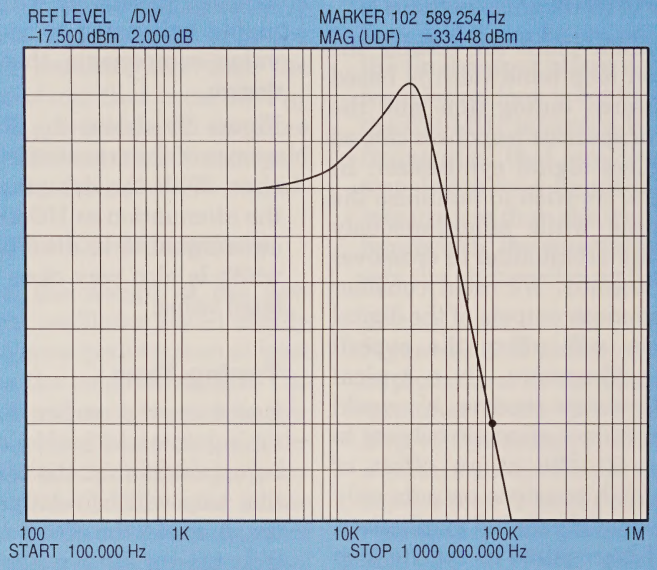


Figure 20. Closed-loop frequency response.

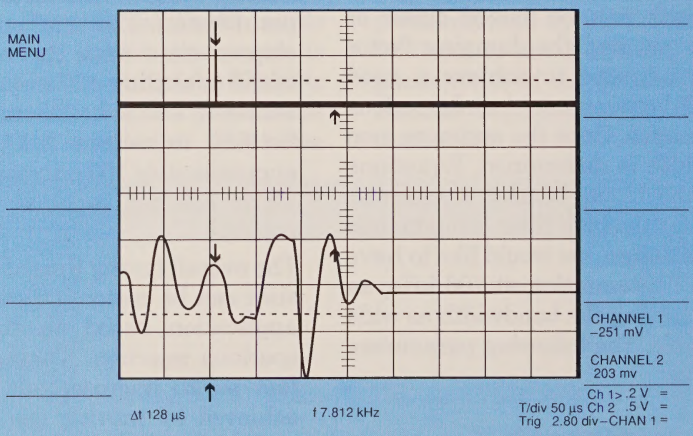


Figure 21. Tuning time.

improves, further improvements in spurious-signal rejection will allow movement of the final translation loop bandwidth out further, thus achieving even faster tuning.

References

1. Rhode, Ulrich L. *Digital PLL Frequency Synthesizers Theory and Design,* Prentice Hall, Inc., 1983.
2. Manassewitsch, V. *Frequency Synthesis,* John Wiley and Sons, Inc., 1976.
3. Gavin, D. "Phase Locked Loop Synthesizer Switching Speed Optimization and Measurement Techniques," *Proceedings RF EXPO 89.*
4. Plessey Semiconductors, *Frequency Dividers and Synthesizers IC Handbook.*
5. Yeager, R. "Control and Automate PLL Phase Detector Gain," *Microwaves and RF, August 1986.*
6. McCune, Earl W., President, Digital RF Solutions, *Direct Digital Synthesis and the Numerically Controlled, Modulated Oscillator.*

Gigabit Logic, *1988 GaAs IC Data Book and Designers Guide.*

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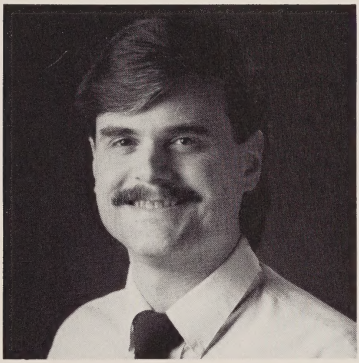

William C. Beam

Mr. Beam is Head, Receiver Engineering section, Watkins-Johnson Company CET Division. His responsibilities include design, development, and product support for the WJ-861XB, WJ-8615, WJ-860X, and WJ-8700 families of surveillance receivers. Administrative responsibilities include project planning, budgeting, scheduling, supervision and the coordination of engineering personnel to meet departmental objectives.

Mr. Beam holds a B.S.E.E. degree from Virginia Polytechnic Institute and State University, and is pursuing graduate studies in engineering management at George Washington University.

Phillip J. Rezin

Mr. Rezin is Head, Synthesizer Engineering, Collection Equipment Department, Watkins-Johnson Company CET Division. He is responsible for directing and coordinating the activities of synthesizer engineering, including the design of new synthesizer products. Typical design responsibilities include noise analysis, low-noise VCO design, and single and multiloop PLL designs. The synthesizers developed, range from low-noise VLF and HF synthesizers to fast-tuning, low-noise VHF/UHF synthesizers combining PLL techniques with direct digital synthesis.

Mr. Rezin holds a B.S.E.E. degree from the University of Illinois.

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 Printed in U.S.A.