GBPPR 'Zine

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"The fact that we are here today to debate raising America's debt limit is a sign of leadership failure. It is a sign that the U.S. government can't pay its own bills. It is a sign that we now depend on ongoing financial assistance from foreign countries to finance our government's reckless fiscal policies.

Increasing America's debt weakens us domestically and internationally. Leadership means that 'the buck stops here.' Instead, Washington is shifting the burden of bad choices today onto the backs of our children and grandchildren.

America has a debt problem and a failure of leadership. Americans deserve better."

––– Quote from then–Senator Barack Hussein Obama on the increasing the debt limit, which he voted *against* in 2006, as recorded in the Congressional Record for the Senate S. 2237–8 March 16, 2006. He never even bothered to vote on the debt limit in 2007 or 2008. Change!

(rpc.senate.gov/public/_files/alternativestothedebtlimitincreasev20.pdf)

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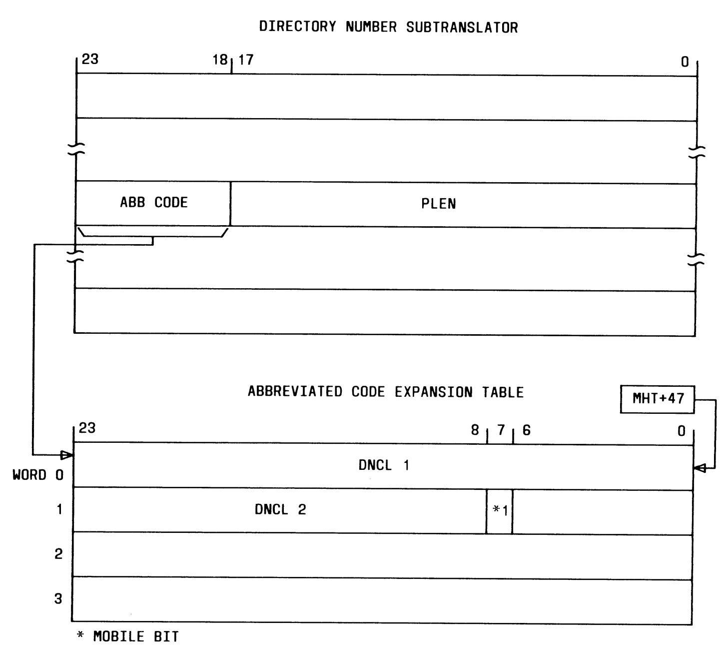


Fig. 4—Directory Number Translator

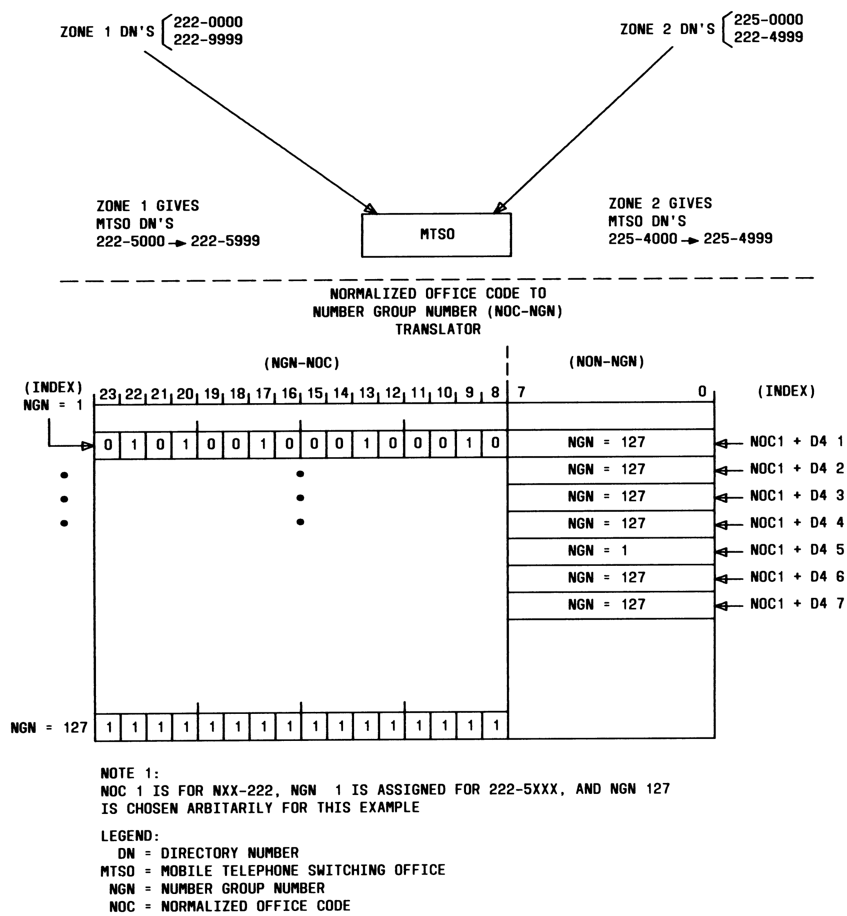


Fig. 5—Example of Mobile DN Assignment

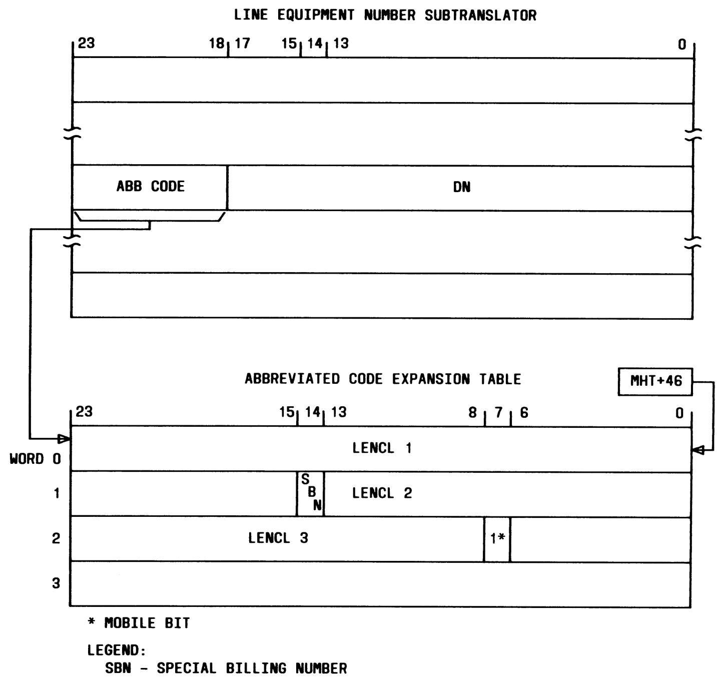
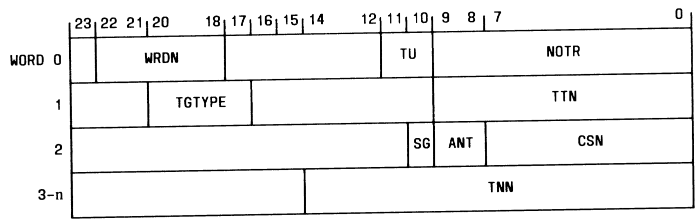
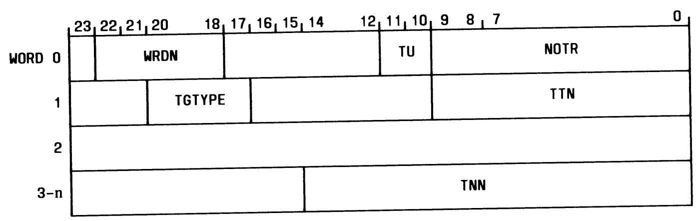


Fig. 6—Line Equipment Number Translator



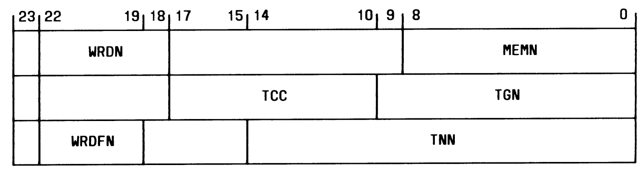
LEGEND:
ANT – ANTENNA FACE
CSN – CELL SITE NUMBER (1-255)
NOTR – NUMBER OF TRUNKS IN GROUP
SG – SERVER GROUP
TGTYPE – TRUNK GROUP TYPE=13 FOR ONE-WAY, = 6 FOR 2-WAY
TNN – TRUNK NETWORK NUMBER
TTN – TEST TABLE NUMBER
TU – TRUNK USAGE (SET TO 2 FOR TWO-WAY, SET TO 0 OR 2 FOR ONE-WAY)
WRGN – NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 7—Trunk Group Number Translator Auxiliary Block



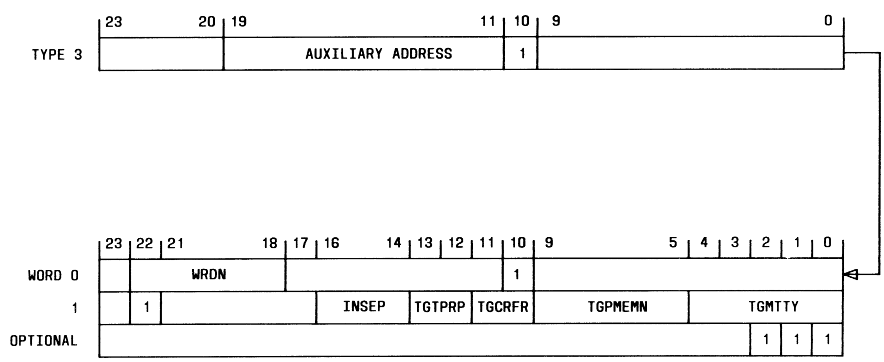
LEGEND:
NOTR – NUMBER OF TRUNKS IN GROUP
TGTYPE – TRUNK GROUP TYPE=2
TNN – TRUNK NETWORK NUMBER
TTN – TEST TABLE NUMBER
TU – TRUNK USAGE (SET TO 2 FOR "AUTOPLEX" SYSTEM 100)
WRGN – NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 8—Trunk Group Number Translator Auxiliary Block for Loop-Around Trunks



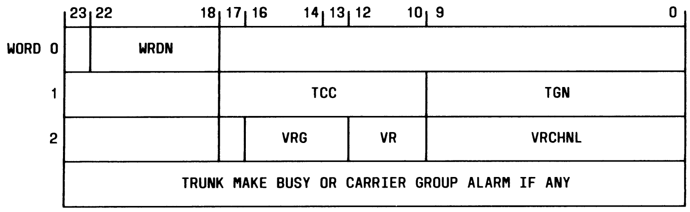
LEGEND:
MEMN – MEMBER NUMBER
TCC – TRUNK CLASS CODE
TGN – TRUNK GROUP NUMBER
TNN – TRUNK NETWORK NUMBER
WRDFN – WORD FUNCTION
WRDN – NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 9—Trunk Network Number to Trunk Group Number Translator Auxiliary Block for Loop-Around Trunks



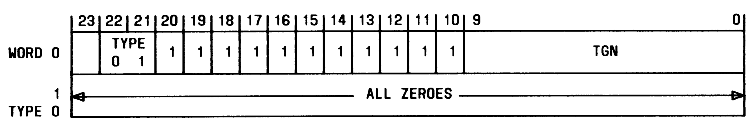
LEGEND:
INSEP – INCOMING SEPARATION OF REVENUE CLASS
TGCRFR – TRUNK GROUP CRAFT FORCE RESPONSIBILITY
TGMTTY – TRUNK GROUP MAINTENANCE TTY CHANNEL
TGPMEMN – TRUNK GROUP TEST PANEL MEMBER NUMBER
TGTPRP – TRUNK GROUP TEST PAD REFERENCE POINT

Fig. 10—Trunk Group Number Supplementary Table Translator



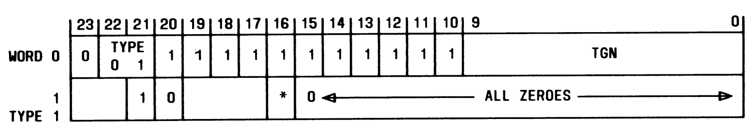
LEGEND:
TCC - TRUNK CLASS CODE
TGN - TRUNK GROUP NUMBER
VR - VOICE RADIO NUMBER
VRCHNL - RADIO CHANNEL NUMBER
VRG - VOICE RADIO GROUP
WRDN - NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 11—Trunk Network Number to Trunk Group Number Translator Auxiliary Block for Cell Site Trunks



LEGEND:
PRI - PSEUDO ROUTE INDEX
TGN - TRUNK GROUP NUMBER

Fig. 12—Pseudo Route Index Expansion Tables for PRI 045, 057, 058, 059, 060, and 061



*RS
LEGEND:
RI - ROUTE INDEX
RS - RETURN SUPERVISION
TGN - TRUNK GROUP NUMBER

Fig. 13—Route Index Expansion Table for RI 131

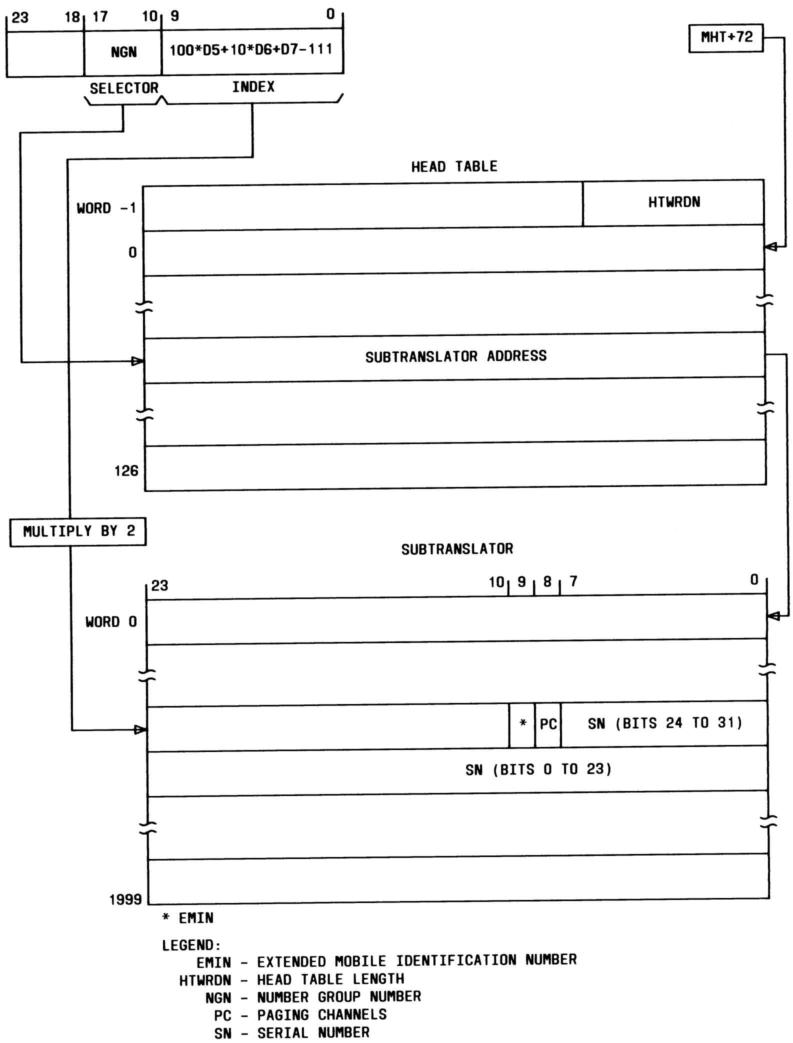


Fig. 14—Directory Number to Serial Number Translator

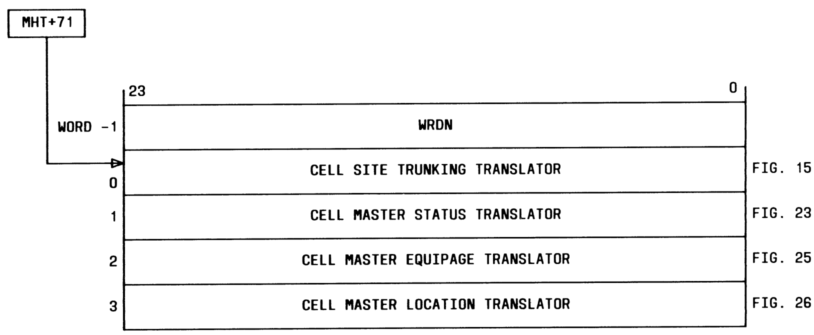


Fig. 15—Cell Site Translator

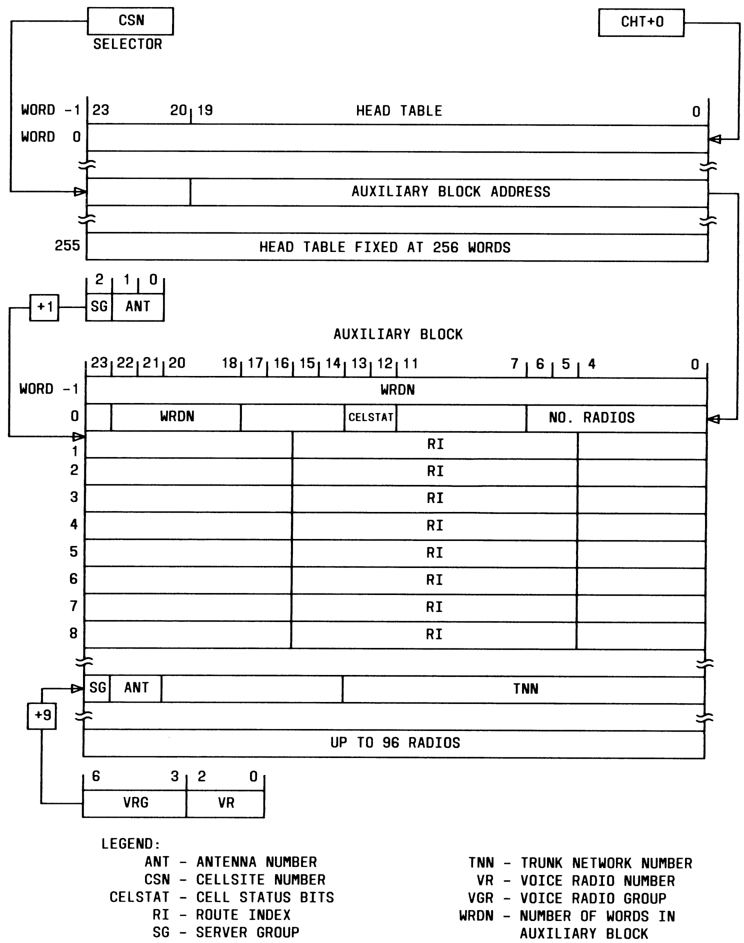
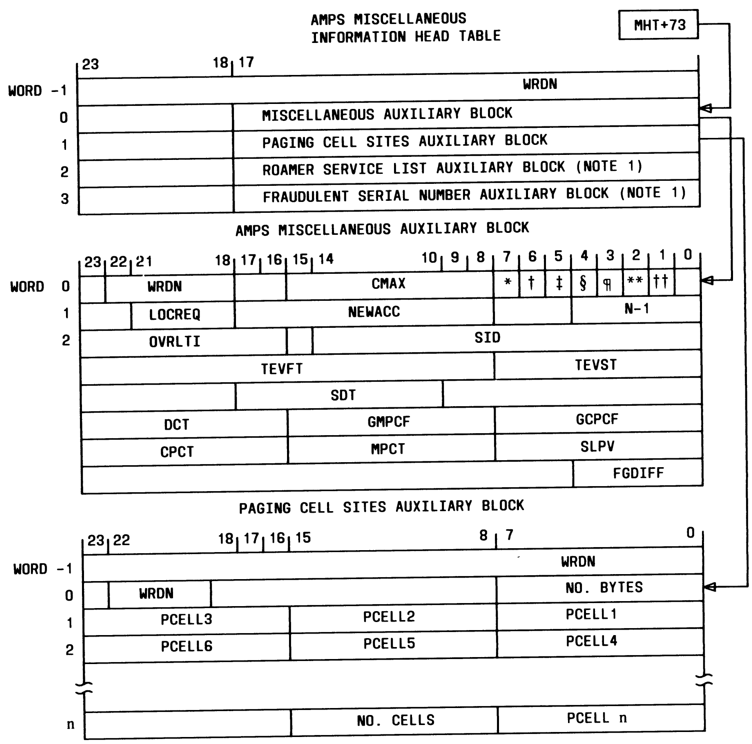


Fig. 16—Cell Site Trunking Translator



* NWAC † RCF ‡ DTX § SRN ¶ CPA ** LPB †† RSV

NOTE:
1. FOR DETAILS OF THE ROAMER SERVICE LIST AND FRAUDULENT SERIAL NUMBER AUXILIARY BLOCK, REFER TO REFERENCE (13) IN PARTH 18.

Fig. 17—AMPS Miscellaneous Information Translator (Sheet 1 of 2)

LEGEND:

CMAX	- MAXIMUM NUMBER OF ACCESS CHANNELS THE MOBILE HAS TO SCAN
CPA	- COMBINED PAGING AND ACCESS
CPCT	- CELLSITE PROCESS COUNTER THRESHOLD
DCT	- DIVERSITY COUNTER THRESHOLD
DTX	- DISCONTINUOUS TRANSMISSION
FGDIFF	- FRAME GAIN DIFFERENTIAL
GCPCF	- GLOBAL CELL SITE POWER CONTROL FLAG
GMPCF	- GLOBAL MODIBLE POWER CONTROL FLAG
LOCREQ	- LOCATION REQUEST LIMIT
LPB	- LONG PAGE BUNDLING
MPCT	- MOBILE PROCESS COUNTER THRESHOLD
N-1	- NUMBER OF PAGING CHANNELS THE MOBILE HAS TO SCAN
NEWACC	- NEW ACCESS CHANNEL
NO. BYTES	- NUMBER OF BYTES (8 BITS)
NO. CELLS	- NUMBER OF CELLS
NWAC	- NEW ACCESS CHANNEL
OVRLTI	- VOICE RADIO LOCATION TIME INTERVAL DURING OVERLOAD
PCELL	- PAGING CELL SITES
RCF	- READ CONTROL FILLER WORD
RSV	- ROAMER SERVICE VALIDATION
SDT	- SAT DETECT THRESHOLD
SID	- SYSTEM IDENTIFICATION NUMBER
SLPV	- SKIP LOCATE PERIOD VALUE
SRN	- SEND SERIAL NUMBER
TEVFT	- TRAFFIC EVENT FAILURE THRESHOLD
TEVST	- TRAFFIC EVENT SUCCESS THRESHOLD
WRDN	- NUMBER OF WORDS IN THE AUXILIARY BLOCK

Fig. 17—AMPS Miscellaneous Information Translator (Sheet 2 of 2)

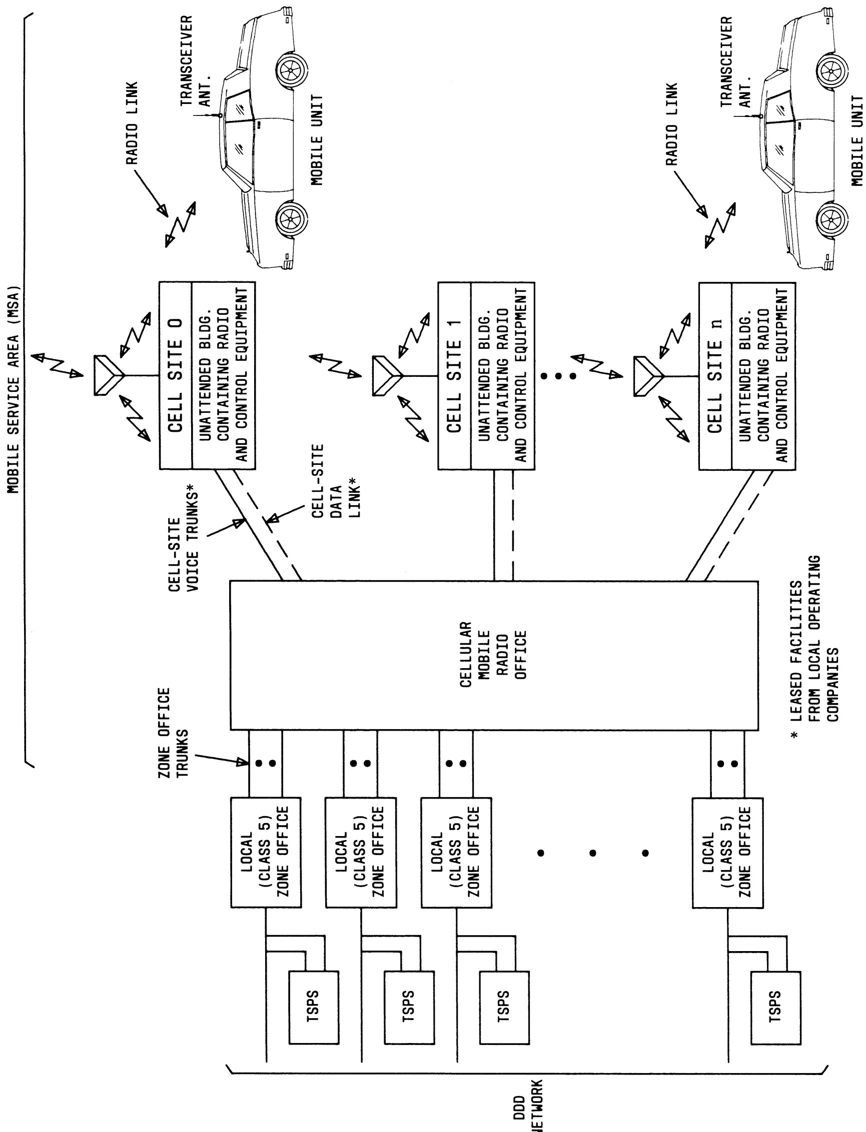
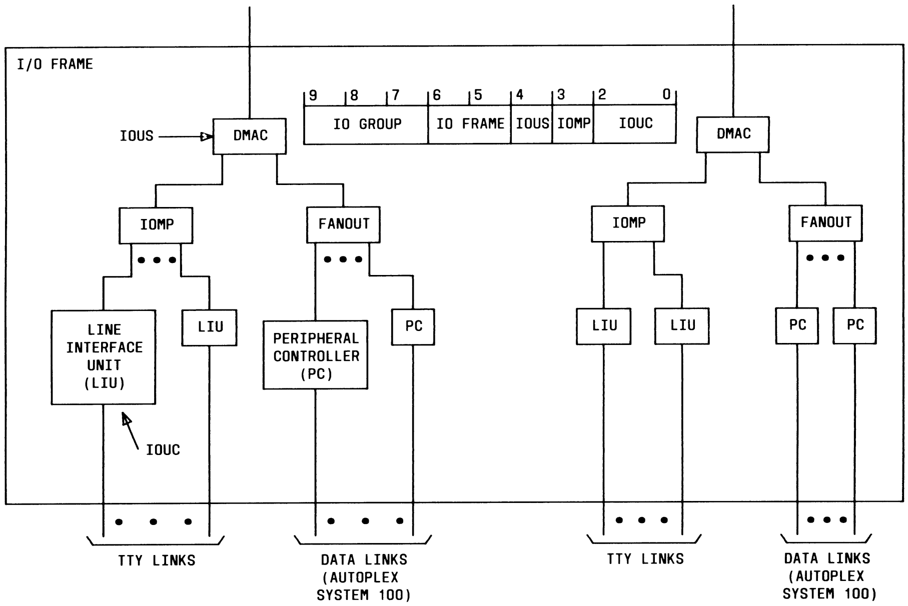


Fig. 18—IOP K-Code to Cell Site Channel Number Translator (Note 1)



NOTE:
1. FOUR I/O FRAMES PER I/O GROUP

LEGEND:
IOMP - INPUT/OUTPUT MICROPROCESSOR
IOUC - INPUT/OUTPUT UNIT CONTROLLER
IOUS - INPUT/OUTPUT UNIT SELECTOR

Fig. 19—I/O Member Configuration (Note 1)

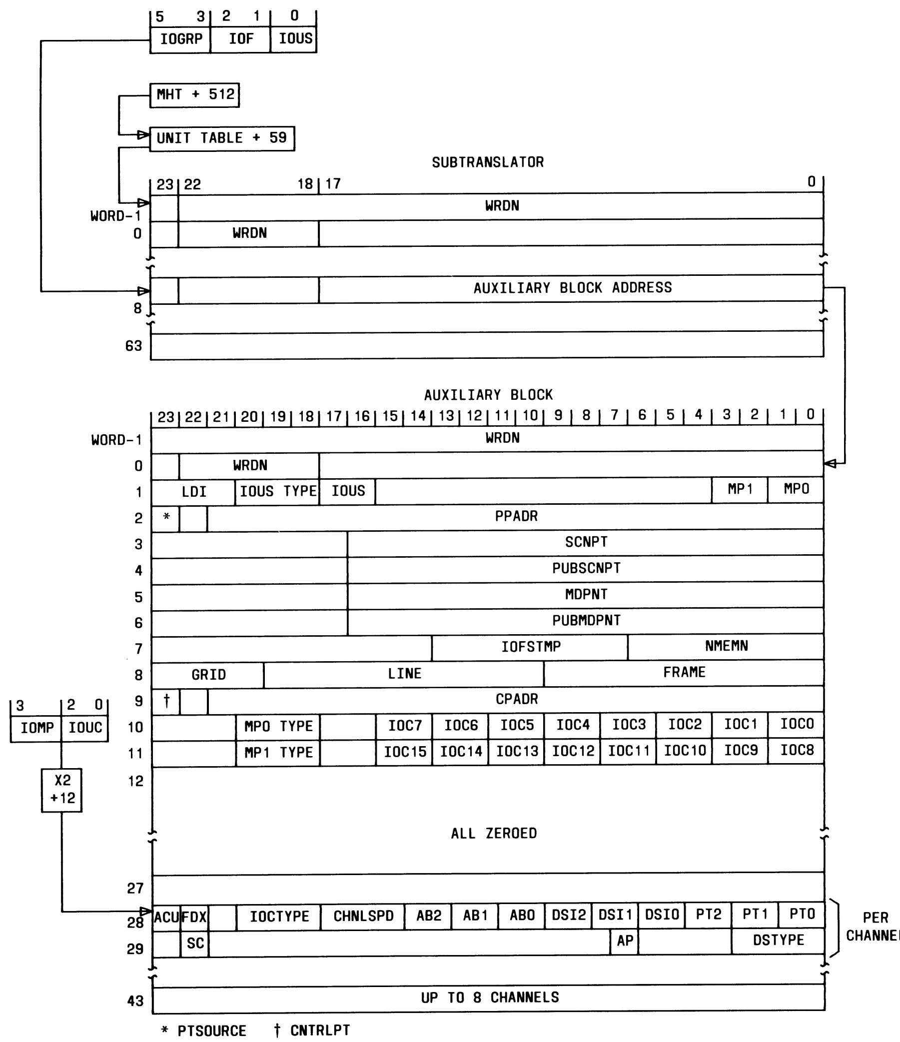


Fig. 20—I/O Processor Member Number Translator (Sheet 1 of 2)

LEGEND:

AB0-AB2	- INDICATES WHETHER PORT 0-2, RESPECTIVELY, IS EQUIPPED WITH ANSWER BACK (HANDSHAKING)=0
ACU	- INDICATES WHETHER AN AUTOMATIC CALL UNIT IS CONNECTED TO THE CHANNEL=0
AP	- INDICATES WHETHER AN APPLICATION IS CONTROLLING THE LINK=1
CHNLSPD	- CHANNEL SPEED OF THE CHANNEL
CNTRLPT	- INDICATES WHETHER THE CONTROL PULSE POINT IN A CC-GCP POINT OR ANOTHER TYPE OF POINT=0 OR 1
CPADR	- CONTROL PULSE POINT OCTAL ADDRESS
DS0-DS2	- DATA SET INDICATOR FOR PORT 0-2, RESPECTIVELY
DSTYPE	- TYPE OF DATA SET ON THE CHANNEL
FDX	- INDICATES WHETHER THE CHANNEL IS HALF OR FULL DUPLEX=1
IOCTYPE	- TYPE OF I/O CONTROLLER ON THE CHANNEL=7
IOC0-IOC15	- EQUIPPAGE FIELDS FOR I/O UNIT CONTROLLERS 0-15, RESPECTIVELY
IOGRP	- I/O GROUP
IOF	- I/O FRAME
IOUS	- I/O UNIT SELECTORS
IOUSTYPE	- TYPE OF IOUS CURRENTLY BEING USED=001
LDI	- HARDWARE LDI NUMBER
MDPNT	- UNIPOLAR CPD POINT ADDRESS OF THE FIRST OF EIGHT SIGNAL DISTRIBUTOR POINTS NEEDED PER I/O FRAME
MP0-MP1	- EQUIPPAGE STATUS OF MICROPROCESSOR 1 OR 2, RESPECTIVELY
NMEMN	- OTHER I/O MEMBER NUMBER IN THE I/O FRAME
PPADR	- PULSE POINT ADDRESS
PTSOURCE	- INDICATES THE FORMAT OF THE IOUS PULSE POINT SOURCE=1
PT0-PT2	- EQUIPPAGE OF PORT 0-2, RESPECTIVELY
PUBMDPNT	- ADDRESS OF THE SET OF SCAN POINTS FOR THE PUB TO THE I/O FRAME
PUBSCNPT	- ADDRESS FOR THE SET OF SCAN POINTS OF THE PUB SERVING THIS FRAME
SC	- TYPE OF TRANSMISSION ON THE CHANNEL=0
SCNPT	- SUPERVISORY MASTER SCANNER OCTAL SCAN POINT ADDRESS OF THE POWER CONTROL SWITCH ASSIGNED TO EACH IOUS.
WRDN	- NUMBER OF WORDS IN AUXILIARY BLOCK

Fig. 20—I/O Processor Member Number Translator (Sheet 2 of 2)

2	2	2	2
7 6	5 4	3 2	1 0
IOUS B	IPUB 1	IOUS A	IPUB 0

(a) ITEMS SCNPT AND PUBSCNPT SPECIFY THE SCAN POINT ADDRESS OF THE POWER CONTROL SWITCH ASSIGNED TO EACH IOUS AND THE SCAN POINT ADDRESS OF THE PUB (PERIPHERAL UNIT BUS) SERVING THIS FRAME, RESPECTIVELY. THE SCNPT AND PUBSCNPT LEAD DESIGNATIONS ARE AS FOLLOWS:

POINT	LEAD DESIGNATIONS
SC0	OSCBP (POSITIVE LEAD) OSCBN (NEGATIVE LEAD)
SC1	OSCAP OSCAN
SC2	ASCBP ASCBN
SC3	ASCAP ASCAN
SC4	1SCBP 1SCBN
SC5	1SCAP 1SCAN
SC6	BSCAP BSCBN
SC7	BSCAP BSCAN

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 1 of 3)

(b) ITEMS MDPNT AND PUBMDPNT SPECIFY THE BIPOLAR CPD (CENTRAL PULSE DISTRIBUTOR) POINT ADDRESS OF THE SIGNAL DISTRIBUTOR POINTS NEEDED PER IOUS AND THE SET OF BIPOLAR POINTS FOR THE PUB TO I/O FRAME, RESPECTIVELY. THE MDPNT AND PUBMDPNT LEAD DESIGNATIONS ARE AS FOLLOWS:

POINT	LEAD DESIGNATIONS
MD0	0COSP 0COSN
MD1	0CACKP 0CACKN
MD2	ACOSP ACOSN
MD3	ACACKP ACACKN
MD4	1COSP 1COSN
MD5	1CACKP 1CACKN
MD6	BCOSP BCOSN
MD7	BCACKP BCACKN

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 2 of 3)

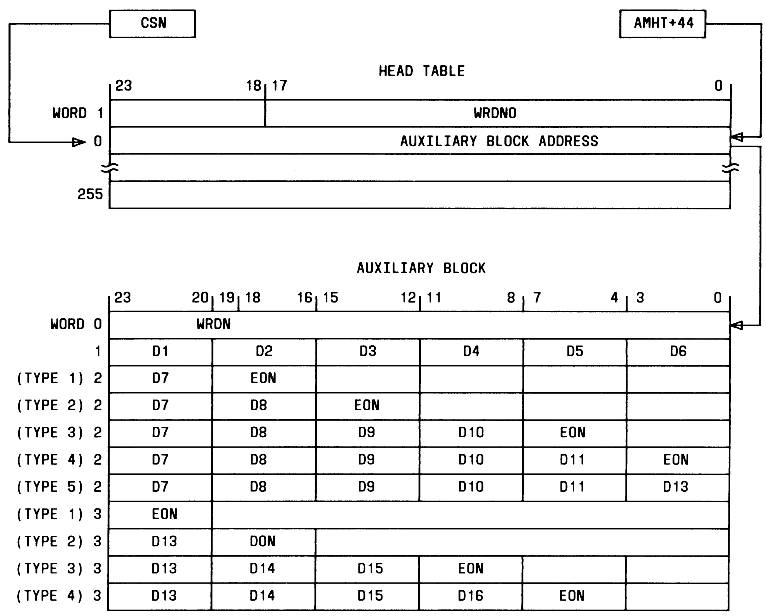
```
(c) ITEM CPADR SPECIFIES A UNIPOLAR CPD POINT. THE
    CPD POINTS ARE ASSIGNED IN CONSECUTIVE ORDER
    FOR THE ENTIRE GROUP OF I/O PROCESSORS (8-63).
    THE LEAD DESIGNATIONS ARE AS FOLLOWS:

                 FOR AN EVEN NUMBERED CPD

           CPD POINT              LEAD DESIGNATIONS
CONTROL
POINTS FOR  XXXX N                    0GCP1N1
IOUS A      XXXX P                    0GCP1P1

CONTROL
POINTS FOR  XXXX N                    0GCP1N1A
IOUS B      XXXX P                    0GCP1P1A

                 FOR AN ODD NUMBERED CPD

           CPD POINT              LEAD DESIGNATIONS
CONTROL
POINTS FOR  XXXX N                    1GCP1N1
IOUS A      XXXX P                    1GCP1P1

CONTROL
POINTS FOR  XXXX N                    1GCP1N1A
IOUS B      XXXX P                    1GCP1P1A

      XXXX IS THE 4-DIGIT NUMBER REPRESENTING CPD POINTS
      IN THE CPD ASSIGNMENT TABLES, REPRESENTING (FROM
      LEFT TO RIGHT) HALF, GROUP, ROW, AND COLUMN.
```

Fig. 21—I/O Processor Frame Scan Point Assignment and Lead Designations (Sheet 3 of 3)

23	22 21	20 … 13	12 … 7	6 … 0
0	0 1	NTPI = 27	UTYN = 59	MEMN = EVEN NUMBERED MEMBER NUMBER

LEGEND:
- MEMN – MEMBER NUMBER
- NTPI – NONTRUNK PROGRAM INDEX
- UTYN – UNIT TYPE NUMBER

Fig. 22—Master Scanner Number and Central Pulse Distributor Subtranslator Word

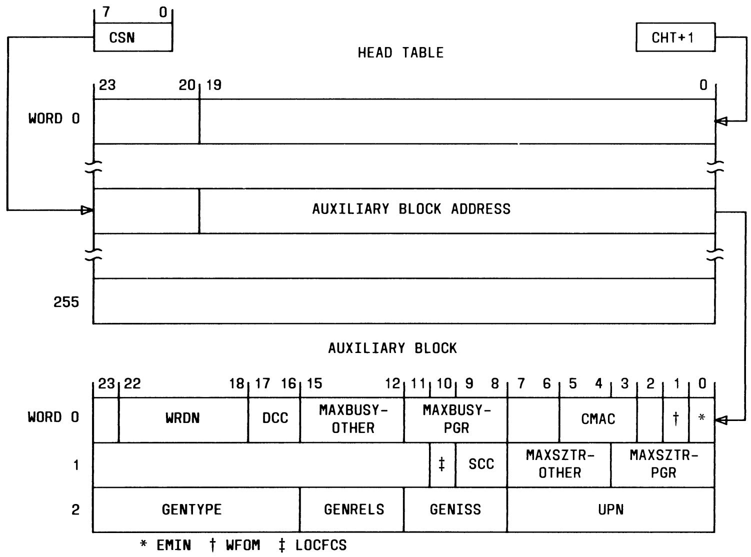


WORD 2 TYPE 1 – 7 DIGIT DN
TYPE 2 – 1+7 DIGIT DN
TYPE 3 – 10 DIGIT DN
TYPE 4 – 1+10 DIGIT DN
TYPE 5 – 10XXX+ (MUST HAVE WORD 3 WITH THIS TYPE)

WORD 3 TYPE 1 – 10XXX+7 DIGIT DN
TYPE 2 – 10XXX+17 DIGIT DN
TYPE 3 – 10XXX+10 DIGIT DN
TYPE 4 – 10XXX+1++10 DIGIT DN
(ZEROS ARE STORED AS ZEROS)

LEGEND:
CSN – CELL SITE NUMBER
CSN – END OF NUMBER INDICATOR
WRDN – NUMBER OF WORDS IN AUXILIARY BLOCK
HRDNO – LENGTH OF HEAD TABLE

Fig. 23—Cell Dialup Channel Translator



LEGEND:

CMAC – CONTROL MOBILE ATTENUATION CODE
DCC – DIGITAL COLOR CODE
EMIN – EXTENDED MOBILE IDENTIFICATION NUMBER
GENISS – GENERIC ISSUE
GENRELS – GENERIC RELEASE NUMBER
GENTYPE – GENERIC TYPE
LOCFCS – LOCATION EQUIPPED FACES
MAXBUSY-OTHER – SAME AS MAXBUSY-PGR, EXCEPT THAT THE MOBILE IS ATTEMPTING TO ACCESS THE SYSTEM FOR ANOTHER REASON BESIDES PAGE RESPONSE
MAXSZTR-OTHER – SAME AS MAXSZTR-PGR, EXCEPT THAT THE MOBILE IS ATTEMPTING TO SEIZE A CHANNEL WITH ANOTHER TYPE OF MESSAGE BESIDE A PAGE RESPONSE
MAXBUSY-PGR – NUMBER OF TIMES A MOBILE IS ALLOWED TO FIND A SETUP CHANNEL BUSY BEFORE GIVING UP WITH ITS PAGE RESPONSE MESSAGE
MAXSZTR-PGR – NUMBER OF TIMES A MOBILE IS ALLOWED TO TRY TO SEIZE A SETUP CHANNEL BEFORE GIVING UP WITH ITS PAGE RESPONSE
SCC – SAT COLOR CODE
UPN – UPDATE NUMBER
WFOM – WAIT FOR OVERHEAD MESSAGE
WRDN – NUMBER OF WORDS IN THE AUXILIARY BLOCK

Fig. 24—Cell Master Status Translator

MOBILE ATTENUATION CODE	MOBILE-STATION POWER CLASS		
	I	II	III
000	0	4	8
001	4	4	8
010	8	8	8
011	12	12	12
100	16	16	16
101	20	20	20
110	24	24	24
111	28	28	28

Fig. 25—Interpretation of Mobile Attenuation Codes and Mobile Station Power Class

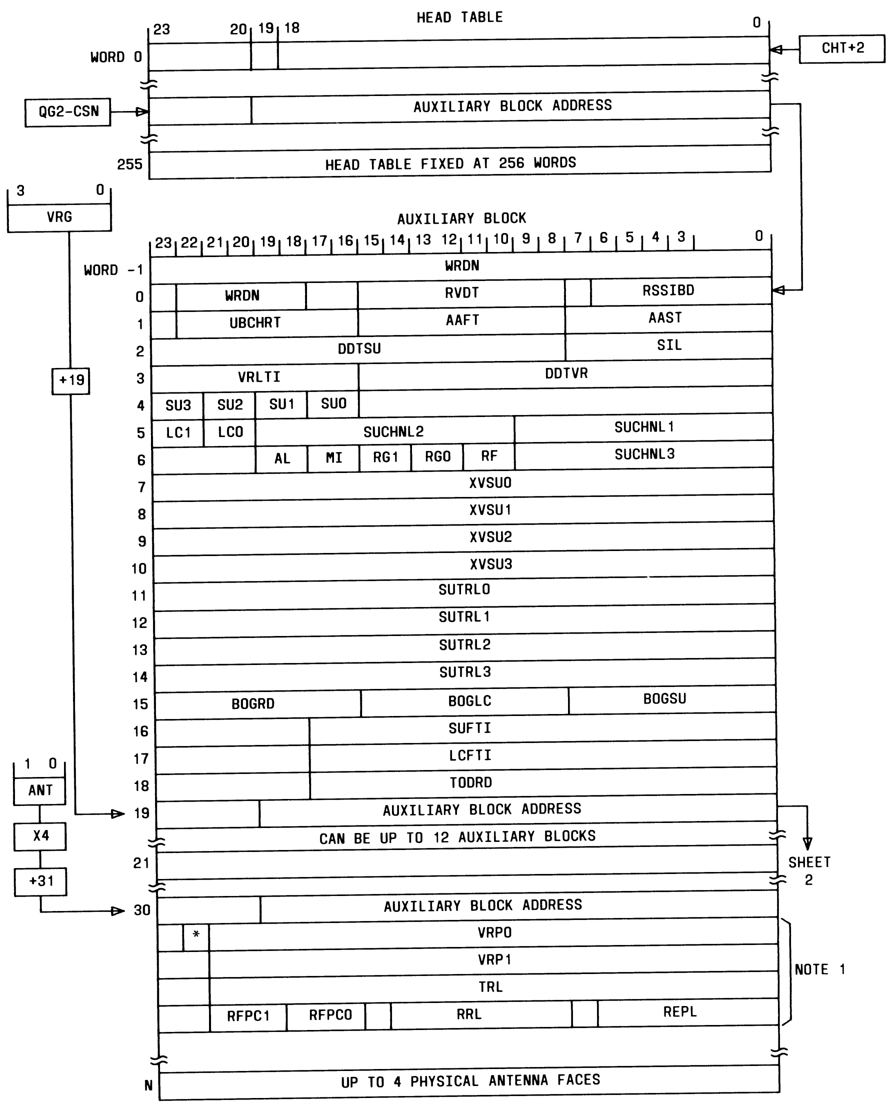


Fig. 26—Cell Master Equipage Translator (Sheet 1 of 2)

Scotty's Spectrum Analyzer – Analog–to–Digital Converter

Overview

This is my version of the analog–to–digital converter for Scotty Sprowls' Modularized Spectrum Analyzer (MSA) project. The original analog–to–digital converter design is SLIM–ADC–16.

The spectrum analyzer's Analog–to–Digital Converter (ADC) stage is based around (two) 16–bit Analog Devices AD7685 serial ADCs There is no need for any external (manual) reference adjustment to set the ADC conversion range and it'll still obtain excellent resolution in the MSA/VNA systems. Each ADC will digitize its input of 0 to 5 volts into a binary serial stream equal to 0 to 65,535. This equates to approximately 76.3 µV per bit resolution. Only one AD7685 will be used in this spectrum analyzer design. The second AD7685 for the VNA phase detector will be constructed and discussed in a future article.

The "MAGVOLTS" magnitude output from the logarithmic detector is connected to the ADC's input. This voltage range should be from +0.4 volts to +2.4 volts (over the AD8306's 100 dB range). The AD7685 will then convert +0.4 volts to a bit value of 5,243. The +2.4 volts will convert to a bit value of 31,457. The overall dynamic bit range is equal to 26,214 bits (31,457 – 5,243). Therefore, the conversion factor for the MSA's combination of logarithmic detector and 16–bit ADC is: 100 dB / 26,214 bits = 0.0038 dB per bit resolution. This is what determines the final displayed RF power magnitude on the spectrum analyzer.

Both ADCs will capture and clock–out their data simultaineously. The MSA software commands both ADCs to begin conversion with a single toggle of the `CONVERT` line. 16 toggles of the `SERCLOCK` line causes the AD7685 to output a serial stream of 16 bits. The Serial Data Output (SDO) of the AD7685 (pin 7) has a limited current (500 µA) capability. Therefore, a 2N2222 transistor provides buffering and current sinking to drive the `WAIT` and `ACK` lines on the controlling computer's parallel port (LPT). The computer's LPT port is normally a TTL–compatible input with an internal pull–up resistor to +5V. Having two pull–up resistors shouldn't hurt and should help make the circuit compatible with different computers. You may have to experiment with different BIOS settings for your computer's parallel port if you encounter problems.

To control the AD7685, two main control lines are used: `CONVERT` and `SERCLOCK`. Both AD7685 chips are controlled simultaneously. Before conversion, these lines are held low. To begin conversion, the `CONVERT` line is commanded high. This initiates the AD7685's in–chip sample–and–hold circuit. While `CONVERT` is high, any voltage changes on the analog input(s) will be disregarded. Also, the SDO output will be high impedance (`WAIT` and `ACK` will be high impedance).

It takes approximately 2 µS for the 16–bit conversion (sample) to take place. When complete, the 16–bit data word will be stored in the AD7685's buffer (hold). After conversion is complete, the `CONVERT` signal is brought low. The Most Significant Bit (MSB) D15 will be present on the SDO pin (there is a logic inversion by the 2N2222 on the line back to the computer, `WAIT` or `ACK`). Each time the `SERCLOCK` is brought low, the data word is shifted by one bit.

The data is valid 15 nanoseconds after the negative edge of `SERCLOCK`. It takes sixteen `SERCLOCKs` to shift out the 16–bit data word. If no data is clocked out of the buffer, the next `CONVERT` signal will overwrite the buffer.

MSA Software

The MSA software works in this way:

1.) It begins with `CONVERT` and `SERCLOCK` lines held low.

2.) `CONVERT` to high. This initiates the A–to–D conversion process.

3.) `CONVERT` to low. High–to–low takes about 5 µS, allowing the minimum 2 µS conversion time requirement.

4.) `SERCLOCK` to high. D15 MSB is valid on SDO, and is read by the computer.

5.) `SERCLOCK` to low. Next data word bit is shifted.

6.) `SERCLOCK` to high. D14 bit is valid on SDO, and is read by the computer.

7.) `SERCLOCK` to low. Next data word bit is shifted.

8.) `SERCLOCK` to high. D13 bit is valid on SDO, and is read by the computer.

9.) `SERCLOCK` to low. Next data word bit is shifted.

10.) `SERCLOCK` to high. D12 bit is valid on SDO, and is read by the computer.

11.) `SERCLOCK` to low. Next data word bit is shifted.

12.) `SERCLOCK` to high. D11 bit is valid on SDO, and is read by the computer.

13.) `SERCLOCK` to low. Next data word bit is shifted.

14.) `SERCLOCK` to high. D10 bit is valid on SDO, and is read by the computer.

15.) `SERCLOCK` to low. Next data word bit is shifted.

16.) `SERCLOCK` to high. D9 bit is valid on SDO, and is read by the computer.

17.) `SERCLOCK` to low. Next data word bit is shifted.

18.) `SERCLOCK` to high. D8 bit is valid on SDO, and is read by the computer.

19.) `SERCLOCK` to low. Next data word bit is shifted.

20.) `SERCLOCK` to high. D7 bit is valid on SDO, and is read by the computer.

21.) `SERCLOCK` to low. Next data word bit is shifted.

22.) `SERCLOCK` to high. D6 bit is valid on SDO, and is read by the computer.

23.) `SERCLOCK` to low. Next data word bit is shifted.

24.) `SERCLOCK` to high. D5 bit is valid on SDO, and is read by the computer.

25.) `SERCLOCK` to low. Next data word bit is shifted.

26.) `SERCLOCK` to high. D4 bit is valid on SDO, and is read by the computer.

27.) `SERCLOCK` to low. Next data word bit is shifted.

28.) `SERCLOCK` to high. D3 bit is valid on SDO, and is read by the computer.

29.) `SERCLOCK` to low. Next data word bit is shifted.

30.) `SERCLOCK` to high. D2 bit is valid on SDO, and is read by the computer.

31.) `SERCLOCK` to low. Next data word bit is shifted.

32.) `SERCLOCK` to high. D1 bit is valid on SDO, and is read by the computer.

33.) `SERCLOCK` to low. Next data word bit is shifted.

34.) `SERCLOCK` to high. D0 bit is valid on SDO, and is read by the computer.

35.) `SERCLOCK` to low. SDO is high impedance.

36.) Subsequent `SERCLOCKs` do nothing and the conversion process repeats.

Video Filter

This magnitude ADC circuit is designed with an optional input video bandwidth filter based around an Analog Devices ADG704 4–channel multiplexer. This will allow a selection of additional capacitance to be placed in parallel with the AD7685's input.

The ADG704 can be used to select four different integration times (video bandwidths) for the final displayed magnitude signal. The capacitor values for the video filter were chosen arbitrarily and you may wish to experiment with different values.

The video filter helps to remove excessive noise before the analog–to–digital conversion process and is a simple way to "narrow" to the response of the spectrum analyzer.

The MSA software video filter selections:

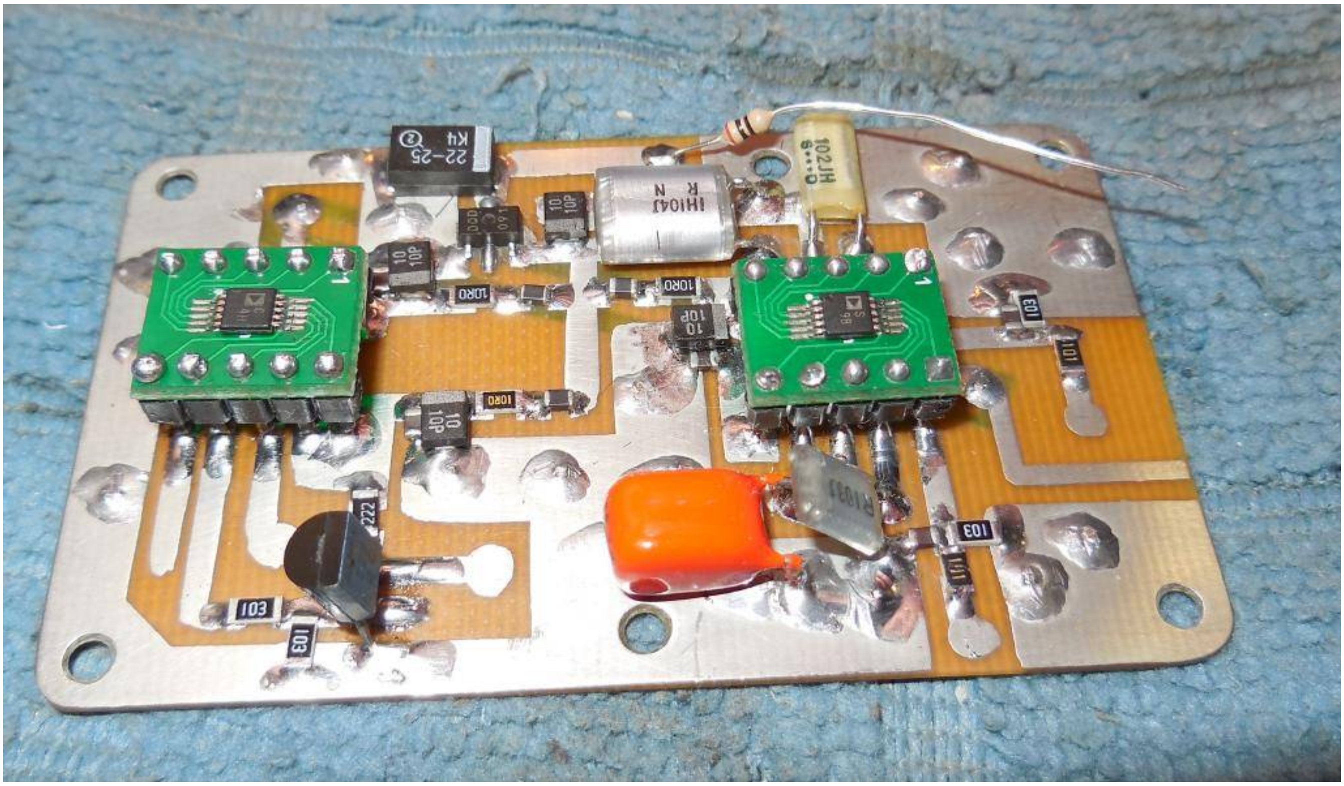
V0	V1	Filter Selection	Video Bandwidth
0	0	S1 – 1000 pF	Wide
0	1	S2 – 0.01 µF	Medium
1	0	S3 – 0.1 µF	Narrow
1	1	S4 – 1.0 µF	Extra Narrow

Scotty's software video filter controls may still be experimental at this point.

The video bandwidth determines the spectrum analyzer's capability to discriminate between two different power levels. This is because a narrower video bandwidth will remove noise in the logarithmic detector output. This filter is used to "smooth" the final display by removing any noise from the signal envelope.

(wikipedia.org/wiki/Spectrum_analyzer#Video_bandwidth)

Pictures & Construction Notes



Overview of the ADG704 video filter (right) and AD7685 16−bit ADC (left).

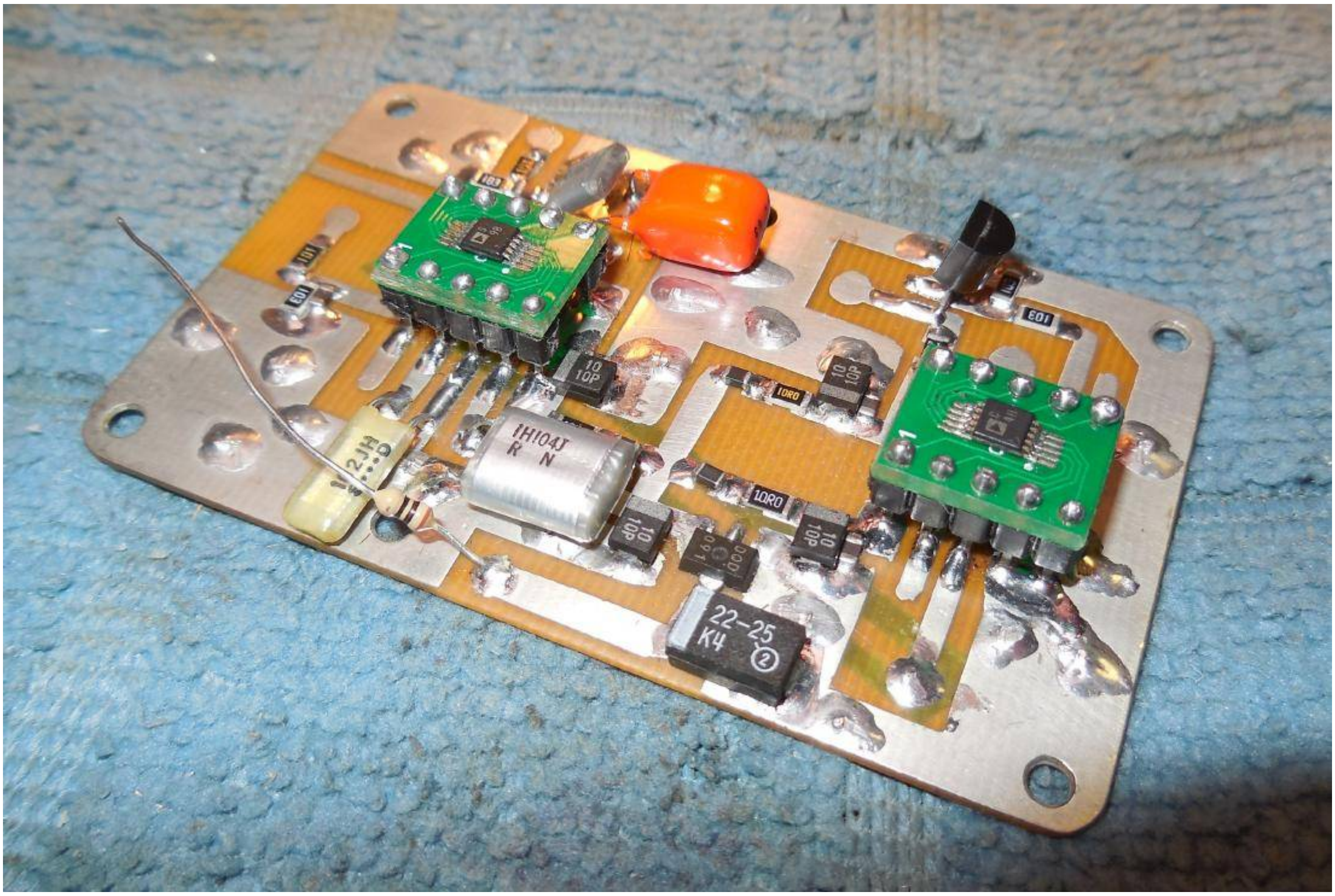
Both the AD7685 and the ADG704 are in 10−pin MSOP packages, so MSOP−to−DIP converters were used for soldering convenience.

Polystyrene capacitors are used in the video filter section and the large non−polarized orange capacitor (1 µF) is for the "extra narrow" video filter selection.

The 2N2222 transistor buffer is on the lower−left.

The SOT−89 device is a Sieko S−81250SG precision 5 volt regulator.

The "reference" voltage (pin 1) for the AD7685 should be very well filtered and regulated for maximum performance and magnitude resolution.



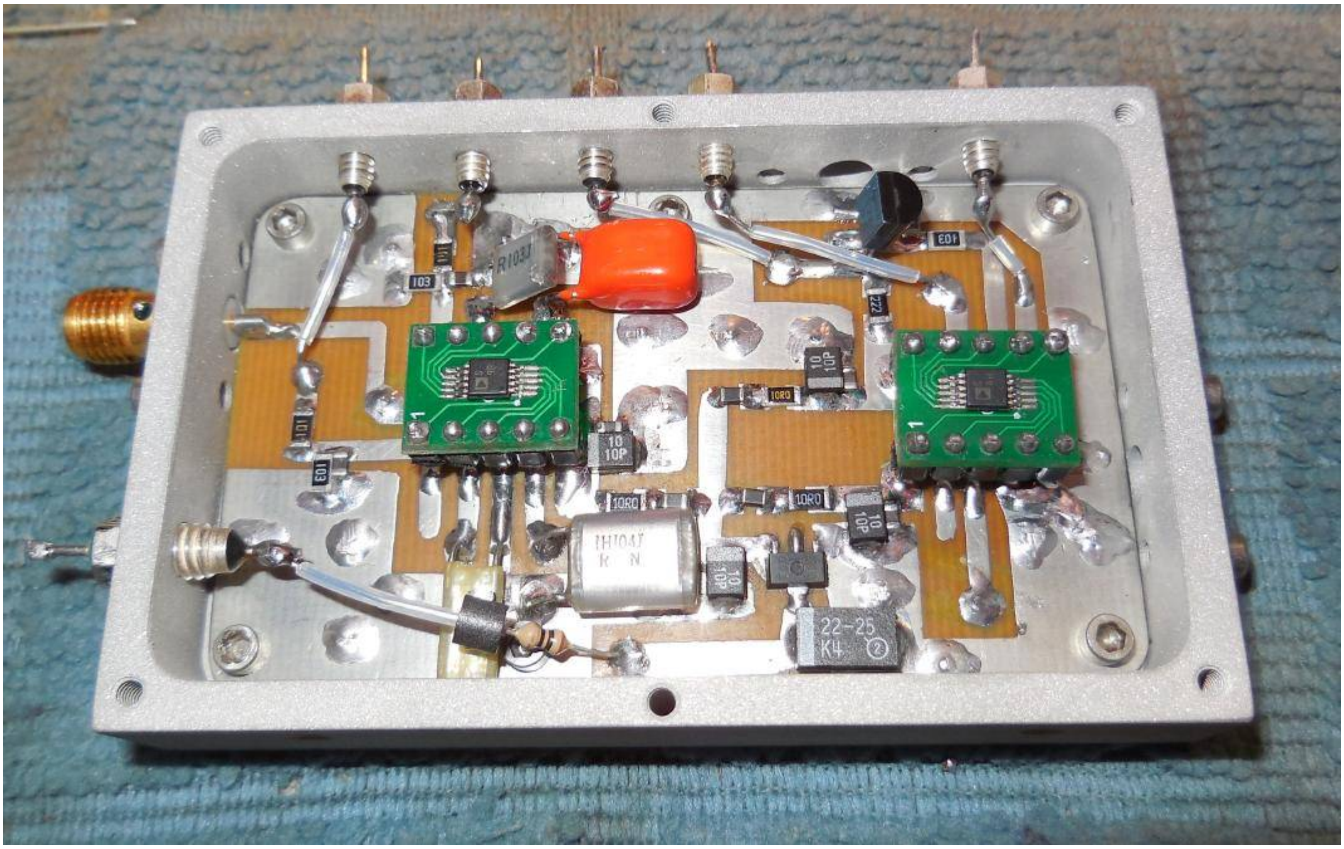
Alternate view.

The capacitors for the video filters should be low−leakage, non−microphonic, high−quality film types (polystyrene, Teflon, etc.). Otherwise, switching in the video filters could cause a small shift in the magnitude voltage.

The selectable video bandwidths are somewhat arbitrary. The wide video bandwidth is for the highest sweeping speed, medium for general speed, and narrow for very slow sweeping or to get the most accurate magnitude/phase data.

The ADG704 video filter is optional and if not used, a single 1000 pF capacitor should be added across the input (pin 3) of the AD7685.

This corresponds to a "wide" video filter as you do want a little bit of low−pass filtering here to keep the noise out, but not too much.



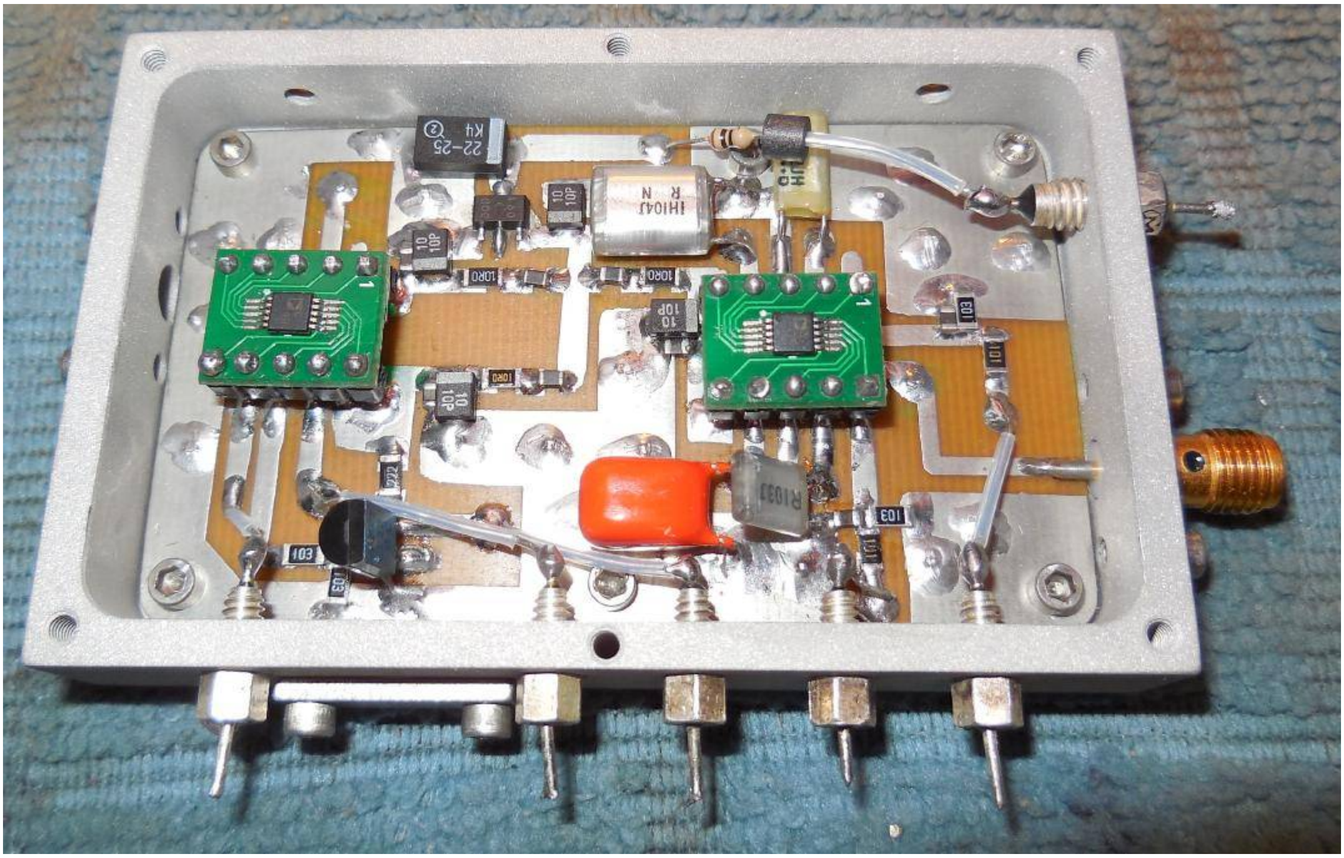
Completed overview of the analog−to−digital converter with video filter.

It's mounted inside an old 800 MHz cellular phone receive pre−amplifier case.

The SMA jack on the left is used for the **MAGVOLTS** input.

A 1000 pF feed−through capacitor (lower−left) is used for the +12 VDC power input.

180 pF feed−through capacitors are used for the ADG704 and AD7685 control lines. These should be low−value capacitors to avoid distorting the control waveforms.

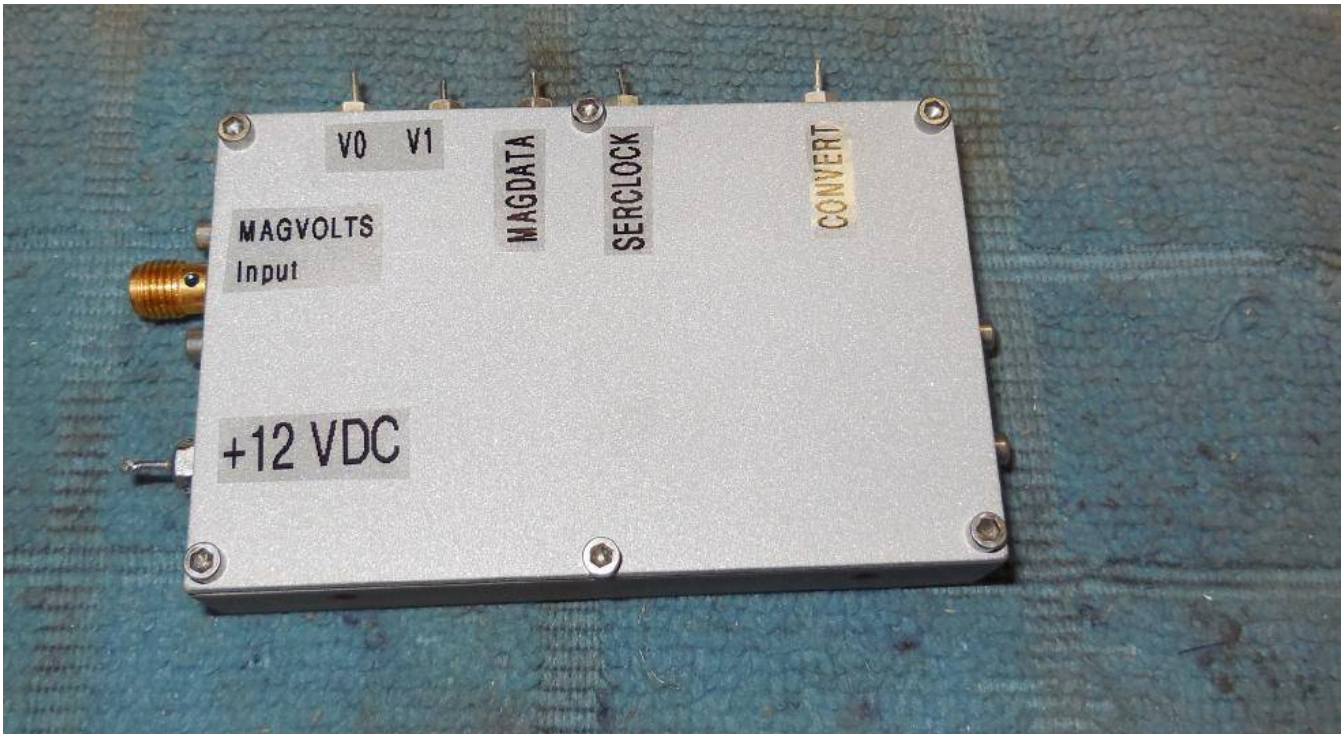


Alternate overview.

AD7685 voltage conversions:

Analog Input (Volts)	Digital Output (Hexadecimal – Binary)	
4.999924	FFFF	1111111111111111
2.500076	8001	1000000000000001
2.500000	8000	1000000000000000
2.499924	7FFF	0111111111111111
0.000076	0001	0000000000000001
0.000000	0000	0000000000000000
0.400000	147B	0001010001111011
2.400000	7AE1	0111101011100001

The two Least Significant Bits (LSB) are somewhat noisy which yields a more realistic 14–bit resolution. Therefore, with this circuit, the magnitude resolution of the MSA is actually around 0.01 dB.



Finished case overview.

The **MAGVOLTS** input of this module will then be connected back to the Logarithmic Detector stage. Be sure to use coaxial cable for this connection.

The `CONVERT`, `SERCLOCK`, `MAGDATA`, `V0`, and `V1` lines go back to their respective latches on the Control Board.

`CONVERT` goes to latch P3D7.

`SERCLOCK` goes to latch P3D6.

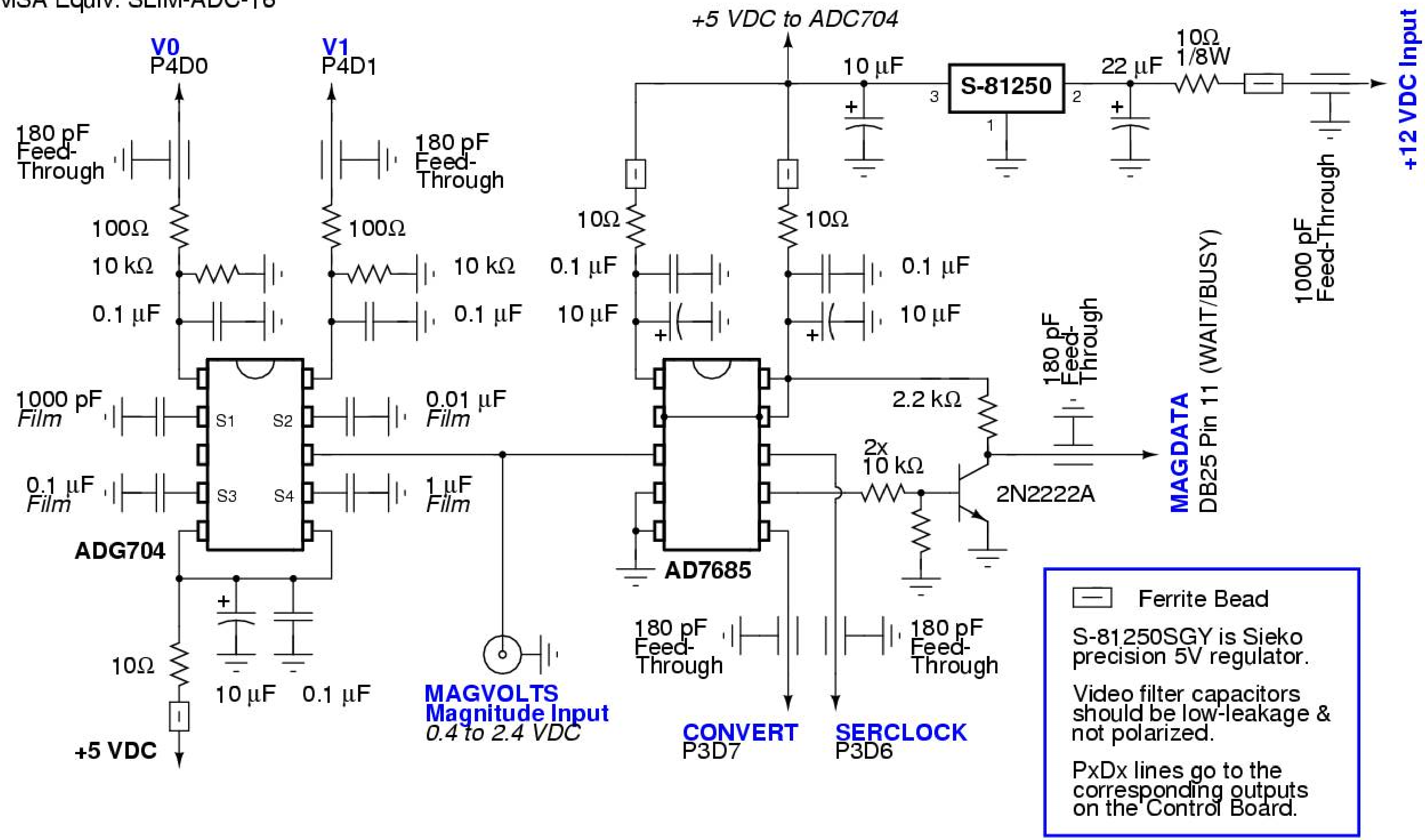
`MAGDATA` goes to WAIT (DB25 pin 11).

`V0` goes to latch P4D0.

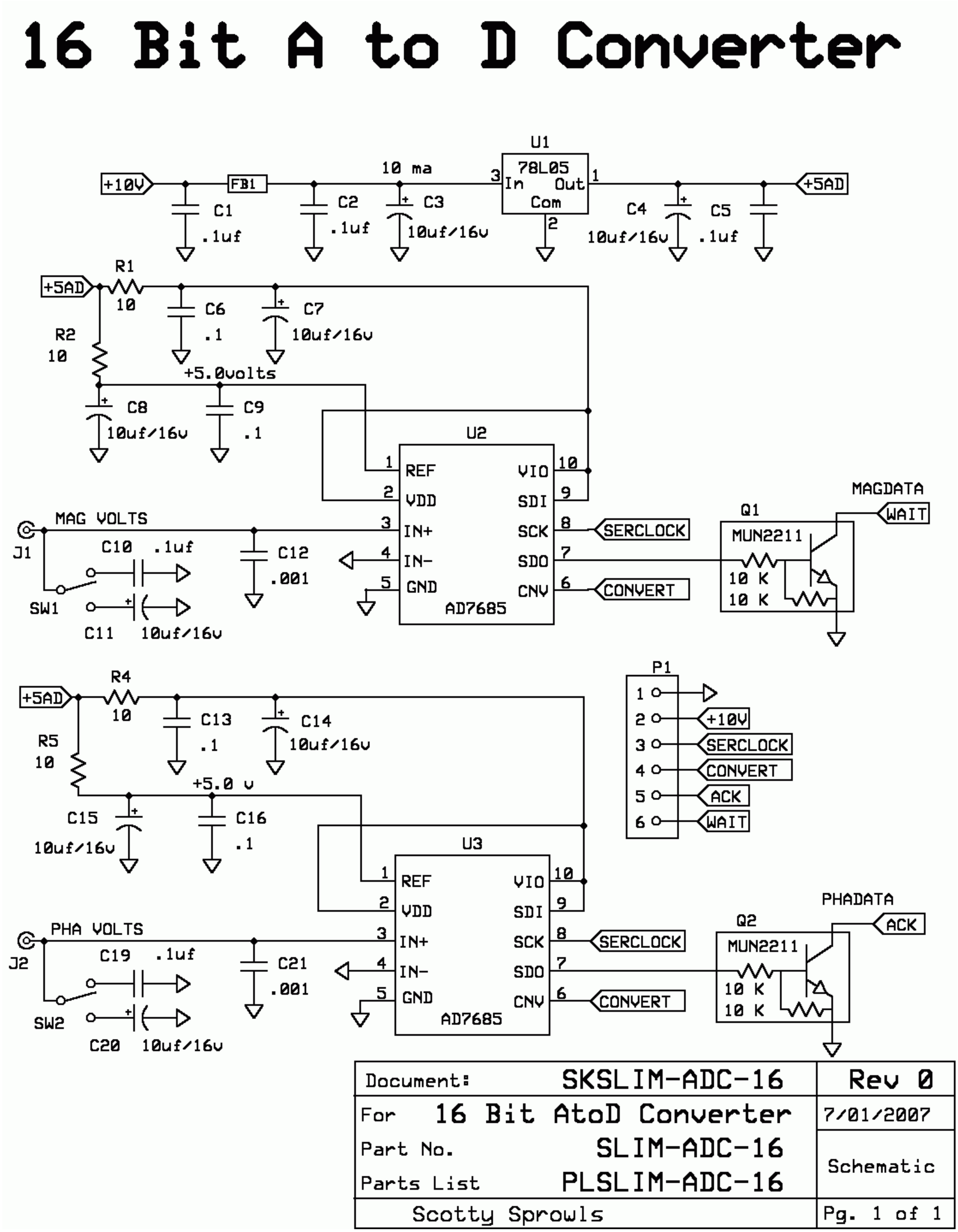
`V1` goes to latch P4D1.

Scotty's Spectrum Analyzer

Analog-to-Digital Converter with Video Filter
MSA Equiv. SLIM-ADC-16



Original SLIM–ADC–16 Schematic

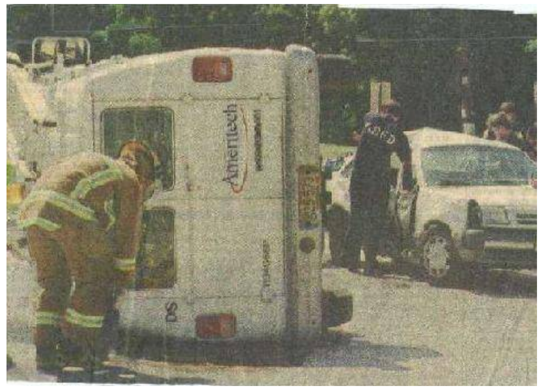


Bonus

"You didn't build that!"

How the fuck do you close a hole in the ground? LOL! Change!

End of Issue #114

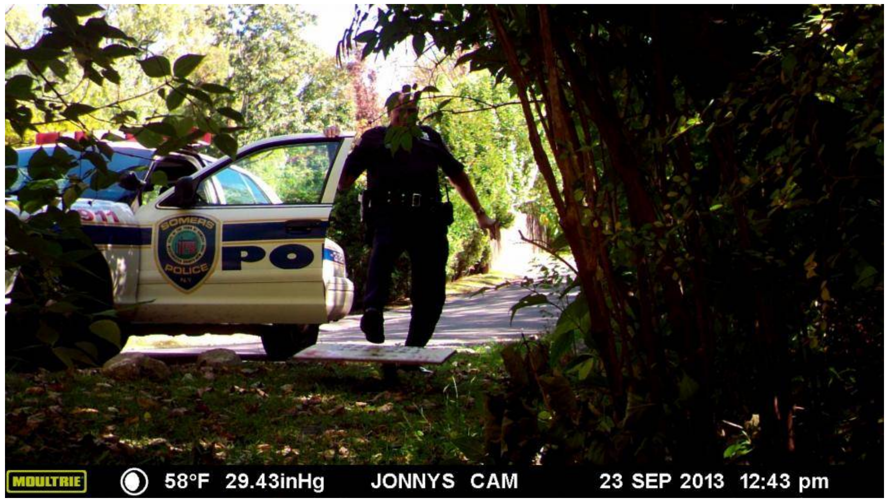


Any Questions?

Editorial and Rants

Jon Gibson of Lake Lincolndale, New York posted a sign in his yard protesting the anti-Second Amendment "NY SAFE Act."

After someone stole four of his signs, he decided to put up a motion-activated trail camera...



Well, well, well... It's the Somers, New York Police Department in action.

Change!

The U.S. Marine Corps War Memorial in Washington D.C. closed because of Obongo and the Democrats failure to make a budget which doesn't bankrupt the entire country.

These memorials cost very little to run, and a troop of Boy/Girl Scouts could (should) manage them while the federal government "shuts down."

Uh−oh!

Looks like someone knocked over the barricades and are now illegally trespassing on federal government property!

Don't let Obama know or he'll send a Predator drone after you!

Don't worry, it was just the Syracuse Honor Flight showing Obama what they think of his "change."

The "shutdown" World War 2 memorial in Washington D.C. has better security than our borders!

Remember when Americans could park their own cars without the government's help?