Digital Energy
MDS

INSTRUCTION SHEET

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The LEDR Interleave setting

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GE MDS LEDR

Interleaving in the LEDR 2 Radio

LEDR interleave setting

In digital communications, interference often occurs in the form of short noise bursts. These bursts normally corrupt a series of consecutive bits.

Interleaving is a digital algorithm that allows Forward Error Correction (FEC) to better handle bursts of noise. Interleaving reorders the data so that the symbols that would normally be neighbors in a given block are spread among multiple blocks. FEC works on a block of data of a specific size and can properly correct errors as long as the number of errors is small enough. With interleaving, the number of errors that occur within a single block is reduced, thereby allowing the FEC to more effectively correct burst errors.

As a simple example, consider a system with blocks consisting of 4 data bytes of which one can be corrected. An example data sequence looks like this:

(1) ABCD EFGH IJKL MNOP

With one error, the sequence may look like this:

(2) ABCD XFGH IJKL MNOP

This is corrected by FEC to yield the original sequence (1). Now consider what would happen (without interleaving) if there were three burst-induced byte errors:

(3) ABCD XXXH IJKL MNOP

Since all three errors occur within one block, they cannot all be corrected, so the best the FEC can do might look like this:

(4) ABCD XFXH IJKL MNOP

Now consider what the sequence might look like with interleaving. In this scheme, new blocks consist of the first, second, third, and fourth byte from each block respectively:

(5) AEIM BFJN CGKO DHLP

Here is what the sequence looks like with the same burst of errors:

(6) AEIM XXXN CGKO DHLP

When the blocks are deinterleaved, they look like this:

(7) AXCD EXGH IXKL MNOP

Notice that each block now holds just one error. Now all three errors may be corrected to yield the original sequence (1).

The LEDR 2 radio system supports a series of up to 12 blocks of 188 data bytes and 16 error control bytes each. The FEC error control coding within these blocks can properly correct 8 symbol (byte) errors.

Consider an example for a bit rate of 768 kbps. In this case a bit time is 1.3 us and the symbol (byte) time is 10.4 us. Let's calculate the longest noise burst that can theoretically be corrected. Without interleaving, we can withstand a burst that is 8 bytes x 10.4 us = 83.2 us long.

Now let's consider 12 block interleaving for the same rate. Assuming bits are spread equally among the 12 blocks, we can correct for a burst that is 12 times longer, or almost 1 ms.

Other combinations of Interleave Depths and Data Rates may be calculated as follows:

burst (ms) = depth x 8 (bits/byte) x 8 (errors/block) / rate (kbps)

Examples are listed in the following table. Keep in mind that this assumes the data is perfectly rearranged within the interleaved blocks. Further, framing and overhead not considered. Actual performance may vary.

Theoretical LEDR 2 Burst Immunity vs. Interleave Depth and Data Rate

			Interleave Depth			
DataRate	1	2	3	4	6	12
(kbps)		Theoretical Burst Immunity (ms)				
8192	0.008	0.016	0.023	0.031	0.047	0.094
6176	0.010	0.021	0.031	0.041	0.062	0.124
2048	0.031	0.063	0.094	0.125	0.188	0.375
1544	0.041	0.083	0.124	0.166	0.249	0.497
768	0.083	0.167	0.250	0.333	0.500	1.000
512	0.125	0.250	0.375	0.500	0.750	1.500
384	0.167	0.333	0.500	0.667	1.000	2.000
256	0.250	0.500	0.750	1.000	1.500	3.000
128	0.500	1.000	1.500	2.000	3.000	6.000
64	1.000	2.000	3.000	4.000	6.000	12.000

Something to note about interleaving is that deeper interleaving increases latency and lock time. This is because the modem must store multiple blocks before deinterleaving them. The theoretical latency induced by interleaving at a given depth for a given data rate can be calculated as follows:

Latency (ms) = depth x 8 (bits/byte) x 204 (bytes/block) / rate (kbps)

This does not account for framing or other customer data provisions that may increase latency.

Theoretical LEDR 2 Latency vs. Interleave Depth and Data Rate

			Interleave Depth			
Data Rate	1	2	3	4	6	12
(kbps)		Theoretical Latency (ms)				
8192	0.2	0.4	0.6	0.8	1.2	2.4
6176	0.3	0.5	0.8	1.1	1.6	3.2
2048	0.8	1.6	2.4	3.2	4.8	9.6
1544	1.1	2.1	3.2	4.2	6.3	12.7
768	2.1	4.3	6.4	8.5	12.8	25.5
512	3.2	6.4	9.6	12.8	19.1	38.3
384	4.3	8.5	12.8	17.0	25.5	51.0
256	6.4	12.8	19.1	25.5	38.3	76.5
128	12.8	25.5	38.3	51.0	76.5	153.0
64	25.5	51.0	76.5	102.0	153.0	306.0

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